16-Bit, 1 MSPS, 8-Channel Data Acquisition System

Data Sheet

ADAS3022

FEATURES

Ease of use—16-bit, 1 MSPS complete data acquisition system
High impedance, 8-channel input: >500 MΩ
Differential input voltage range: ±24.576 V maximum
High input common-mode rejection: >100 dB
User-programmable input ranges
Channel sequencer with individual channel gains
On-chip 4.096 V reference and buffer
Auxiliary input—direct interface to PulSAR ADC inputs
No latency or pipeline delay (SAR architecture)
Serial 4-wire, 1.8 V to 5 V SPI-/SPORT-compatible interface
LFCSP package (6 mm × 6 mm)
−40°C to +85°C industrial temperature range

APPLICATIONS

Multichannel data acquisition and system monitoring
Process control
Power line monitoring
Automated test equipment
Instrumentation

GENERAL DESCRIPTION

The ADAS3022 is a complete 16-bit, 1 MSPS, successive approximation–based analog-to-digital data acquisition system, which is manufactured on Analog Devices, Inc., proprietary *i*CMOS® high voltage industrial process technology. The device integrates an 8-channel, low leakage multiplexer; a high impedance programmable gain instrumentation amplifier (PGIA) stage with high common-mode rejection; a precision, low drift 4.096 V reference and buffer; and a 16-bit charge redistribution analog-to-digital converter (ADC) with successive approximation register (SAR) architecture. The ADAS3022 can resolve eight single-ended inputs or four fully differential inputs up to ±24.576 V when using ±15 V supplies. In addition, the device can accept the commonly used bipolar differential, bipolar single-ended, pseudo bipolar, or pseudo unipolar input signals, as shown in Table 1, thus enabling the use of almost any direct sensor interface.

The ADAS3022 simplifies design challenges by eliminating signal buffering, level shifting, amplification/attenuation, common-mode rejection, settling time, and any other analog signal conditioning challenge while allowing a smaller form factor, faster time to market, and lower cost.

Table 1. Typical Input Range Selection

Signal	Input Range, V_{IN}
Differential	
±1 V	±1.28 V
±2.5 V	±2.56 V
±5 V	±5.12 V
±10 V	±10.24 V
Single Ended[1]	
0 V to 1 V	±1.28 V
0 V to 2.5 V	±2.56 V
0 V to 5 V	±5.12 V
0 V to 10 V	±10.24 V

[1] See Figure 59 and Figure 60 in the Analog Inputs section for more information.

FUNCTIONAL BLOCK DIAGRAM

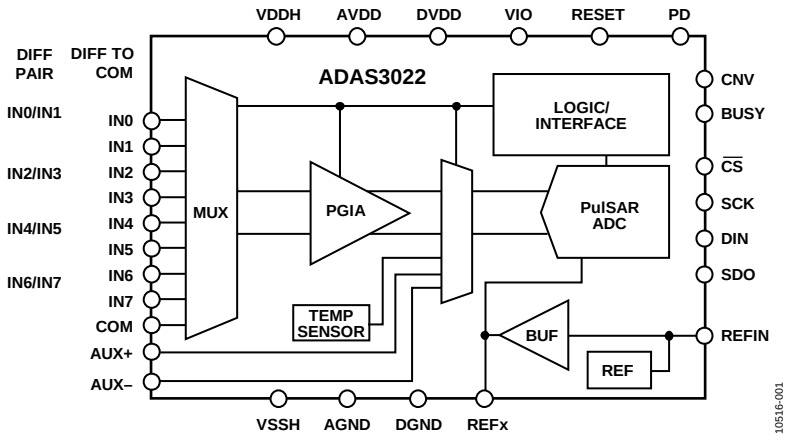

Figure 1.

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Technical Support
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ADAS3022* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADAS3022 Evaluation Kit

DOCUMENTATION

Data Sheet

- ADAS3022-EP: Enhanced Data Sheet
- ADAS3022: 16-Bit, 1 MSPS, 8-Channel Data Acquisition System Data Sheet

User Guides

- UG-484: Evaluation Board for the ADAS3022 16-Bit, 8-Channel, 1 MSPS Data Acquisition System

TOOLS AND SIMULATIONS

- ADAS3022 FPGA Reference Design
- ADAS3022/ADAS3023 IBIS Model

REFERENCE DESIGNS

- CN0201

REFERENCE MATERIALS

Press

- Analog Devices' Data Acquisition IC Simplifies Industrial and Instrumentation Equipment Design

Technical Articles

- Exploring Different SAR ADC Analog Input Architectures
- Komplette Sensor-to-Bits-Lösung: Vereinfachte Entwicklung industrieller Datenerfassungssysteme
- Let's Compare SAR & Δ-Σ Converters for a Mux'd DAS (Planet Analog, 12/2013)
- Sensor-To-Bits: Simplifying DAQ Design

DESIGN RESOURCES

- ADAS3022 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADAS3022 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

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DOCUMENT FEEDBACK

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11/12—Revision 0: Initial Version

SPECIFICATIONS

VDDH = 15 V ± 5%, VSSH = −15 V ± 5%, AVDD = DVDD = 5 V ± 5%, VIO = 1.8 V to AVDD, internal reference, V_{REF} = 4.096 V, f_S = 1 MSPS. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
RESOLUTION		16			Bits
ANALOG INPUTS—IN[7:0], COM					
Operating Input Voltage Range	V_{IN}	−VSSH + 2.5		VDDH − 2.5	V
Differential Input Voltage Range, V_{IN}	$V_{IN+} - V_{IN-}$				
	PGIA gain = 0.16, V_{IN} = 49.15 V p-p	$-6V_{REF}$		$+6V_{REF}$	V
	PGIA gain = 0.2, V_{IN} = 40.96 V p-p	$-5V_{REF}$		$+5V_{REF}$	V
	PGIA gain = 0.4, V_{IN} = 20.48 V p-p	$-2.5V_{REF}$		$+2.5V_{REF}$	V
	PGIA gain = 0.8, V_{IN} = 10.24 V p-p	$-1.25V_{REF}$		$+1.25V_{REF}$	V
	PGIA gain = 1.6, V_{IN} = 5.12 V p-p	$-0.625V_{REF}$		$+0.625V_{REF}$	V
	PGIA gain = 3.2, V_{IN} = 2.56 V p-p	$-0.3125V_{REF}$		$+0.3125V_{REF}$	V
	PGIA gain = 6.4, V_{IN} = 1.28 V p-p	$-0.1563V_{REF}$		$+0.1563V_{REF}$	V
Input Impedance	Z_{IN}	500			MΩ
Channel Off Leakage			±0.6		nA
Channel On Leakage			±0.02		nA
Common-Mode Voltage Range[2]	V_{IN+}, V_{IN-}; full-scale differential inputs				
	PGIA gain = 0.4	−5.12		+5.12	V
	PGIA gain = 0.8	−7.68		+7.68	V
	PGIA gain = 1.6	−8.96		+8.96	V
	PGIA gain = 3.2	−9.60		+9.60	V
	PGIA gain = 6.4	−9.92		+9.92	V
ANALOG INPUTS—AUX+, AUX−					
Differential Input Voltage Range		$-V_{REF}$		$+V_{REF}$	V
THROUGHPUT					
Conversion Rate	One channel/one pair	0		1000	kSPS
	Two channels/two pairs	0		500	kSPS
	Four channels/four pairs	0		250	kSPS
	Eight channels	0		125	kSPS
Transient Response	Full-scale step			520	ns
DC ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error	PGIA gain = 0.16, 0.2, 0.4, 0.8, 1.6	−2	±0.6	+2	LSB
	PGIA gain = 3.2	−3	±1.0	+3	LSB
	PGIA gain = 6.4	−5	±1.5	+5	LSB
Differential Linearity Error	PGIA gain = 0.16, 0.2, 0.4, 0.8, 1.6	−0.9	±0.6	+1.0	LSB
	PGIA gain = 3.2	−0.9	±0.75	+1.25	LSB
	PGIA gain = 6.4	−0.9	±0.75	+1.25	LSB
Transition Noise	External reference				
	PGIA gain = 0.16, 0.2, 0.4, 0.8, 1.6		5		LSB
	PGIA gain = 3.2		7		LSB
	PGIA gain = 6.4		11		LSB
Gain Error	External reference, all PGIA gains, T_A = 25°C	−9		+9	LSB
Gain Error Temperature Drift	External reference, all PGIA gains			0.1	ppm/°C
Offset Error	External reference, T_A = 25°C				
	PGIA gain = 0.16, 0.2, 0.4, 0.8	−3.0	+0.2	+3.0	LSB
	PGIA gain = 1.6	−4.0	+0.2	+4.0	LSB
	PGIA gain = 3.2	−7.5	+0.2	+7.5	LSB
	PGIA gain = 6.4	−12.5	+0.2	+12.5	LSB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
Offset Error Temperature Drift	External reference				
	PGIA gain = 0.16, 0.2, 0.4, 0.8		0.1	0.5	ppm/°C
	PGIA gain = 1.6		0.2	1.0	ppm/°C
	PGIA gain = 3.2		0.4	2.0	ppm/°C
	PGIA gain = 6.4		0.8	4.0	ppm/°C
Total Unadjusted Error	External reference, T_A = 25°C				
	PGIA gain = 0.16, 0.2, 0.4, 0.8, 1.6, 3.2	−9		+9	LSB
	PGIA gain = 6.4	−15		+15	LSB
AC ACCURACY[3]					
Signal-to-Noise Ratio (SNR)	f_{IN} = 10 kHz				
	PGIA gain = 0.16	90.0	91.5		dB
	PGIA gain = 0.2	90.0	91.5		dB
	PGIA gain = 0.4	89.5	91.5		dB
	PGIA gain = 0.8	89.0	91.0		dB
	PGIA gain = 1.6	88.0	89.7		dB
	PGIA gain = 3.2	86.0	86.8		dB
	PGIA gain = 6.4	83.0	84.5		dB
Signal-to-Noise-and-Distortion (SINAD)	f_{IN} = 10 kHz				
	PGIA gain = 0.16	88.0	90.0		dB
	PGIA gain = 0.2	88.0	90.0		dB
	PGIA gain = 0.4	88.5	91.0		dB
	PGIA gain = 0.8	88.5	90.5		dB
	PGIA gain = 1.6	87.5	89.5		dB
	PGIA gain = 3.2	85.5	86.5		dB
	PGIA gain = 6.4	82.5	84.0		dB
Dynamic Range	f_{IN} = 10 kHz, −60 dB input				
	PGIA gain = 0.16	91.0	92.0		dB
	PGIA gain = 0.2	91.0	92.0		dB
	PGIA gain = 0.4	90.5	91.5		dB
	PGIA gain = 0.8	90.0	91.0		dB
	PGIA gain = 1.6	89.0	90.0		dB
	PGIA gain = 3.2	86.0	87.0		dB
	PGIA gain = 6.4	83.5	85.0		dB
Total Harmonic Distortion	f_{IN} = 10 kHz, all PGIA gains		−100		dB
Spurious-Free Dynamic Range	f_{IN} = 10 kHz, all PGIA gains		101		dB
Channel-to-Channel Crosstalk	f_{IN} = 10 kHz, all channels inactive		−120		dB
Common-Mode Rejection Ratio (CMRR)	f_{IN} = 2 kHz				
	PGIA gain = 0.16, 0.2, 0.4, 0.8	90.0	110.0		dB
	PGIA gain = 1.6	90.0	105.0		dB
	PGIA gain = 3.2	90.0	98.0		dB
	PGIA gain = 6.4	90.0	98.0		dB
−3 dB Input Bandwidth	−40 dBFS		8		MHz
AUXILIARY ADC INPUT CHANNEL					
DC Accuracy	External reference				
Integral Nonlinearity Error		−1.5	±0.5	+1.5	LSB
Differential Nonlinearity Error		−0.8	±0.6	+1.0	LSB
Gain Error		−2.5	±0.2	+2.5	LSB
Offset Error		−5	±0.2	+5	LSB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
AC Performance	Internal reference				
Signal-to-Noise Ratio (SNR)		90.0	93.0		dB
Signal-to-Noise-and-Distortion (SINAD)		89.5	92.5		dB
Total Harmonic Distortion			−105		dB
Spurious-Free Dynamic Range (SFDR)			110		dB
INTERNAL REFERENCE					
REFx Output Voltage	T_A = 25°C	4.088	4.096	4.104	V
REFx Output Current	T_A = 25°C		250		µA
REFx Temperature Drift	REFEN = 1		±5		ppm/°C
	REFEN = 0		±1		ppm/°C
REFx Line Regulation	AVDD = 5 V ± 5%				
Internal Reference			20		µV/V
Buffer Only			4		µV/V
REFIN Output Voltage[4]	T_A = 25°C	2.495	2.500	2.505	V
Turn-On Settling Time	C_{REFIN}, C_{REF1}, C_{REF2} = 10 µF and 0.1 µF		100		ms
EXTERNAL REFERENCE					
Voltage Range	REFx input	4.000	4.096	4.104	V
	REFIN input (buffered)		2.5	2.505	V
Current Drain	V_{REF} = 4.096 V		100		µA
TEMPERATURE SENSOR					
Output Voltage	T_A = 25 °C		275		mV
Temperature Sensitivity			800		µV/°C
DIGITAL INPUTS					
Logic Levels					
V_{IL}	VIO > 3 V	−0.3		+0.3 × VIO	V
V_{IH}	VIO > 3 V	0.7 × VIO		VIO + 0.3	V
V_{IL}	VIO ≤ 3 V	−0.3		+0.1 × VIO	V
V_{IH}	VIO ≤ 3 V	0.9 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS[5]					
Data Format			Twos complement		
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES	PD = 0				
VIO		1.8		AVDD + 0.3	V
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
VDDH[6]	VDDH > input voltage + 2.5 V	14.25	15	15.75	V
VSSH[6]	VSSH < input voltage − 2.5 V	−15.75	−15	−14.25	V
I_{VDDH}	PGIA gain = 0.16		3.0	3.5	mA
	PGIA gain = 0.2		3.0	3.5	mA
	PGIA gain = 0.4		3.5	4.0	mA
	PGIA gain = 0.8		5.0	5.5	mA
	PGIA gain = 1.6		8.5	9.5	mA
	PGIA gain = 3.2		15.5	17.5	mA
	PGIA gain = 6.4		15.5	17.5	mA
	All PGIA gains, PD = 1		100		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
I_{VSSH}	PGIA gain = 0.16	−3.0	−2.5		mA
	PGIA gain = 0.2	−3.0	−2.5		mA
	PGIA gain = 0.4	−3.5	−3.0		mA
	PGIA gain = 0.8	−5.5	−4.5		mA
	PGIA gain = 1.6	−9.5	−8.0		mA
	PGIA gain = 3.2	−17.5	−15		mA
	PGIA gain = 6.4	−17.5	−15		mA
	All PGIA gains, PD = 1		10		µA
I_{AVDD}	PGIA gain = 6.4, reference buffer enabled		18	21.0	mA
	All other PGIA gains, reference buffer enabled		16	19.0	mA
	PGIA gain = 6.4, reference buffer disabled		14	17.5	mA
	All other PGIA gains, reference buffer disabled		12	16.0	mA
	All PGIA gains, PD = 1		100		µA
I_{DVDD}	All PGIA gains, PD = 0		2.5	3.5	mA
	All PGIA gains, PD = 1		10		µA
I_{VIO}	VIO = 3.3 V, PD = 0		0.30	1.2	mA
	PD = 1		10		µA
Power Supply Sensitivity					
At T_A = 25°C	External reference				
	PGIA gain = 0.16, 0.2, 0.4, 0.8; VDDH/VSSH ± 5%		±0.5		LSB
	PGIA gain = 3.2, VDDH/VSSH ± 5%		±1.0		LSB
	PGIA gain = 6.4, VDDH/VSSH ± 5%		±2.0		LSB
	PGIA gain = 0.16, AVDD/DVDD ± 5%		±0.6		LSB
	PGIA gain = 0.2, AVDD/DVDD ± 5%		±0.8		LSB
	PGIA gain = 0.4, AVDD/DVDD ± 5%		±1.0		LSB
	PGIA gain = 0.8, AVDD/DVDD ± 5%		±1.5		LSB
	PGIA gain = 1.6, AVDD/DVDD ± 5%		±2.0		LSB
	PGIA gain = 3.2, AVDD/DVDD ± 5%		±3.5		LSB
	PGIA gain = 6.4, AVDD/DVDD ± 5%		±7.0		LSB
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] LSB means least significant bit and changes depending on the voltage range. See the Programmable Gain section for the LSB size.
[2] The common-mode voltage (V_{CM}) range for a PGIA gain of 0.16 or 0.2 is 0 V.
[3] All ac accuracy specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[4] This is the output from the internal band gap reference.
[5] There is no pipeline delay. Conversion results are available immediately after a conversion is complete.
[6] The differential input common-mode voltage (V_{CM}) range changes according to the maximum input range selected and the high voltage power supplies (VDDH and VSSH). Note that the specified operating input voltage of any input pin requires 2.5 V of headroom from the VDDH and VSSH supplies; therefore, (VSSH + 2.5 V) ≤ INx/COM ≤ (VDDH − 2.5 V).

TIMING SPECIFICATIONS

VDDH = 15 V ± 5%, VSSH = −15 V ± 5%, AVDD = DVDD = 5 V ± 5%, VIO = 1.8 V to AVDD, internal reference, V_{REF} = 4.096 V, f_S = 1 MSPS. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
Time Between Conversions	t_{CYC}				
Warp Mode,[1] CMS = 0		1		1000	µs
Normal Mode (Default), CMS = 1		1.1			µs
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}				
Warp Mode, CMS = 0			825		ns
Normal Mode (Default), CMS = 1			925	1000	ns
Auxiliary ADC Input Channel Acquisition Time	t_{ACQ}	600			ns
CNV Pulse Width	t_{CH}	10			ns
CNV High to Hold Time (Aperture Delay)	t_{AD}		2		ns
CNV High to Busy Delay	t_{CBD}			520	ns
Safe Data Access Time During Conversion	t_{DDC}			500	ns
Quiet Conversion Time (BUSY High)	t_{QUIET}				
Warp Mode, CMS = 0				400	ns
Normal Mode (Default), CMS = 1				500	ns
Data Access During Quiet Conversion Time	t_{DDCA}				
Warp Mode, CMS = 0				200	ns
Normal Mode (Default), CMS = 1				300	ns
SCK Period	t_{SCK}	15			ns
SCK Low Time	t_{SCKL}	5			ns
SCK High Time	t_{SCKH}	5			ns
SCK Falling Edge to Data Valid	t_{SDOH}	4			ns
SCK Falling Edge to Data Valid Delay	t_{SDOD}				
VIO > 4.5 V				12	ns
VIO > 3.0 V				18	ns
VIO > 2.7 V				24	ns
VIO > 2.3 V				25	ns
VIO > 1.8 V				37	ns
$\overline{CS}$/RESET/PD Low to SDO	t_{EN}				
VIO > 4.5 V				15	ns
VIO > 3.0 V				16	ns
VIO > 2.7 V				18	ns
VIO > 2.3 V				23	ns
VIO > 1.8 V				28	ns
$\overline{CS}$/RESET/PD High to SDO High Impedance	t_{DIS}			25	ns
DIN Valid Setup Time from SCK Rising Edge	t_{DINS}	4			ns
DIN Valid Hold Time from SCK Rising Edge	t_{DINH}	4			ns
CNV Rising to $\overline{CS}$	t_{CCS}	5			ns
RESET/PD High Pulse	t_{RH}	5			ns

[1] Exceeding the maximum time has an effect on the accuracy of the conversion (see the Conversion Modes section).

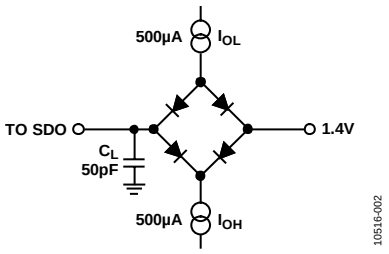


Figure 2. Load Circuit for Digital Interface Timing

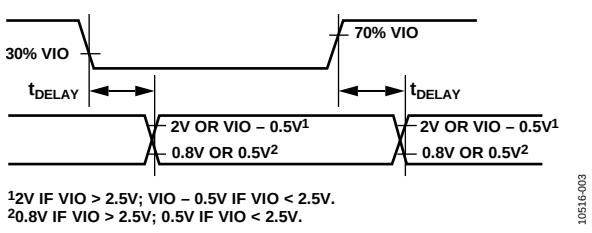
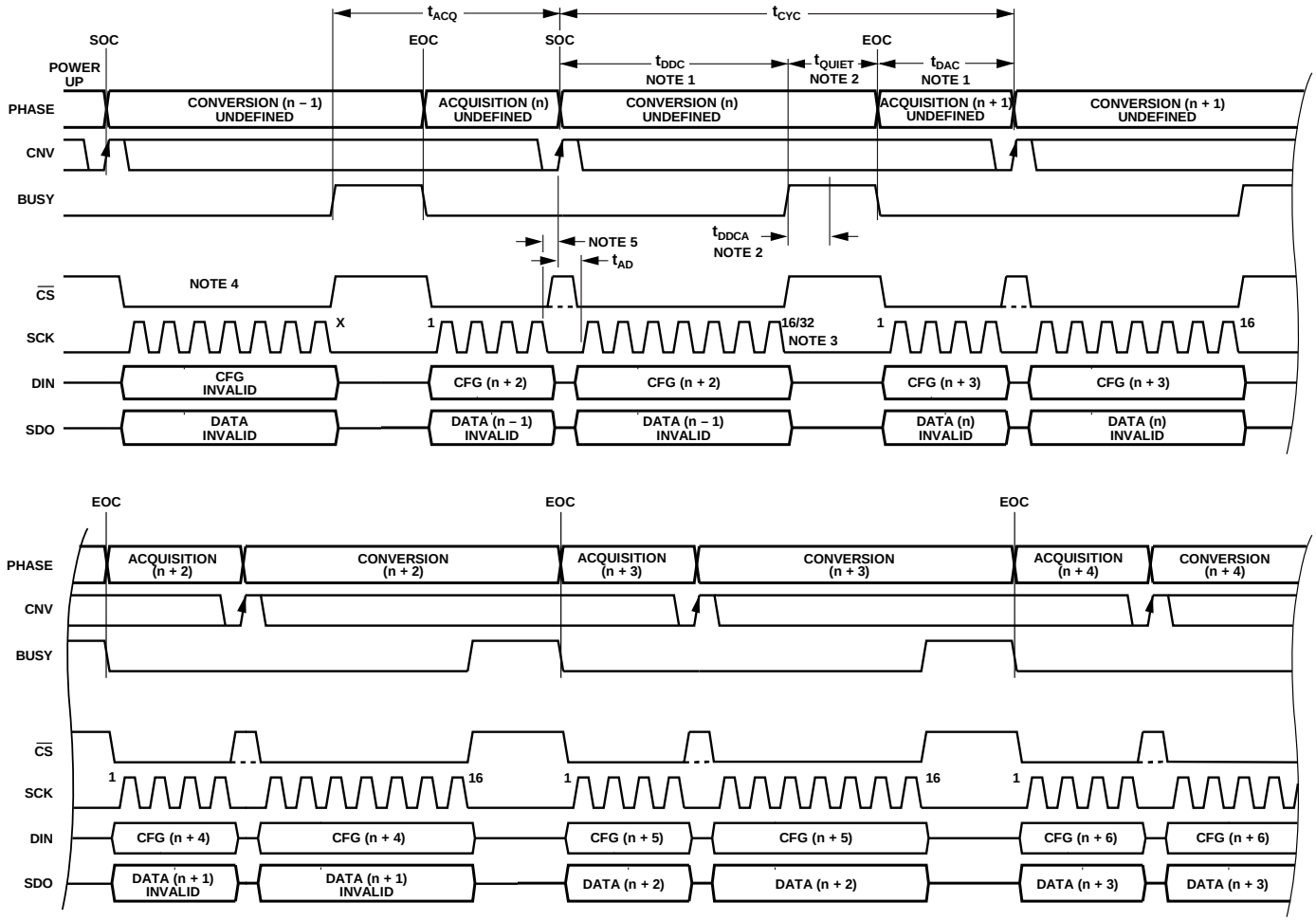


Figure 3. Voltage Levels for Timing



NOTES

1. DATA ACCESS CAN OCCUR DURING A CONVERSION (t_{DDC}), AFTER A CONVERSION (t_{DAC}), OR BOTH DURING AND AFTER A CONVERSION. THE CONVERSION RESULT AND THE CFG REGISTER ARE UPDATED AT THE END OF A CONVERSION (EOC).
2. DATA ACCESS CAN ALSO OCCUR UP TO t_{DDCA} WHILE BUSY IS ACTIVE (SEE THE DIGITAL INTERFACE SECTION FOR DETAILS). ALL OF THE BUSY TIME CAN BE USED TO ACQUIRE DATA.
3. A TOTAL OF 16 SCK FALLING EDGES IS REQUIRED FOR A CONVERSION RESULT. AN ADDITIONAL 16 EDGES ARE REQUIRED TO READ BACK THE CFG RESULT ASSOCIATED WITH THE CURRENT CONVERSION.
4. $\overline{CS}$ CAN BE HELD LOW OR CONNECTED TO CNV. $\overline{CS}$ WITH FULL INDEPENDENT CONTROL IS SHOWN IN THIS FIGURE.
5. FOR OPTIMAL PERFORMANCE, DATA ACCESS SHOULD NOT OCCUR DURING THE SAMPLING EDGE. A MINIMUM TIME OF THE APERTURE DELAY (t_{AD}) SHOULD ELAPSE PRIOR TO DATA ACCESS.

10516-028

Figure 4. General Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Analog Inputs/Outputs	
INx, COM to AGND	VSSH − 0.3 V to VDDH + 0.3 V
AUX+, AUX− to AGND	−0.3 V to AVDD + 0.3 V
REFx to AGND	AGND − 0.3 V to AVDD + 0.3 V
REFIN to AGND	AGND −0.3 V to +2.7 V
REFN to AGND	±0.3 V
Ground Voltage Differences	
AGND, RGND, DGND	±0.3 V
Supply Voltages	
VDDH to AGND	−0.3 V to +16.5 V
VSSH to AGND	+0.3 V to −16.5 V
AVDD, DVDD, VIO to AGND	−0.3 V to +7 V
ACAP, DCAP, RCAP to GND	−0.3 V to +2.7 V
Digital Inputs/Outputs	
CNV, DIN, SCK, RESET, PD, $\overline{CS}$ to DGND	−0.3 V to VIO + 0.3 V
SDO, BUSY to DGND	−0.3 V to VIO + 0.3 V
Internal Power Dissipation	2 W
Junction Temperature	125°C
Storage Temperature Range	−65°C to +125°C
θ_{JA} Thermal Impedance	44.1°C/W
θ_{JC} Thermal Impedance	0.28°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

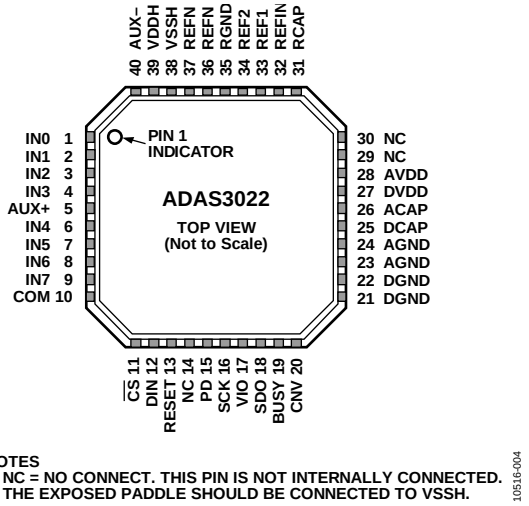


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1 to 4	IN0 to IN3	AI	Input Channel 0 to Input Channel 3.
5	AUX+	AI	Auxiliary Input Channel Positive Input.
6 to 9	IN4 to IN7	AI	Input Channel 4 to Input Channel 7.
10	COM	AI	IN[7:0] Common Channel Input. The IN[7:0] input channels can be referenced to a common point. The maximum voltage on this pin is ±10.24 V for all PGIA gains except for a PGIA gain of 0.16, in which case the maximum voltage on this pin is ±12.228 V. AUX+ and AUX− are not referenced to COM.
11	$\overline{CS}$	DI	Chip Select. Active low signal. Enables the digital interface for writing and reading data. Use this pin when sharing the serial bus. For a dedicated ADAS3022 serial interface, $\overline{CS}$ can be tied to DGND or CNV to simplify the interface.
12	DIN	DI	Data Input. Serial data input used for writing the 16-bit configuration word (CFG) that is latched on SCK rising edges. CFG is an internal register that is updated on the rising edge of the end of a conversion, which is the falling edge of BUSY. The configuration register can be written to during and after a conversion.
13	RESET	DI	Asynchronous Reset. A low-to-high transition resets the ADAS3022. The current conversion, if active, is aborted and CFG is reset to the default state.
14, 29, 30	NC	NC	No Connect. This pin is not connected internally.
15	PD	DI	Power-Down. A low-to-high transition powers down the ADAS3022, minimizing the bias current. Note that this pin must be held high until the user is ready to power on the device; after powering on the device, the user must wait 100 ms until the reference is enabled and then wait for the completion of two dummy conversions before the device is ready to convert. See the Power-Down Mode section for more information.
16	SCK	DI	Serial Clock Input. The DIN and SDO data sent to and from the ADAS3022 are synchronized with SCK.
17	VIO	P	Digital Interface Supply. Nominally, this supply should be at the same voltage as the supply of the host interface: 1.8 V, 2.5 V, 3.3 V, or 5 V.
18	SDO	DO	Serial Data Output. The conversion result is output on this pin and is synchronized to SCK falling edges. The conversion result is output in twos complement format.
19	BUSY	DO	Busy Output. An active high signal on this pin indicates that a conversion is in process. Reading or writing data during the quiet conversion phase (t_{QUIET}) may cause incorrect bit decisions.
20	CNV	DI	Convert Input. A conversion is initiated on the rising edge of this pin.
21, 22	DGND	P	Digital Ground. Connect these pins to the system digital ground plane.
23, 24	AGND	P	Analog Ground. Connect these pins to the system analog ground plane.
25	DCAP	P	Internal 2.5 V Digital Regulator Output. Decouple this internally regulated output using a 10 µF capacitor and a 0.1 µF local capacitor.
26	ACAP	P	Internal 2.5 V Analog Regulator Output. This regulator supplies power to the internal ADC core and all of the supporting analog circuits with the exception of the internal reference. Decouple this internally regulated output using a 10 µF capacitor and a 0.1 µF local capacitor.

Pin No.	Mnemonic	Type[1]	Description
27	DVDD	P	Digital 5 V Supply. Decouple this supply using a 10 µF capacitor and a 0.1 µF local capacitor.
28	AVDD	P	Analog 5 V Supply. Decouple this supply using a 10 µF capacitor and a 0.1 µF local capacitor.
31	RCAP	P	Internal 2.5 V Analog Regulator Output. This regulator supplies power to the internal reference. Decouple this pin using a 1 µF capacitor connected to RCAP and a 0.1 µF local capacitor.
32	REFIN	AI/O	Internal 2.5 V Band Gap Reference Output, Reference Buffer Input, or Reference Power-Down Input. See the Voltage Reference Input/Output section for more information.
33, 34	REF1, REF2	AI/O	Reference Input/Output. Regardless of the reference method, these pins need individual decoupling using external 10 µF ceramic capacitors connected as close to REF1, REF2, and REFN as possible. See the Voltage Reference Output/Input section for more information. REF1 and REF2 must be tied together externally.
35	RGND	P	Reference Supply Ground. Connect this pin to the system analog ground plane.
36, 37	REFN	P	Reference Input/Output Ground. Connect the 10 µF capacitors on REF1 and REF2 to these pins, and connect these pins to the system analog ground plane.
38	VSSH	P	High Voltage Analog Negative Supply. Nominally, the supply of this pin should be −15 V. Decouple this pin using a 10 µF capacitor and a 0.1 µF local capacitor.
39	VDDH	P	High Voltage Analog Positive Supply. Nominally, the supply of this pin should be +15 V. Decouple this pin using a 10 µF capacitor and a 0.1 µF local capacitor.
40	AUX−	AI	Auxiliary Input Channel Negative Input.
	EPAD		Exposed Paddle. The exposed paddle should be connected to VSSH.

[1]AI = analog input, AI/O = analog input/output, DI = digital input, DO = digital output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

VDDH = 15 V, VSSH = −15 V, AVDD = DVDD = 5 V, VIO = 1.8 V to AVDD, unless otherwise noted.

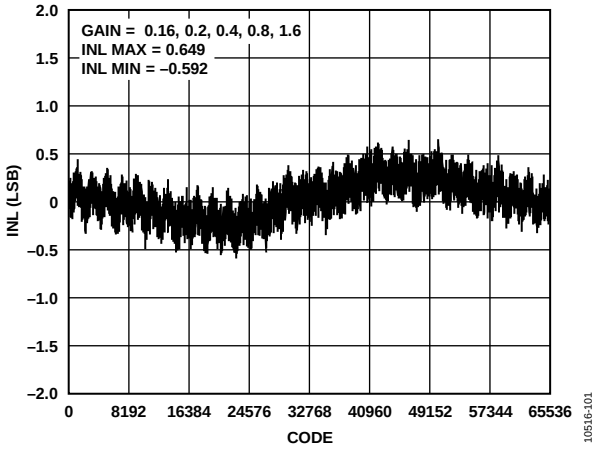


Figure 6. Integral Nonlinearity vs. Code, PGIA Gain = 0.16, 0.2, 0.4, 0.8, and 1.6

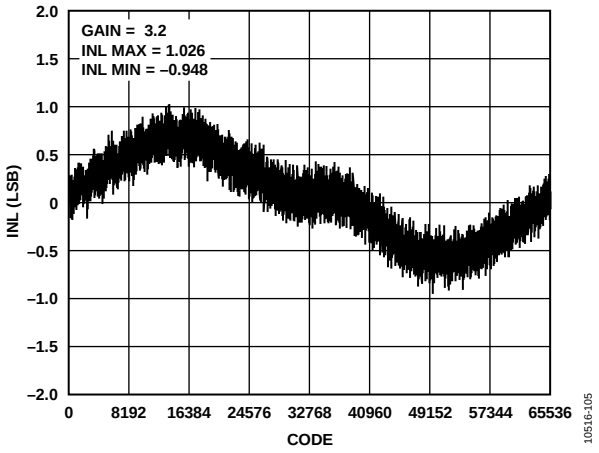


Figure 7. Integral Nonlinearity vs. Code, PGIA Gain = 3.2

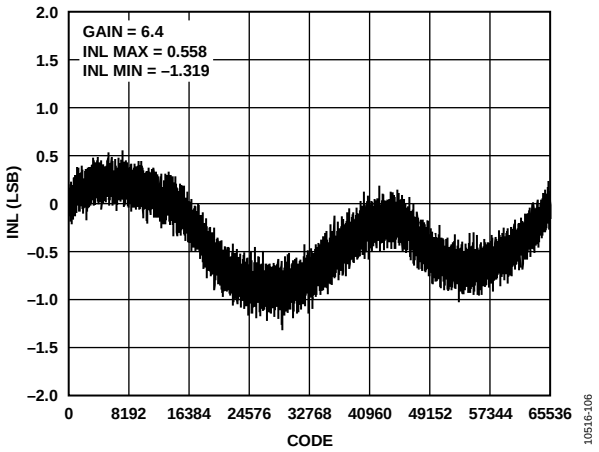


Figure 8. Integral Nonlinearity vs. Code, PGIA Gain = 6.4

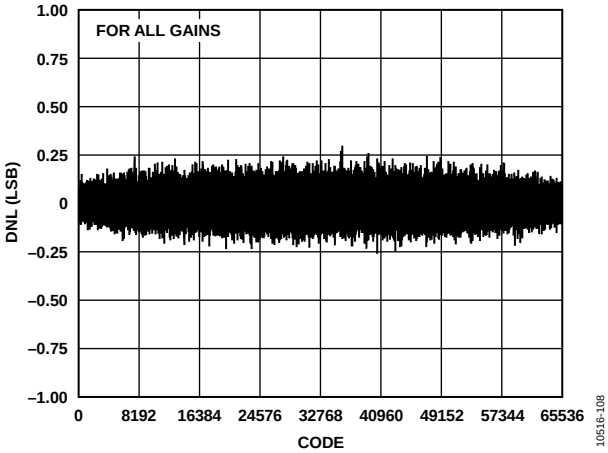


Figure 9. Differential Nonlinearity vs. Code for All PGIA Gains

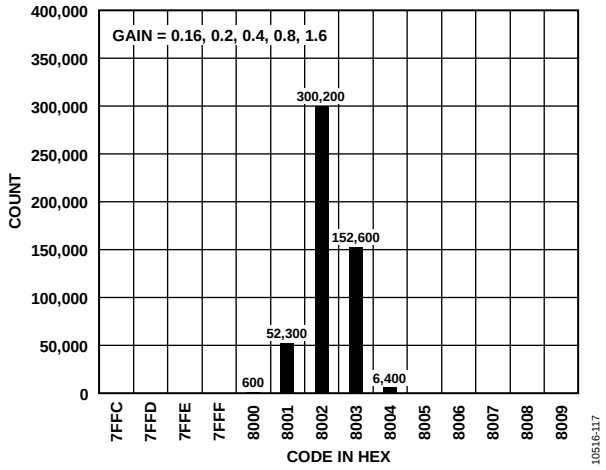


Figure 10. Histogram of a DC Input at Code Center, PGIA Gain = 0.16, 0.2, 0.4, 0.8, and 1.6

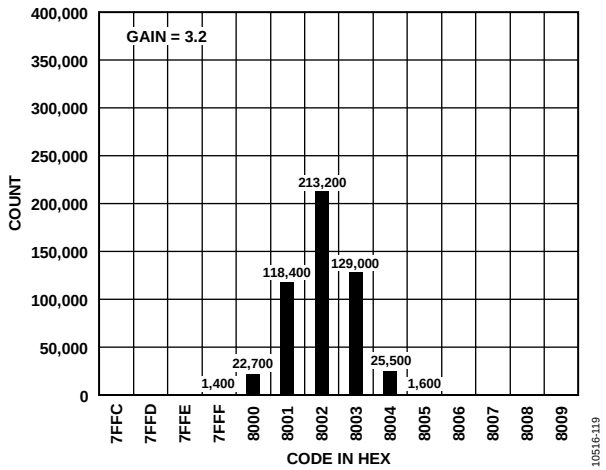


Figure 11. Histogram of a DC Input at Code Center, PGIA Gain = 3.2

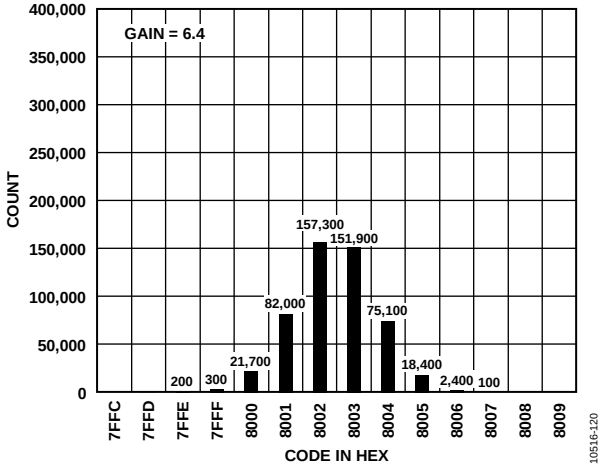


Figure 12. Histogram of a DC Input at Code Center, PGIA Gain = 6.4

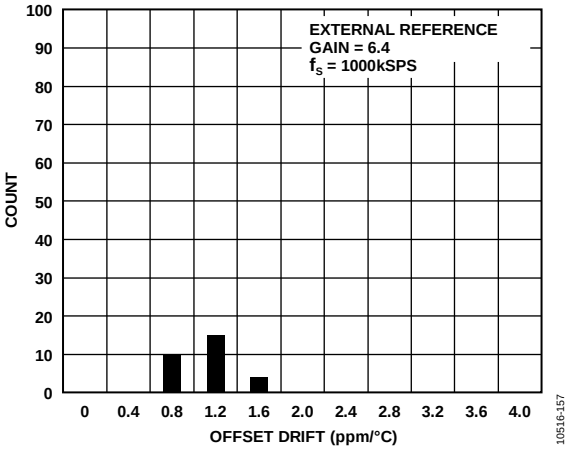


Figure 15. Offset Drift, PGIA Gain = 6.4

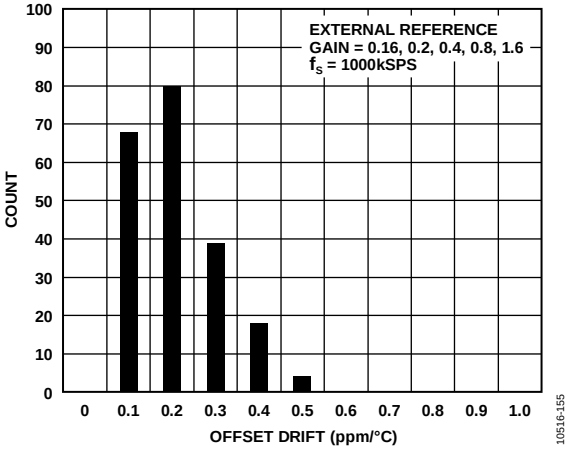


Figure 13. Offset Drift, PGIA Gain = 0.16, 0.2, 0.4, 0.8, and 1.6

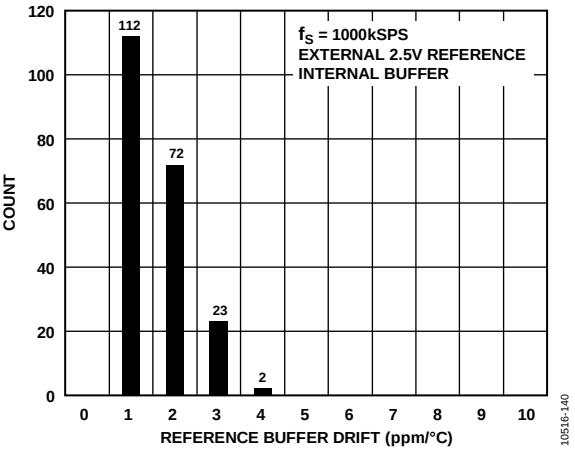


Figure 16. Reference Buffer Drift, External Reference

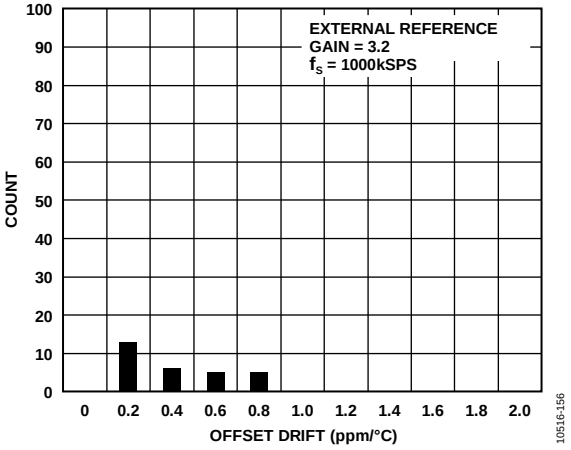


Figure 14. Offset Drift, PGIA Gain = 3.2

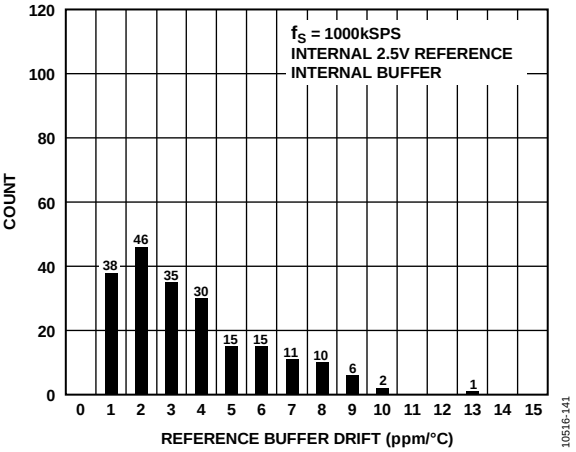


Figure 17. Reference Buffer Drift, Internal Reference

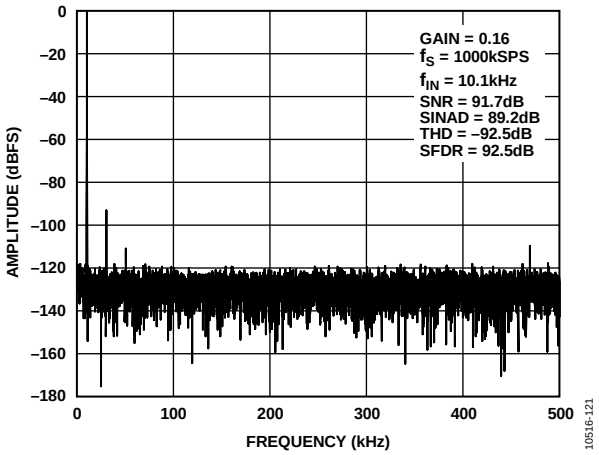


Figure 18. 10 kHz FFT, PGIA Gain = 0.16

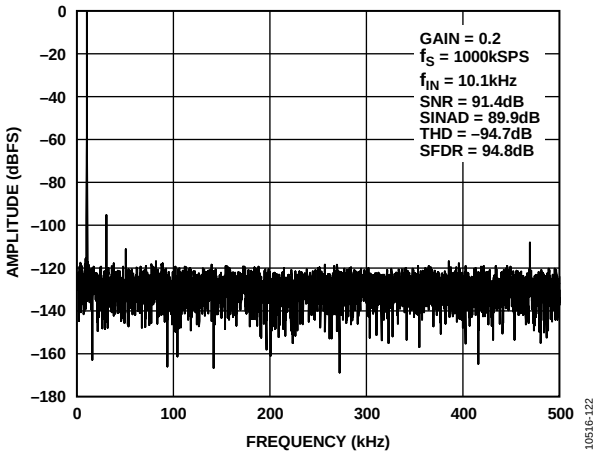


Figure 19. 10 kHz FFT, PGIA Gain = 0.2

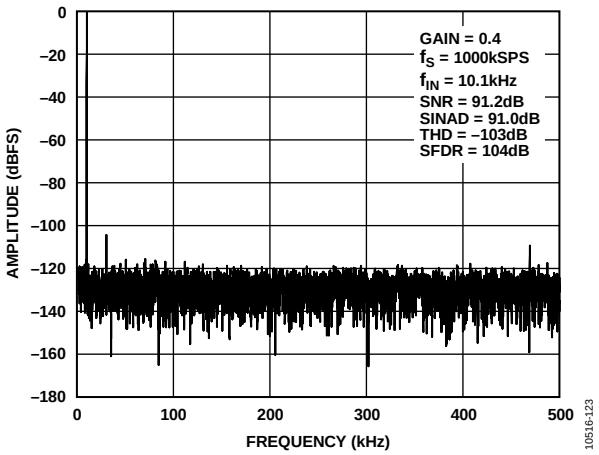


Figure 20. 10 kHz FFT, PGIA Gain = 0.4

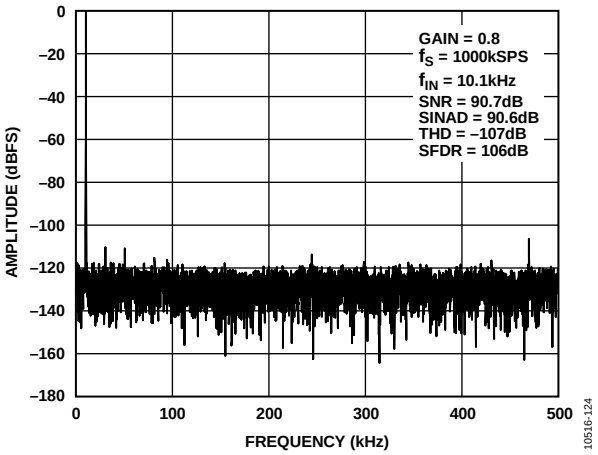


Figure 21. 10 kHz FFT, PGIA Gain = 0.8

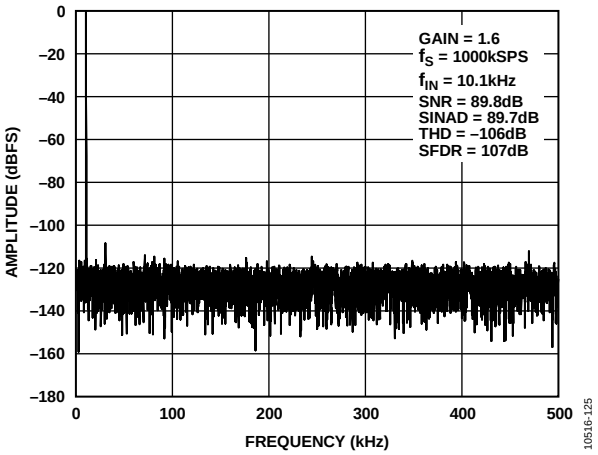


Figure 22. 10 kHz FFT, PGIA Gain = 1.6

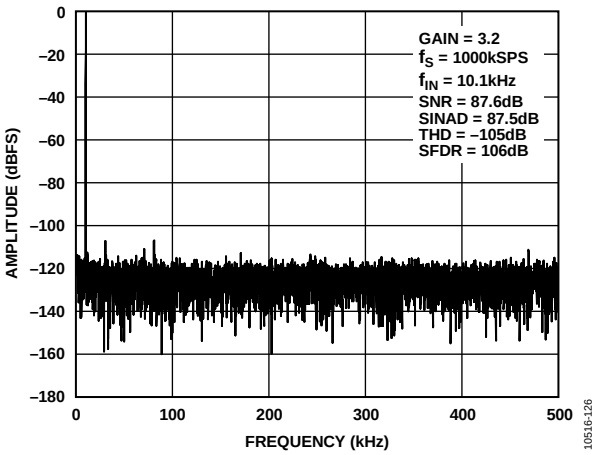


Figure 23. 10 kHz FFT, PGIA Gain = 3.2

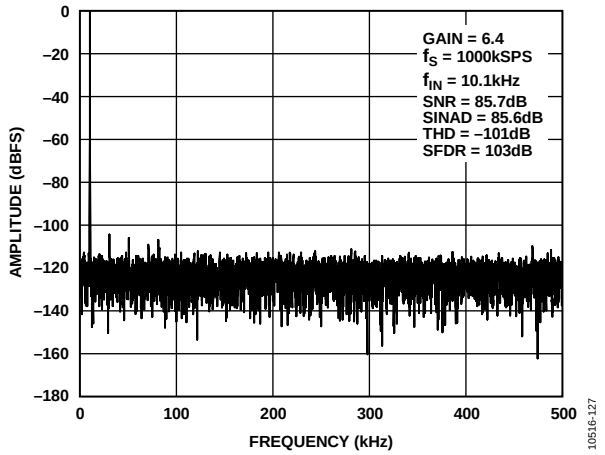


Figure 24. 10 kHz FFT, PGIA Gain = 6.4

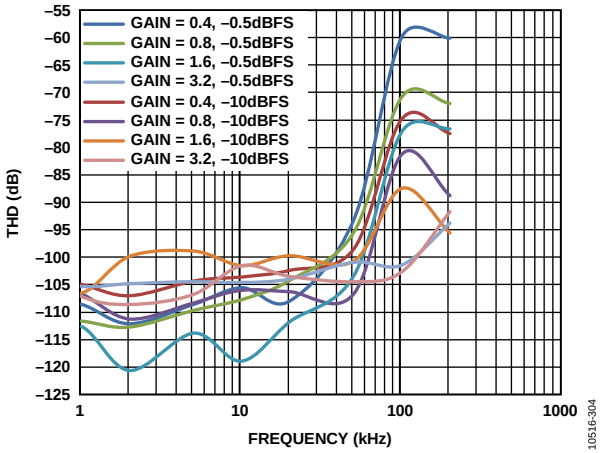


Figure 27. THD vs. Frequency

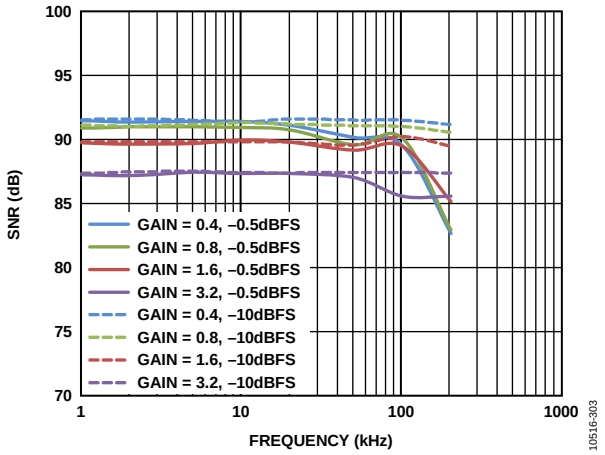


Figure 25. SNR vs. Frequency

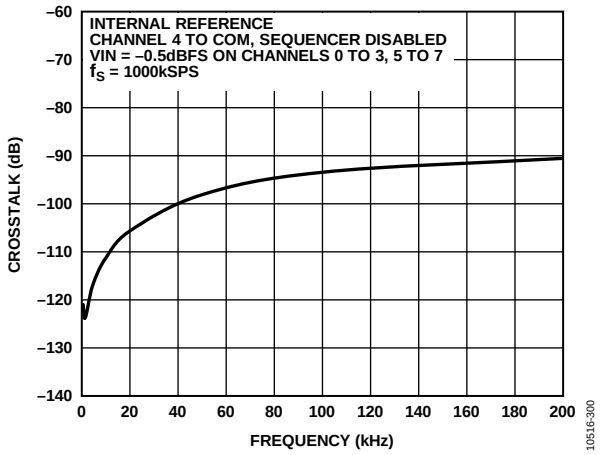


Figure 28. Crosstalk vs. Frequency

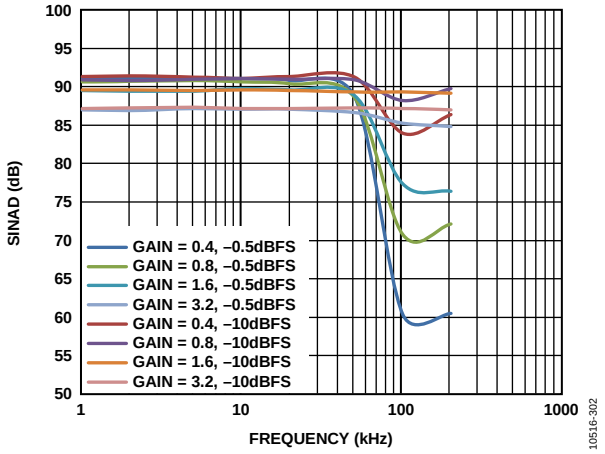


Figure 26. SINAD vs. Frequency

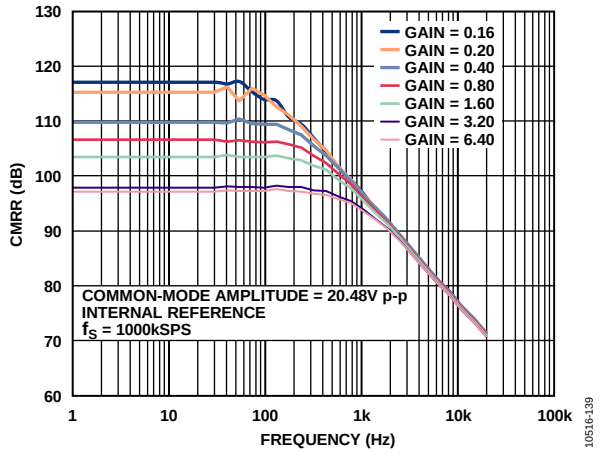


Figure 29. CMRR vs. Frequency

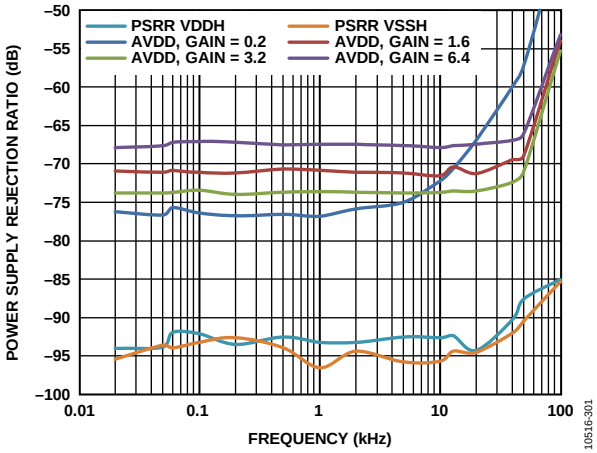


Figure 30. PSRR vs. Frequency

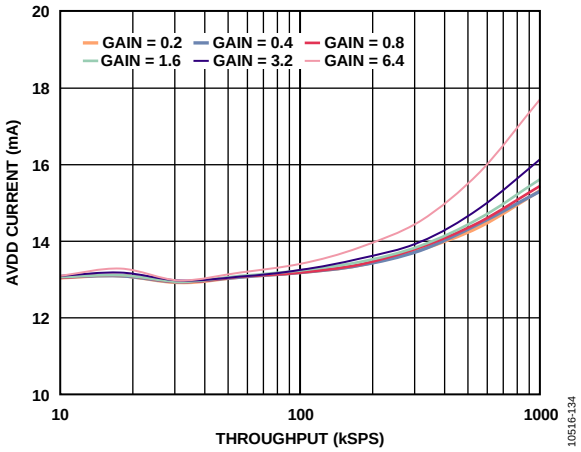


Figure 33. AVDD Current vs. Throughput, Internal Reference

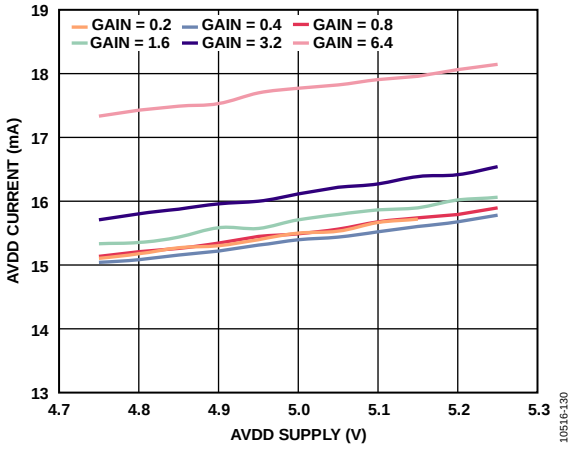


Figure 31. AVDD Current vs. Supply, Internal Reference

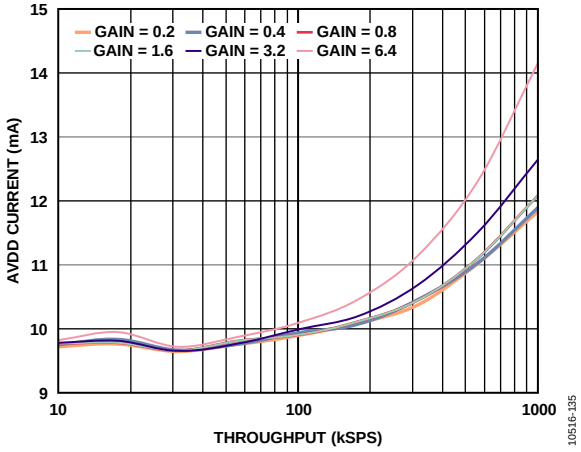


Figure 34. AVDD Current vs. Throughput, External Reference

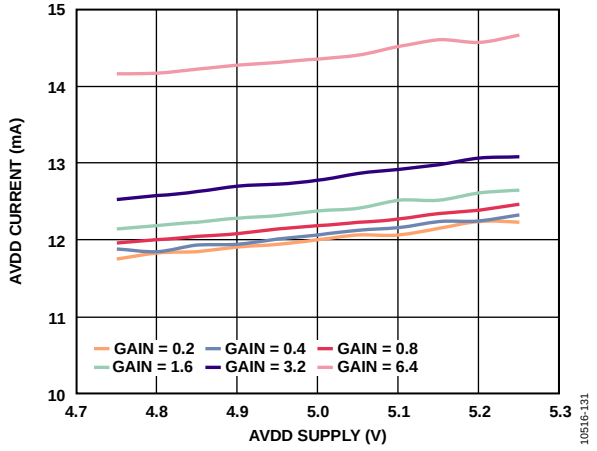


Figure 32. AVDD Current vs. Supply, External Reference

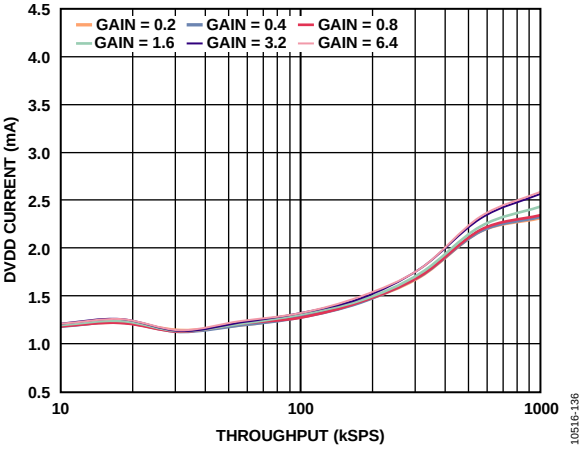


Figure 35. DVDD Current vs. Throughput

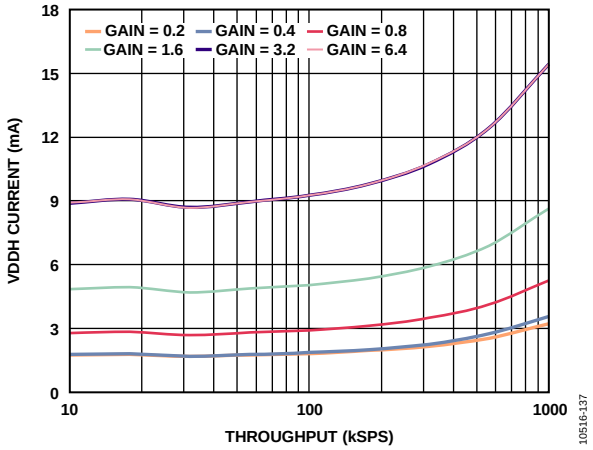


Figure 36. VDDH Current vs. Throughput

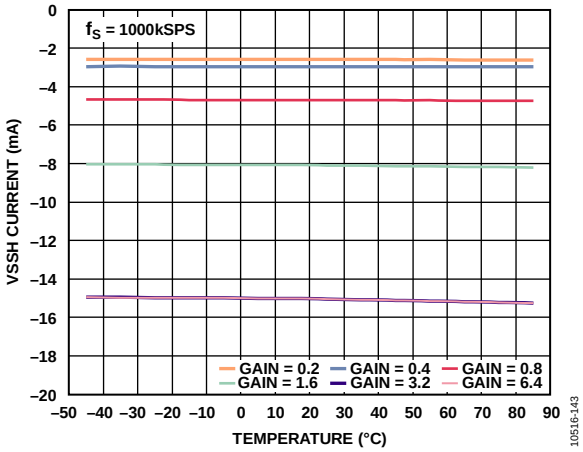


Figure 39. VSSH Current vs. Temperature

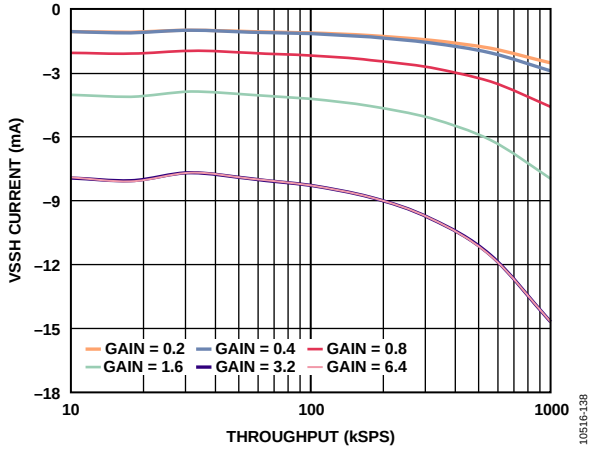


Figure 37. VSSH Current vs. Throughput

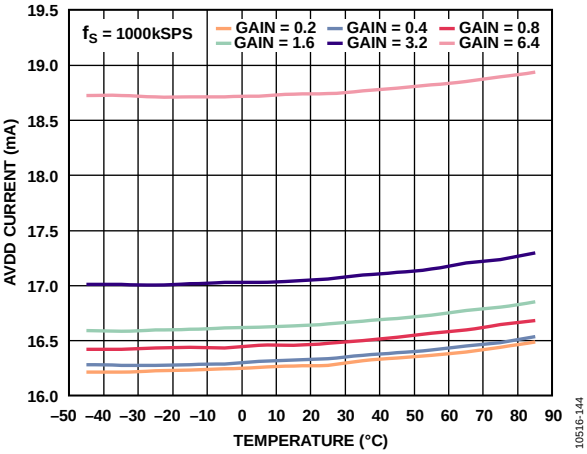


Figure 40. AVDD Current vs. Temperature

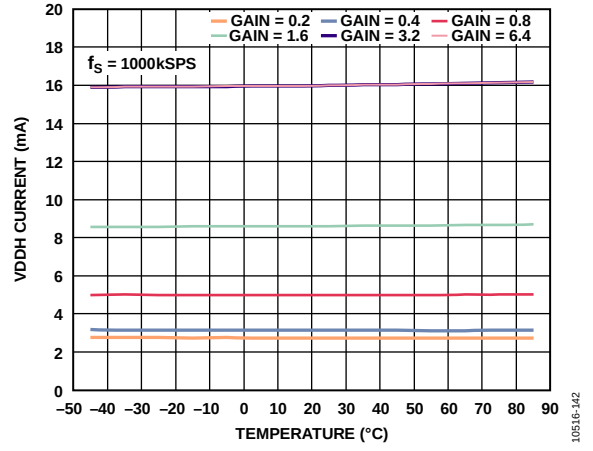


Figure 38. VDDH Current vs. Temperature

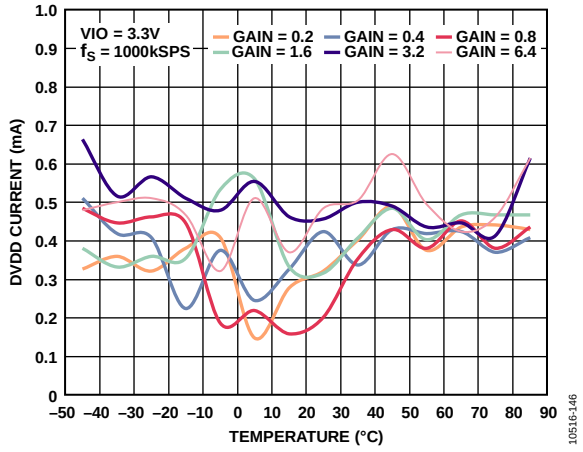


Figure 41. DVDD Current vs. Temperature

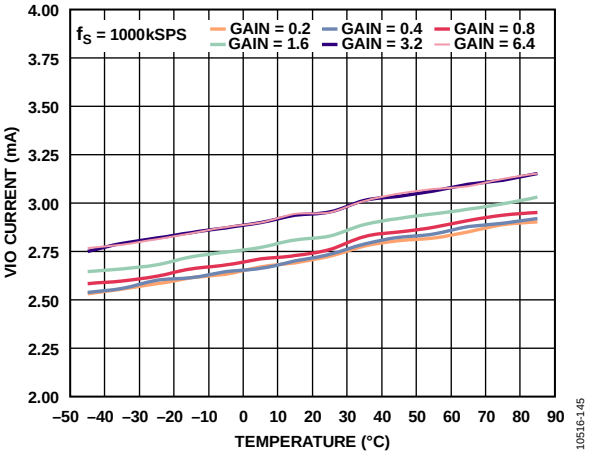


Figure 42. VIO Current vs. Temperature

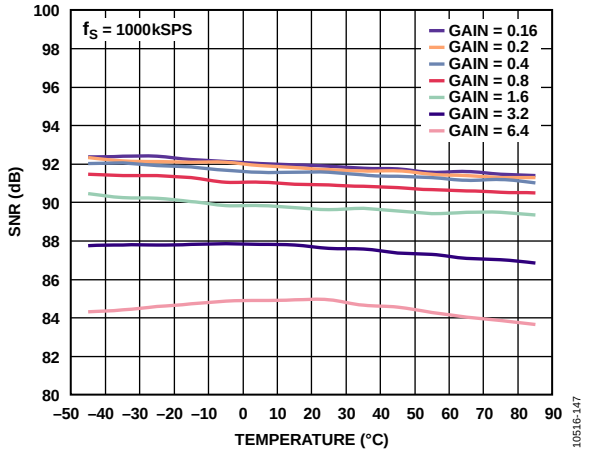


Figure 43. SNR vs. Temperature

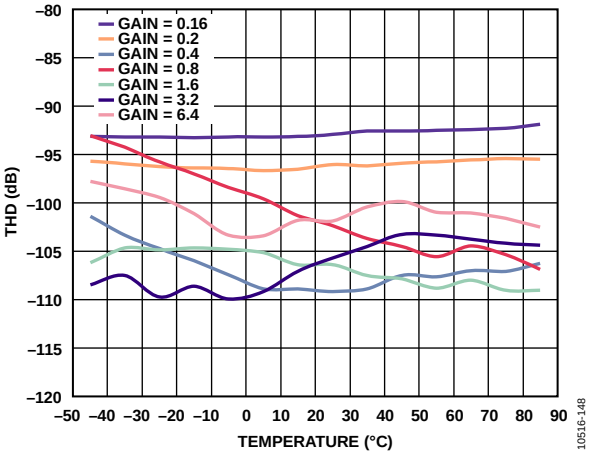


Figure 44. THD vs. Temperature

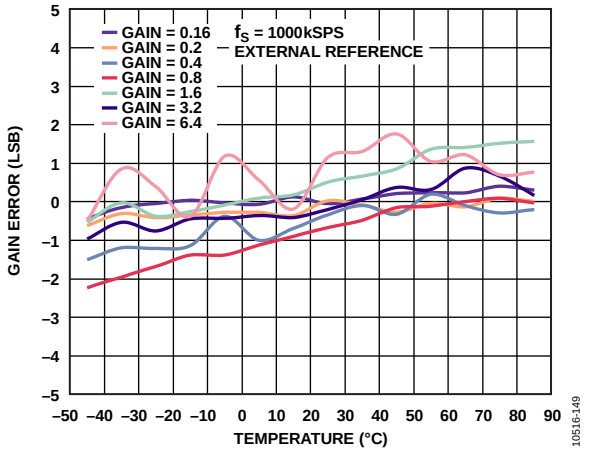


Figure 45. Gain Error vs. Temperature

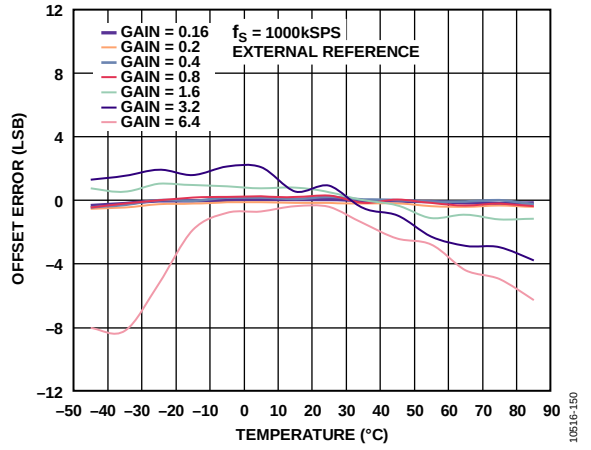


Figure 46. Offset Error vs. Temperature

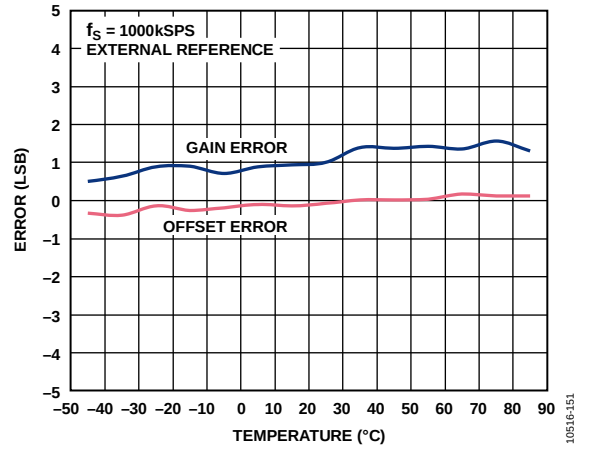


Figure 47. Offset and Gain Errors of the AUX ADC Channel Pair vs. Temperature

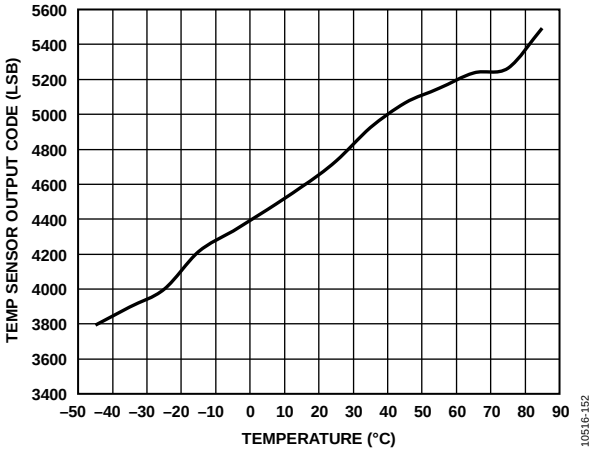


Figure 48. Temperature Sensor Output Code vs. Temperature

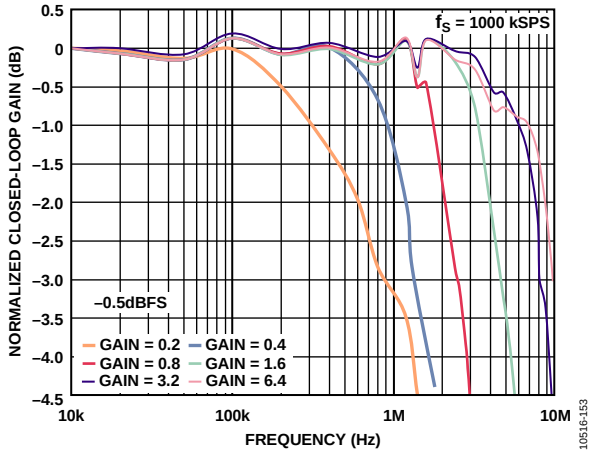


Figure 49. Large Signal Frequency Response vs. Gain

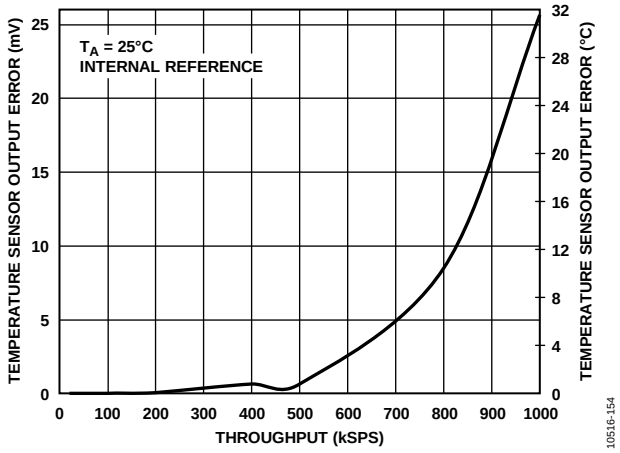


Figure 50. Temperature Sensor Output Error vs. Throughput

TERMINOLOGY

Operating Input Voltage Range
Operating input voltage range is the maximum input voltage range, including the common-mode voltage, allowed on the input channels IN[7:0] and COM.

Differential Input Voltage Range
Differential input voltage range is the maximum differential full-scale input range. The value changes according to the programmable gain setting.

Channel Off Leakage
Channel off leakage is the leakage current with the channel off.

Channel On Leakage
Channel on leakage is the leakage current with the channel on.

Charge Injection
Charge injection is a measure of the glitch impulse that is transferred through the analog input pin into the source when the sample is taken and/or the multiplexer is switched.

Common-Mode Rejection Ratio (CMRR)
CMRR is the ratio of the amplitude of a signal referred to input in the converted result to the amplitude of the modulation common to a pair of inputs and is expressed in decibels. CMRR is a measure of the ability of the ADAS3022 to reject signals, such as power line noise, that are common to the inputs. This specification is for a 2 kHz sine wave of 20.48 V p-p applied to both channels of an input pair.

Transient Response
Transient response is a measure of the time required for the ADAS3022 to properly acquire the input after a full-scale step function is applied to the system.

Least Significant Bit (LSB)
LSB is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\,(\mathrm{V}) = \frac{2V_{REF}}{2^N}$$

Integral Nonlinearity (INL) Error
INL refers to the deviation of each individual code from a line drawn from negative full scale to positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 53).

Differential Nonlinearity (DNL) Error
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error
Offset error is the deviation of the actual MSB transition from the ideal MSB transition point. The ideal MSB transition occurs at an input level ½ LSB above analog ground.

Gain Error
The last transition (from 111 … 10 to 111 … 11) for an analog voltage should occur 1½ LSB below the nominal full scale. The gain error is the deviation expressed in LSB (or as a percentage of the full-scale range) of the actual level of the last transition from the ideal level after the offset error is removed. Closely related to this parameter is the full-scale error (also expressed in LSB or as a percentage of the full-scale range), which includes the effects of the offset error.

Total Unadjusted Error (TUE)
TUE is the deviation of each code from an ideal transfer function and is a combination of all error contributors, including non-linearity, offset error, and gain error. TUE for the ADAS3022 is expressed as the maximum deviation in LSB or as a percentage of the full-scale range.

Aperture Delay
Aperture delay is a measure of the acquisition performance. It is the time between the rising edge of the CNV input and the point at which the input signal is held for a conversion.

Dynamic Range
Dynamic range is the ratio of the rms value of the full-scale signal to the total rms noise measured with the inputs shorted together. The value for the dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, expressed in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Channel-to-Channel Crosstalk
Channel-to-channel crosstalk is a measure of the level of crosstalk between any channel and all other channels. The crosstalk is measured by applying a dc input to the channel under test and applying a full-scale, 10 kHz sine wave signal to all other channels. The crosstalk is the amount of signal that leaks into the test channel and is expressed in decibels.

Reference Voltage Temperature Coefficient
Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T (25°C), and T_{MAX}. The value is expressed in ppm/°C as

$$TCV_{REF}\,(\text{ppm/°C}) = \frac{V_{REF}\,(Max) - V_{REF}\,(Min)}{V_{REF}\,(25°C) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}\,(Max)$ is the maximum reference output voltage at T_{MIN}, T (25°C), or T_{MAX}.
$V_{REF}\,(Min)$ is the minimum reference output voltage at T_{MIN}, T (25°C), or T_{MAX}.
$V_{REF}\,(25°C)$ is the reference output voltage at 25°C.
T_{MAX} = +85°C.
T_{MIN} = −40°C.

THEORY OF OPERATION

OVERVIEW

The ADAS3022 is the first system on a single chip that integrates the typical components used in a data acquisition system in one easy to use, programmable device. This single-chip solution is capable of converting up to 1,000,000 samples per second (1 MSPS) of aggregate throughput. The ADAS3022 features

- High impedance inputs
- High common-mode rejection
- 8-channel, low crosstalk multiplexer (mux)
- Programmable gain instrumentation amplifier (PGIA) with seven selectable differential input ranges from ±0.64 V to ±24.576 V
- 16-bit PulSAR® ADC with no missing codes
- Internal, precision, low drift 4.096 V reference and buffer
- Temperature sensor
- Channel sequencer

The ADAS3022 uses an Analog Devices patented high voltage *i*CMOS® process, allowing up to a ±24.576 V differential input voltage range when using ±15 V supplies, which makes the device suitable for industrial applications.

The device is housed in a small, 6 mm × 6 mm, 40-lead LFCSP and can operate over the industrial temperature range (−40°C to +85°C). A typical discrete multichannel data acquisition system containing similar circuitry would require at least three times more space on the circuit board. Therefore, advantages of the ADAS3022 solution include reduced footprint and less complex design requirements, which also results in faster time to market and lower cost.

ADAS3022 OPERATION

As shown in Figure 51, the ADAS3022 internal analog circuitry consists of a high impedance, low leakage multiplexer and a programmable gain instrumentation amplifier that can accept full-scale differential voltages of ±0.64 V, ±1.28 V, ±2.56 V, ±5.12 V, ±10.24 V, ±20.48 V, and ±24.576 V. The ADAS3022 can be configured to use up to eight single-ended input channels or four pairs of channels, that is, 125 kSPS per channel for eight channels or effectively 250 kSPS for four channel pairs. The device can also provide a relative temperature measurement using the internal temperature sensor. In addition, the differential auxiliary channel pair (AUX+ and AUX−) is provided with the specified input range of $\pm V_{REF}$. This option bypasses the mux and PGIA stages, allowing direct access to the SAR ADC core.

Reducing the number of channels or pairs increases the throughput rate by an amount proportional to the reciprocal of the number of sampled channels multiplied by the aggregate throughput:

1/(*Number of Channels or Pairs*) × 1000 kSPS

For a single channel or channel pair, the maximum throughput rate is 1 MSPS. For all eight channels, the AUX channel pair, and the temperature sensor, the throughput rate of a given channel decreases to 100 kSPS.

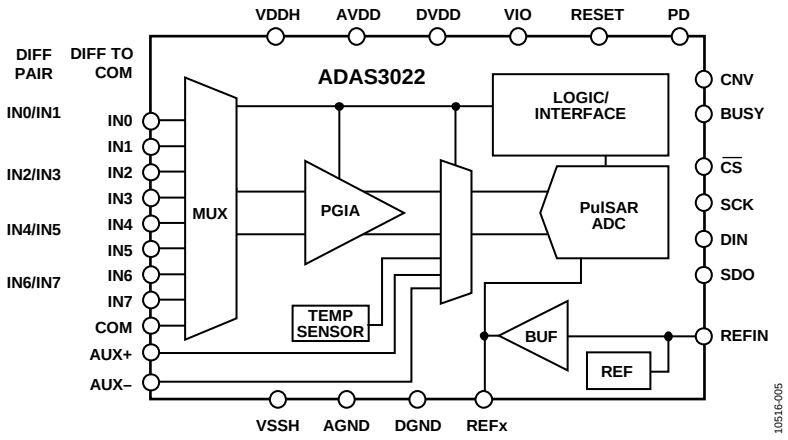


Figure 51. ADAS3022 Simplified Block Diagram

The ADAS3022 offers true high impedance inputs in a differential structure and rejects common-mode signals present on the inputs. The ADAS3022 architecture does not require any of the additional input buffers (op amps) that are usually required to condition the input signal and drive the ADC inputs when using switched capacitor-based successive approximation register (SAR) analog-to-digital converters (ADCs).

The inputs are multiplexed to the PGIA using a high voltage multiplexer with low charge injection and very low leakage. The inputs can be configured for a single-ended to common point (COM) measurement or can be paired for up to four fully differential inputs with independent gain settings. This requires using the advanced sequencer or programming sequential configuration words with the desired gain for each pair. The digitally controlled, programmable gain is used to select one of seven voltage input ranges (see Table 7).

When the sequencer option is used, an on-chip sequencer scans channels in order and offers independent input voltage ranges for each channel (see the On Demand Conversion Mode section). In this mode, a single configuration word initiates the sequencer to scan repeatedly without the need to rewrite the register. After the last channel is scanned, the ADAS3022 automatically begins at IN0 again and repeats the sequence until a word is written to stop the sequencer or the asynchronous RESET is asserted. Additionally, if changes are made to certain configuration bits, the sequencer is reset to IN0.

The PulSAR-based ADC core is capable of converting 1 MSPS from a single rising edge on the convert start input (CNV). The conversion results are available in twos complement format and are presented on the serial data output (SDO). The digital interface uses a dedicated chip select pin ($\overline{CS}$) to transfer data to and from the ADAS3022 and also provides a BUSY indicator, asynchronous RESET, and power-down (PD) inputs.

The ADAS3022 on-chip reference uses an internal temperature compensated 2.5 V output band gap reference and a precision buffer amplifier to provide the 4.096 V high precision system reference.

All of the bits in Table 11 are configured through a serial (SPI-compatible), 16-bit configuration register (CFG). Configuration and conversion results can be read after or during a conversion, or the readback option can be disabled.

The ADAS3022 requires a minimum of three power supplies: +5 V, +15 V, and −15 V. On-chip low dropout regulators provide the necessary 2.5 V system voltages and must be decoupled externally via dedicated pins (ACAP, DCAP, and RCAP). The ADAS3022 can be interfaced to any 1.8 V to 5 V digital logic family using the dedicated VIO logic level voltage supply (see Table 9).

A rising edge on CNV initiates a conversion and changes the state of the ADAS3022 from track to hold. In this state, the ADAS3022 performs analog signal conditioning. When the signal conditioning is complete, the ADAS3022 returns to the track state while at the same time quantizing the sample. This two-part process satisfies the necessary settling time requirement while achieving a fast throughput rate of up to 1 MSPS with 16-bit accuracy.

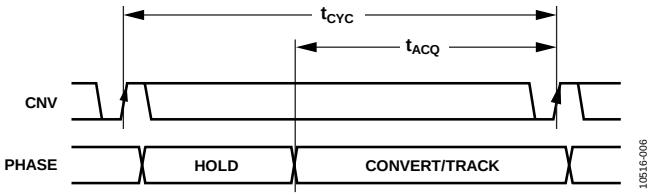


Figure 52. ADAS3022 System Timing

Regardless of the type of signal (differential or single-ended, antiphase or nonantiphase, symmetric or asymmetric), the ADAS3022 converts all signals present on the enabled inputs in a differential fashion, like an industry-standard difference or instrumentation amplifier.

The conversion result is available after the conversion is complete and can be read back at any time before the end of the next conversion. Reading back data should be avoided during the quiet period, as indicated by BUSY being active high. Because the ADAS3022 has an on-board conversion clock, the serial clock (SCK) is not required for the conversion process. It is only required to present results to the user.

TRANSFER FUNCTION

The ideal transfer characteristics of the ADAS3022 are shown in Figure 53. With the inputs configured for differential input ranges, the data output is twos complement, as described in Table 6.

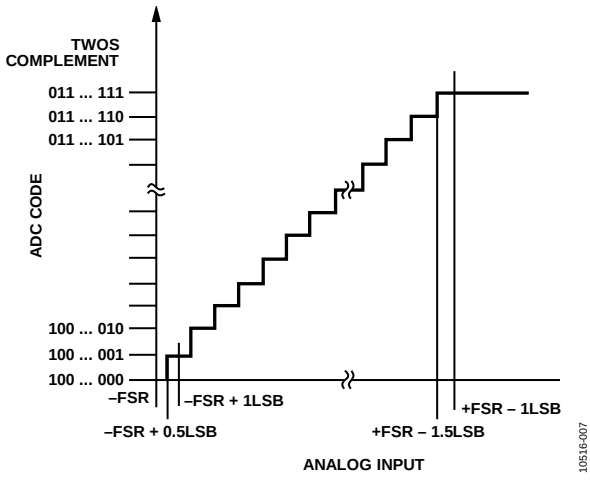


Figure 53. ADC Ideal Transfer Function

Table 6. Output Codes and Ideal Input Voltages

Description	Differential Analog Inputs, V_{REF} = 4.096 V	Digital Output Code (Twos Complement, Hex)
FSR – 1 LSB	(32,767 × V_{REF})/(32,768 × PGIA gain)	0x7FFF
Midscale + 1 LSB	V_{REF}/(32,768 × PGIA gain)	0x0001
Midscale	0	0x0000
Midscale – 1 LSB	–(V_{REF}/(32,768 × PGIA gain))	0xFFFF
–FSR + 1 LSB	–(32,767 × V_{REF})/(32,768 × PGIA gain)	0x8001
–FSR	–V_{REF} × PGIA gain	0x8000

TYPICAL APPLICATION CONNECTION DIAGRAM

As shown in Figure 54, the ADP1613 is used in an inexpensive SEPIC-Ćuk topology, which is an ideal candidate for providing the ADAS3022 with the necessary high voltage ±15 V robust supplies (at 20 mA) and low output ripple (3 mV maximum) from an external 5 V supply. The ADP1613 satisfies the specification requirements of the ADAS3022 with minimal external components while achieving greater than 86% of efficiency. Refer to the CN-0201 circuit note for complete information about this test setup.

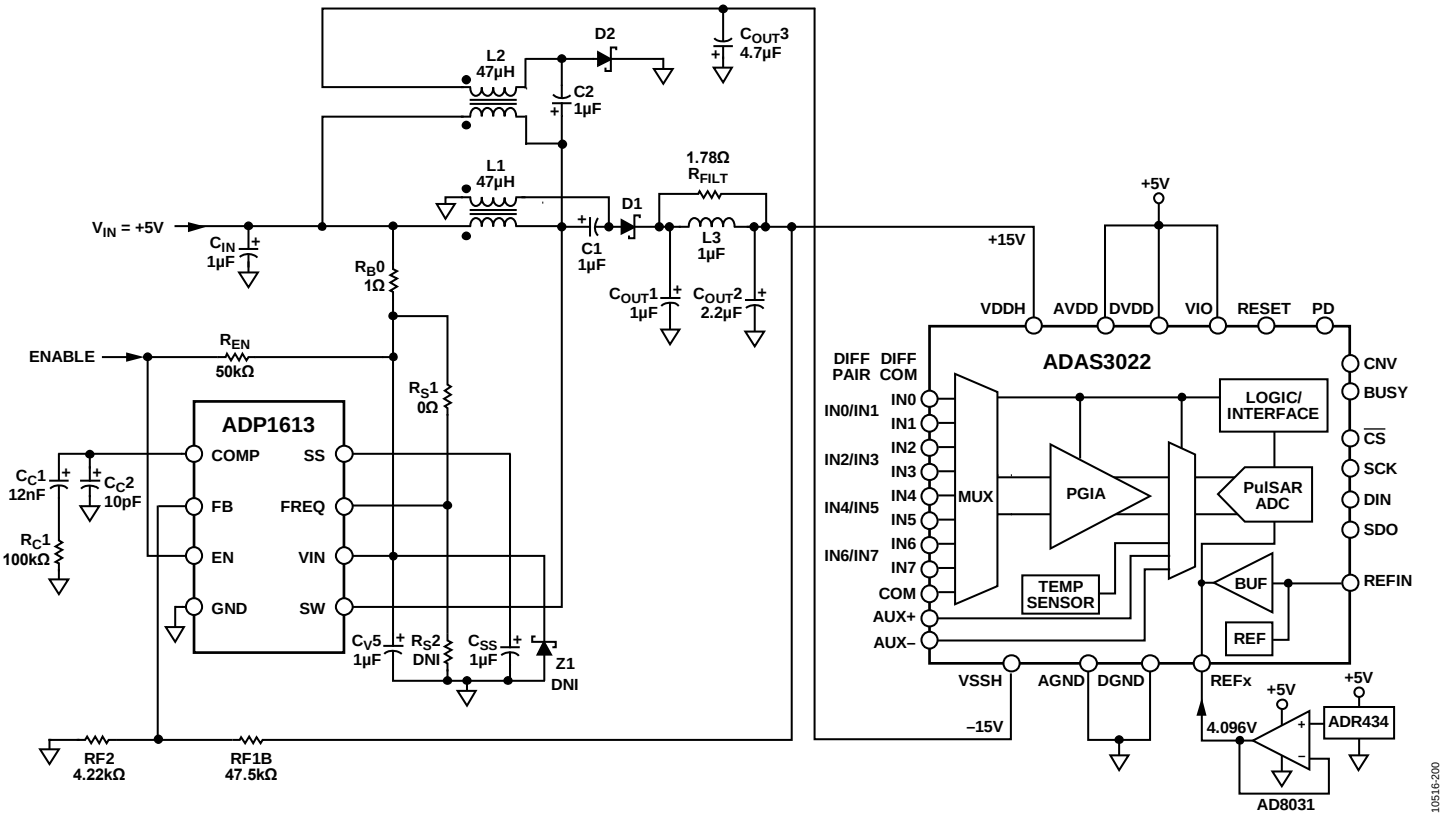


Figure 54. Complete 5 V, Single-Supply, 8-Channel Multiplexed Data Acquisition System with PGIA

ANALOG INPUTS

Input Structure

The ADAS3022 uses a differential input structure between IN[7:0] and COM or between IN[7:0]+ and IN[7:0]− of a channel pair. The COM input is sampled identically such that the same voltages can be present on inputs IN[7:0]. Therefore, the selection of paired channels or all channels referenced to one common point is available. Because all inputs are sampled differentially, the ADAS3022 offers true high common-mode rejection, whereas a discrete system would require the use of additional instrumentation or a difference amplifier.

Figure 55 shows an equivalent circuit of the analog inputs. The internal diodes provide ESD protection for the analog inputs (IN[7:0] and COM) from the high voltage supplies (VDDH and VSSH). Care must be taken to ensure that the analog input signal does not exceed the supply rails by more than 0.3 V because this can cause the diodes to become forward-biased and to start conducting current. Note that if the auxiliary input pair (AUX±) is used, the diodes provide ESD protection from only the lower voltage AVDD (5 V) supply and the system analog ground because these inputs are connected directly to the internal SAR ADC circuitry.

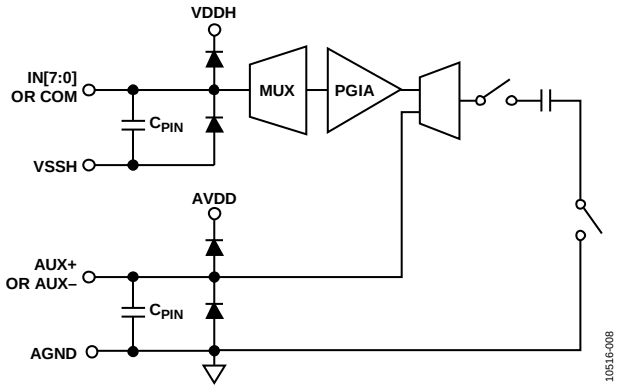


Figure 55. Equivalent Analog Input Circuit

Voltages beyond the absolute maximum ratings may cause permanent damage to the ADAS3022 (see Table 4).

Programmable Gain

The ADAS3022 incorporates a programmable gain instrumentation amplifier with seven selectable ranges (±0.64 V, ±1.28 V, ±2.56 V, ±5.12 V, ±10.24 V, ±20.48 V, and ±24.576 V), enabling the use of almost any direct sensor interface. The PGIA settings are specified in terms of the maximum absolute differential input voltage across a pair of inputs (for example, INx+ to INx− or INx+ to COM). The power-on and default conditions are preset to the ±20.48 V (PGIA = 111) input range.

Note that because the ADAS3022 can use any input type, such as bipolar differential (antiphase or nonantiphase), bipolar single ended, or pseudo bipolar, setting the PGIA is important to make full use of the allowable input span.

Table 7 describes each differential input range and the corresponding LSB size, PGIA bits settings, and PGIA gain.

Table 7. Differential Input Ranges, LSB Size, and PGIA Settings

Differential Input Ranges, INx+ − INx− (V)	LSB (µV)	PGIA Bits	PGIA Gain (V/V)
±24.576	750	000	0.16
±20.48	625	111	0.2
±10.24	312.5	001	0.4
±5.12	156.3	010	0.8
±2.56	78.13	011	1.6
±1.28	39.06	100	3.2
±0.64	19.53	101	6.4

Common-Mode Operating Range

The differential input common-mode voltage (V_{CM}) range changes according to the maximum input range selected and the high voltage power supplies (VDDH and VSSH). Note that the specified operating input voltage of any input pin (see the Specifications section) requires 2.5 V of headroom from the VDDH and VSSH supplies; therefore,

$$(VSSH + 2.5\ V) \leq INx/COM \leq (VDDH - 2.5\ V)$$

This section provides some examples of setting the PGIA for various input signals. Note that the ADAS3022 always calculates the difference between the IN+ and IN− signals.

Fully Differential, Antiphase Signals with a Zero Common Mode

For a pair of 20.48 V p-p differential antiphase signals with a zero common mode, the maximum differential voltage across the inputs is ±20.48 V, and the PGIA gain configuration should be set to 111.

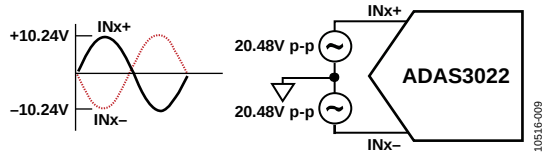


Figure 56. Differential, Antiphase Inputs with a Zero Common Mode

Fully Differential, Antiphase Signals with a Nonzero Common Mode

For a pair of 5.12 V p-p differential antiphase signals with a nonzero common mode (dc common-mode voltage of 7 V in this example), the maximum differential voltage across the inputs is ±5.12 V (dc common-mode voltage is rejected), and the PGIA gain configuration should be set to 010.

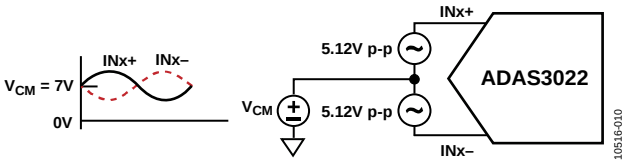


Figure 57. Differential, Antiphase Inputs with a Nonzero Common Mode

Differential, Nonantiphase Signals with a Zero Common Mode

For a pair of 10.24 V p-p differential nonantiphase signals with a zero common mode, the maximum differential voltage across the inputs is ±10.24 V, and the PGIA gain configuration should be set to 001.

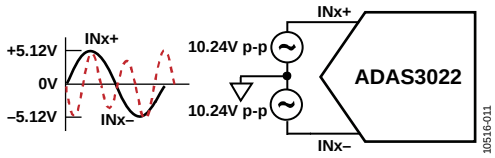


Figure 58. Differential, Nonantiphase Inputs with a Zero Common Mode

Single-Ended Signals with a Nonzero DC Offset (Asymmetrical)

When a 12 V p-p signal with a 6 V dc level-shift is connected to one input (INx+) and the dc ground sense of the signal is connected to INx– or COM, the PGIA gain configuration is set to 000 for the ±24.576 V range because the maximum differential voltage across the inputs is 12 V p-p and only half the codes available for the transfer function are used.

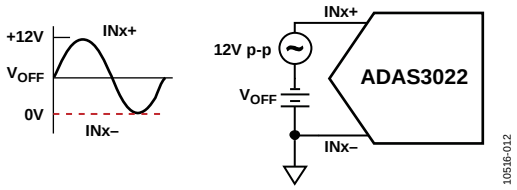


Figure 59. Typical Single-Ended Unipolar Input—Uses Only Half the Codes

Single-Ended Signals with a 0 V DC Offset (Symmetrical)

Compared with the example in the Single-Ended Signals with a Nonzero DC Offset (Asymmetrical) section, a better solution for single-ended signals, if possible, is to remove as much dc offset as possible between INx+ and INx– to produce a bipolar input voltage that is symmetric around the ground sense. In this example, the differential voltage across the inputs is never greater than ±0.64 V, and the PGIA gain configuration is set to 101 for the 1.28 V p-p range. This scenario uses all of the codes available for the transfer function, making full use of the allowable differential input range.

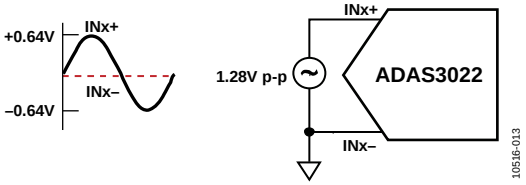


Figure 60. Better Single-Ended Configuration—Uses All Codes

Notice that the voltages in this example are not integer values due to the 4.096 V reference and the PGIA scaling ratios.

Multiplexer

The ADAS3022 uses a high voltage, high performance, low charge injection multiplexer and a total of nine inputs (IN[7:0] and COM). Using the INx and COM bits of the configuration register, the ADAS3022 is configurable for differential inputs between any of the eight input channels (IN[7:0]) and COM or for up to four input pairs. Figure 61 shows various methods for configuring the analog inputs for the type of channel (single or paired). Refer to the Configuration Register section for more information.

The analog inputs can be configured as follows:

- Figure 61A: IN[7:0] referenced to a system ground.
- Figure 61B: IN[7:0] with a common reference point.
- Figure 61C: IN[7:0] differential pairs. For pairs, COM = 0. The positive channel is configured with INx. If INx is even, then IN0, IN2, IN4, and IN6 are used. If INx is odd, then IN1, IN3, IN5, and IN7 are used, as indicated by the channels with parentheses in Figure 61C. For example, for the IN0/IN1 pair with the positive channel on IN0, INx = 000_2. For the IN4/IN5 pair with the positive channel on IN5, INx = 101_2. Note that when the channel sequencer is used, as detailed in the On Demand Conversion Mode section, the positive channels are always IN0, IN2, IN4, and IN6.
- Figure 61D: inputs configured in a combination of any of the preceding configurations (showing that the ADAS3022 can be configured dynamically).

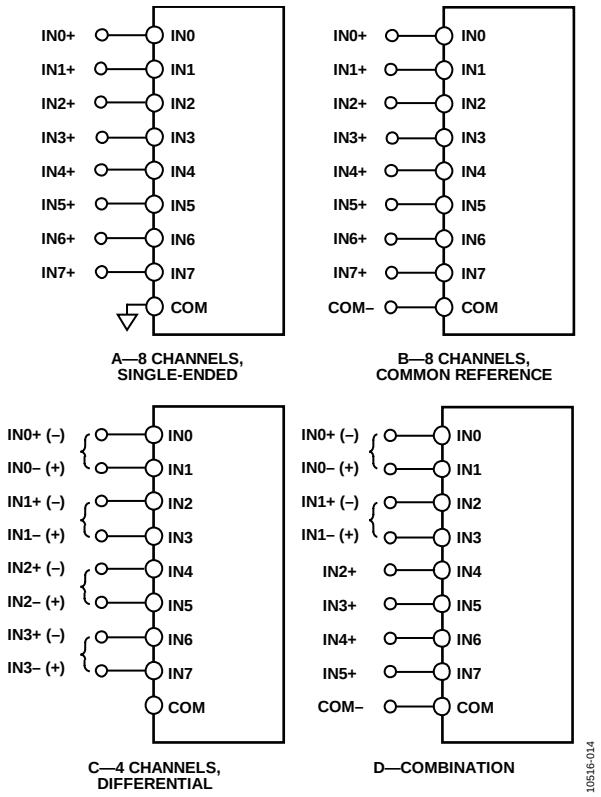


Figure 61. Multiplexed Analog Input Configurations

Channel Sequencer

The ADAS3022 includes a channel sequencer that is useful for scanning channels in a repeated fashion. Refer to the On Demand Conversion Mode section for more information.

Auxiliary Input Channel

The ADAS3022 includes an auxiliary input channel pair (AUX+ and AUX–) that bypasses the mux and PGIA stages, allowing direct access to the SAR ADC core for applications where the additional dedicated channel pair is required. As detailed previously, the inputs are protected only from AVDD and AGND because the high voltage supplies are used for the mux and PGIA stages but not the lower voltage ADC core.

When the source impedance of the driving circuit is low, the AUX± inputs can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performance parameters are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

Driver Amplifier Choice

For systems that cannot drive AUX± directly, a suitable op amp buffer should be used to preserve the ADAS3022 performance. The driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and the transition noise performance of the ADAS3022. The noise from the amplifier is filtered by the ADAS3022 analog input circuit or by an external filter, if one is used. Because the typical noise of the ADAS3022's SAR ADC core is 35 µV rms (V_{REF} = 4.096 V), the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{35}{\sqrt{35^2 + \frac{\pi}{2} f_{-3dB}(Ne_N)^2}}\right)$$

  where:
  f_{-3dB} is the input bandwidth (8 MHz) of the ADAS3022's SAR ADC core expressed in megahertz or the cutoff frequency of an input filter, if one is used.
  N is the noise gain of the amplifier (for example, 1 in buffer configuration).
  e_N is the equivalent input noise voltage of the op amp expressed in nV/√Hz.
- For ac applications, the driver should have a THD performance commensurate with the ADAS3022.
- The analog input circuit must settle a full-scale step onto the capacitor array at a 16-bit level (0.0015%). In amplifier data sheets, settling at 0.1% to 0.01% is more commonly specified. This may differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection.

Table 8. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4841-1, ADA4841-2	Very low noise, small, and low power
ADA4897-1, ADA4897-2	Very low noise, low and high frequencies
AD8655	5 V single supply, low noise
AD8021, AD8022	Very low noise and high frequency
OP184	Low power, low noise, and low frequency
AD8605, AD8615	5 V single supply, low power

VOLTAGE REFERENCE OUTPUT/INPUT

The ADAS3022 allows the choice of an internal reference or an external reference using the on-chip buffer/amplifier, or an external reference.

The internal reference of the ADAS3022 provides excellent performance and can be used in almost all applications. To set the reference selection mode, use the internal reference enable bit (REFEN) and the REFIN pin as described in this section. REF1 and REF2 must be tied together externally.

Internal Reference

The precision internal reference is factory trimmed and is suitable for most applications.

Setting the REFEN bit in the CFG register to 1 (default) enables the internal reference and produces 4.096 V on the REF1 and REF2 pins; this 4.096 V output serves as the main system reference. The unbuffered 2.5 V (typical) band gap voltage is output on the REFIN pin, which requires an external parallel decoupling using 10 µF and 0.1 µF capacitors to reduce the noise on the output. Because the current output of REFIN is limited, it can be used as a source if followed by a suitable buffer, such as the AD8031. Note that excessive loading of the REFIN output will also lower the 4.096 V system reference because the internal amplifier uses a fixed gain.

The internal reference output is trimmed to the targeted value of 4.096 V with an initial accuracy of ±8 mV. The reference is also temperature compensated to provide a typical drift of ±5 ppm/°C.

When the internal reference is used, the ADAS3022 should be decoupled as shown in Figure 62. Note that both REF1 and REF2 connections are required, along with suitable decoupling on the REFIN output and the RCAP internally regulated supply.

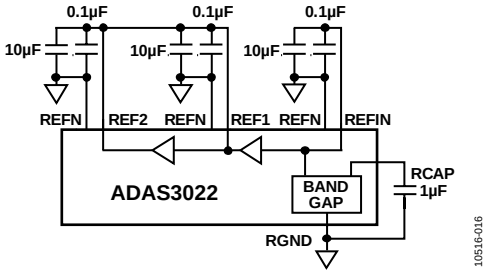


Figure 62. 4.096 V Internal Reference Connection

External Reference and Internal Buffer

The external reference and internal buffer are useful when a common system reference is used or if improved drift performance is required.

Setting REFEN to 0 disables the internal band gap reference, allowing the user to provide an external voltage reference (2.5 V typical) to the REFIN pin. The internal buffer remains enabled, thus reducing the need for an external buffer amplifier to generate the main system reference. With REFIN = 2.5 V, REF1 and REF2 output 4.096 V, which serves as the main system reference.

For this configuration, connect the external source as shown in Figure 63. Any type of 2.5 V reference, including those with low power, low drift, and a small package, can be used in this configuration because the internal buffer handles the dynamics of the ADAS3022 reference.

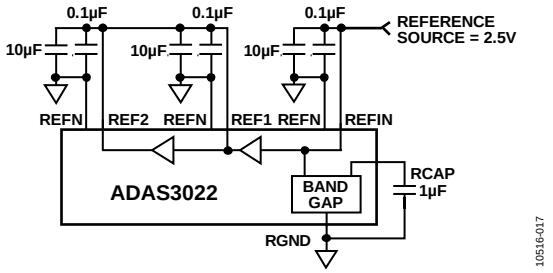


Figure 63. External Reference Using Internal Buffer

External Reference

For applications that require a precise, low drift 4.096 V reference, an external reference can also be used.

This option requires disabling the internal buffer by setting REFEN to 0 and driving or connecting REFIN to AGND; therefore, both hardware and software control are necessary. Attempting to drive the REF1 and REF2 pins prior to disabling the internal buffer can cause source/sink contention in the driving amplifiers.

Connect the precision 4.096 V reference, which serves as the main system reference, through a low impedance buffer (such as the AD8031 or the AD8605) to REF1 and REF2 as shown in Figure 64. Recommended references include the ADR434, ADR444, and ADR4540.

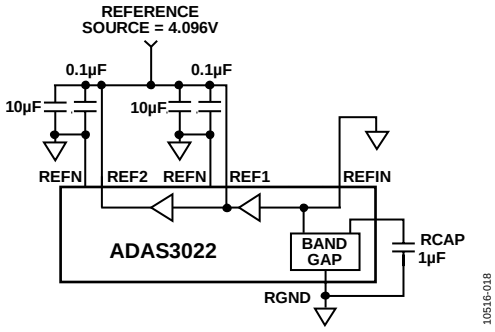


Figure 64. External Reference

If an op amp is used as the external reference source, take note of any concerns regarding driving capacitive loads. Capacitive loading for op amps usually refers to the ability of the amplifier to remain marginally stable in ac applications but can also play a role in dc applications, such as a reference source. Keep in mind that the reference source sees the dynamics of the bit decision process on the reference pins and further analysis beyond the scope of this data sheet may be required.

Reference Decoupling

With any of the reference topologies described in the Voltage Reference Input/Output section, the REF1 and REF2 reference pins of the ADAS3022 have dynamic impedances and require sufficient decoupling, regardless of whether the pins are used as inputs or outputs. This decoupling usually consists of a low ESR capacitor connected to each REF1 and REF2 and to the accompanying REFN return paths. Using X5R, 1206 size ceramic chip capacitors is recommended for decoupling in all the reference topologies described in the Voltage Reference Input/Output section.

The placement of the reference decoupling capacitors plays an important role in the system performance. Mount the decoupling capacitors on the same side as the ADAS3022, close to the REF1 and REF2 pins, with thick PCB traces. Route the return paths to the REFN inputs, which are in turn connected to the analog ground plane of the system. The resistance of the return path to ground should be minimized by using as many through vias as possible when it is necessary to connect to an internal PCB layer.

The REFN and RGND inputs should be connected with the shortest distance to the analog ground plane of the system, preferably adjacent to the solder pads, using several vias. One common mistake is to route these traces to an individual trace that connects to the ground of the system. This can introduce noise, which may adversely affect LSB sensitivity. To prevent such noise, it is highly recommended to use PCBs with multiple layers, including ground planes, rather than using single- or double-sided boards. Refer to UG-484 for more information about the PCB layout of the EVAL-ADAS3022EDZ.

For applications that use multiple ADAS3022 devices or other PulSAR ADCs, it is more effective to use the internal reference buffer to buffer the external reference voltage, thus reducing SAR conversion crosstalk.

The voltage reference temperature coefficient (TC) directly affects the full-scale accuracy of the system; therefore, in applications where full-scale accuracy is crucial, care must be taken with the TC. For example, a ±15 ppm/°C TC of the reference changes the full-scale accuracy by ±1 LSB/°C.

POWER SUPPLY

The ADAS3022 uses five supplies: AVDD, DVDD, VIO, VDDH, and VSSH (see Table 9). Note that ACAP, DCAP, and RCAP are included in Table 9 for informational purposes only because these supplies are outputs of the on-chip supply regulators. Refer to UG-484 for more information about how these supplies are generated on the EVAL-ADAS3022EDZ.

Table 9. Power Supplies

Name	Function	Required
AVDD	Analog 5 V core	Yes
DVDD	Digital 5 V core	Yes, or can connect to AVDD
VIO	Digital input/output	Yes, and can connect to DVDD (for 5 V level)
VDDH	Positive high voltage	Yes, +15 V typ
VSSH	Negative high voltage	Yes, −15 V typ
ACAP	Analog 2.5 V core	No, on chip
DCAP	Digital 2.5 V core	No, on chip
RCAP	Analog 2.5 V core	No, on chip

Core Supplies

AVDD and DVDD supply the ADAS3022 analog and digital cores, respectively. Sufficient decoupling of these supplies is required, consisting of at least a 10 µF capacitor and a 100 nF capacitor on each supply. The 100 nF capacitors should be placed as close as possible to the ADAS3022. To reduce the number of supplies needed, DVDD can be supplied from the analog supply by connecting a simple RC filter between AVDD and DVDD, as shown in Figure 65.

VIO is the variable digital input/output supply and can be directly interfaced to any logic between 1.8 V and 5 V (DVDD supply maximum). To reduce the supplies needed, VIO can alternatively be connected to DVDD when DVDD is supplied from the analog supply through an RC filter. The recommended low dropout regulators are ADP3334, ADP1715, and ADP7102/ADP7104 for the AVDD, DVDD, and VIO supplies.

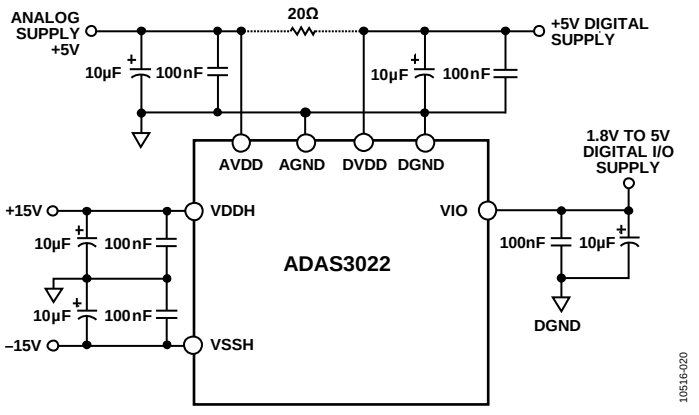


Figure 65. ADAS3022 Supply Connections

High Voltage Supplies

The high voltage bipolar supplies (VDDH and VSSH) are required and must be at least 2.5 V larger than the maximum input. For example, the supplies should be ±15 V for headroom in the ±24.576 V differential input range. Sufficient decoupling of these supplies is also required, consisting of at least a 10 µF capacitor and a 100 nF capacitor on each supply.

Power Dissipation Modes

The ADAS3022 offers two power dissipation modes: fully operational mode and power-down mode.

Fully Operational Mode

In fully operational mode, the ADAS3022 can perform conversions as soon as all internal bias currents are established.

Power-Down Mode

To minimize the operating currents of the device when it is idle, place the device in full power-down mode by bringing the PD input high. This places the ADAS3022 into a deep sleep mode, in which CNV activity is ignored and the digital interface is inactive. Refer to the Reset and Power-Down (PD) Inputs section for timing details. In deep sleep mode, the internal regulators (ACAP, RCAP, and DCAP) and the voltage reference are also powered down. To reestablish operation, return PD low. Note that before the device can operate at the specified performance, the reference voltage must charge up the external reservoir capacitor(s) and be allowed the specified settling time. Returning PD and RESET low from high resets the ADAS3022 digital core, including the CFG register, to its default state. Therefore, the desired CFG must be rewritten to the device and two dummy conversions must be completed before the device operation is restored to the configuration programmed prior to PD assertion.

CONVERSION MODES

The ADAS3022 offers two conversion modes to accommodate varying applications. The mode is set with the conversion mode select bit (CMS, Bit 1 of the CFG register).

Warp Mode (CMS = 0)

Setting CMS to 0 is useful when an aggregate throughput rate of 1 MSPS is required. However, in this mode, the maximum time between conversions is restricted. If this maximum period is exceeded, the conversion result may be corrupted. Therefore, this mode is more suitable for continually sampled applications.

Normal Mode (CMS = 1, Default)

Setting CMS to 1 is useful for all applications with a maximum aggregate throughput of 900 kSPS. In this mode, there is no restriction in terms of the maximum time between conversions. This mode is the default condition from the assertion of an asynchronous RESET. The main difference between normal mode and warp mode is the BUSY time; t_{QUIET} is slightly longer in normal mode than it is in warp mode.

DIGITAL INTERFACE

The ADAS3022 digital interface consists of asynchronous inputs, a busy indicator, and a 4-wire serial interface for conversion result readback and configuration register programming.

This interface uses the three asynchronous signals (CNV, RESET, and PD) and a 4-wire serial interface composed of $\overline{CS}$, SDO, SCK, and DIN. $\overline{CS}$ can also be tied to CNV for some applications.

Conversion results are available on the serial data output pin (SDO), and the 16-bit configuration word (CFG) is programmed on the serial data input pin (DIN). This register controls settings such as the channel to be converted, the programmable gain setting, and the reference choice (see the Configuration Register section for more information).

CONVERSION CONTROL

Conversions are initiated by the CNV input. The ADAS3022 is fully asynchronous and can perform conversions at any frequency from dc up to 1 MHz, depending on the conversion mode.

CNV Rising Edge—Start of a Conversion (SOC)

A rising edge on CNV changes the state of the ADAS3022 from track mode to hold mode and is all that is necessary to initiate a conversion. All conversion timing clocks are internally generated. After a conversion is initiated, the ADAS3022 ignores other activity on the CNV line (governed by the throughput rate) until the end of the conversion; the conversion can only be aborted by the power-down (PD) or RESET inputs.

When the ADAS3022 is performing a conversion and the BUSY output is driven high, the ADAS3022 uses a unique 2-phase conversion process to allow for safe data access and quiet times.

The CNV signal is decoupled from the $\overline{CS}$ pin, allowing multiple ADAS3022 devices to be controlled by the same processor. For applications where SNR is critical, the CNV source should have very low jitter. This can be achieved by using a dedicated oscillator or by clocking CNV with a high frequency, low jitter clock. For applications where jitter is more tolerable or a single device is in use, CNV can be tied to $\overline{CS}$. For more information about sample clock jitter and aperture delay, refer to the MT-007 Tutorial, *Aperture Time, Aperture Jitter, Aperture Delay Time—Removing the Confusion*.

Although CNV is a digital signal, it should be designed to ensure fast, clean edges with minimal overshoot, undershoot, and ringing. The CNV trace should be shielded by connecting a trace to ground, and a low value (such as 50 Ω) serial resistor termination should be added close to the output of the component that drives this line. In addition, care should be taken to avoid digital activity close to the sampling instant because such activity may result in degraded SNR performance.

BUSY Falling Edge—End of a Conversion (EOC)

The EOC event is indicated by BUSY returning low and can be used as a host interrupt. In addition, the EOC gates data access to and from the ADAS3022. If the current conversion result is not read prior to the following EOC event, the data is lost. Furthermore, if the CFG update is not completed prior to EOC, it is discarded and the current configuration is applied to future conversions. This pipeline ensures that the ADAS3022 has sufficient time to acquire the next sample to the specified 16-bit accuracy.

Conversion Timing

A detailed timing diagram of the conversion process is shown in Figure 66.

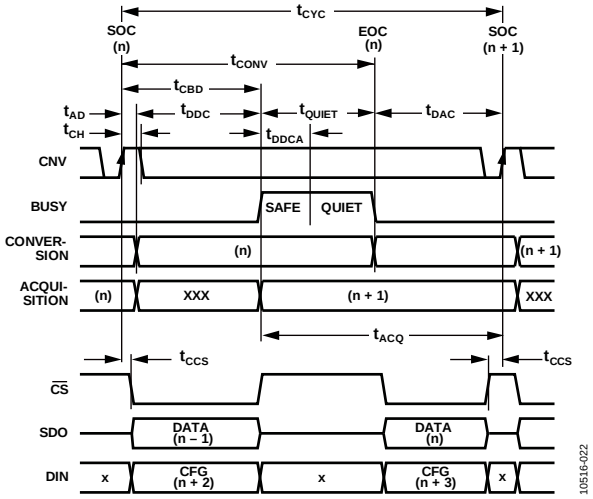


Figure 66. Basic Conversion Timing

Register Pipeline

To ensure that all CFG updates are applied during a known safe instant to the various circuit elements, the asynchronous data transfer is synchronized to the ADAS3022 timing engine using the EOC event. This synchronization introduces an inherent delay between updating the CFG register setting and the application of the configuration to a conversion. This pipeline from the end of the current conversion (n) consists of a two-deep delay (shown as (n + 2) in Figure 66) before the CFG setting takes effect. This means that two SOC and EOC events must elapse before the setting (that is, new channel, gain, and so on) takes effect. Note that the nomenclature (n), (n + 1), and so on is used in the remainder of the following digital sections for simplicity.

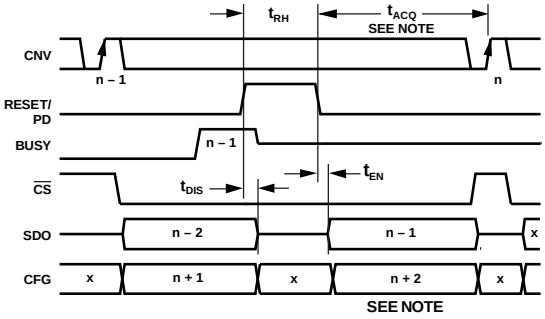
There is no pipeline after the end of a conversion, however, before data can be read back.

RESET AND POWER-DOWN (PD) INPUTS

The asynchronous RESET and PD inputs can be used to reset and power down the ADAS3022, respectively. Timing details are shown in Figure 67.

A rising edge on RESET or PD aborts the conversion process and places SDO into high impedance, regardless of the $\overline{CS}$ level. Note that RESET has a minimum pulse width (active high) time for setting the ADAS3022 into the reset state. See the Configuration Register section for the default CFG setting when the ADAS3022 returns from the reset state. If the default setting is used after RESET is deasserted (Logic 0), a period equal to the acquisition time (t_{ACQ}) must elapse before CNV can be asserted for the conversion result to be valid. If a conversion is initiated, the result will be corrupted. In addition, the output data from the previous conversion is cleared upon a reset. Attempting to access the data result prior to initiating a new conversion results in an invalid result.

When the device returns from power-down mode or from a reset and the default CFG is not used, there is no t_{ACQ} requirement; the first two conversions from power-up are undefined/invalid because the two-deep delay pipeline requirement must be satisfied to reconfigure the device to the desired setting.



NOTES
1. WHEN THE PART IS RELEASED FROM RESET, t_{ACQ} MUST BE MET FOR CONVERSION n IF USING THE DEFAULT CFG SETTING FOR CHANNEL IN0. WHEN THE PART IS RELEASED FROM POWER-DOWN, t_{ACQ} IS NOT REQUIRED, AND THE FIRST TWO CONVERSIONS, n AND n + 1, ARE UNDEFINED.

Figure 67. RESET and PD Timing

SERIAL DATA INTERFACE

The ADAS3022 uses a simple 4-wire interface and is compatible with FPGAs, DSPs, and common serial interfaces, such as SPI, QSPI, and MICROWIRE™. The interface uses the $\overline{CS}$, SCK, SDO, and DIN signals. Timing details for the serial interface are shown in Figure 68. SDO is activated when $\overline{CS}$ is asserted. The conversion result is output on SDO and is updated on SCK falling edges. Simultaneously, the 16-bit CFG word is updated, if desired, on the serial data input (DIN). The state of the clock phase select bit (CPHA, Bit 0) determines whether the MSB is output again on the first clock or whether the MSB − 1 bit is output when SDO is activated after the EOC.

Note that in Figure 67 and Figure 68, SCK is shown idling high. SCK can idle high or low, requiring that the system developer design an interface that suits setup and hold times for both SDO and DIN.

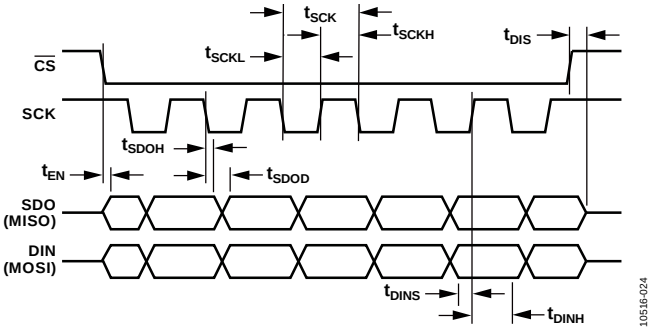


Figure 68. Serial Timing

CPHA

The clock phase select bit (CPHA, Bit 0) sets the first bit of the conversion result on SDO after the end of a conversion (see Figure 69).

Setting CPHA to 0 outputs the MSB when $\overline{CS}$ is asserted. Subsequent SCK falling edges clock out bits in an MSB − 1, MSB − 2, and so on fashion. This mode is useful for hosts limited to 16 clock edges where the first falling (or rising) edge can be used to latch the data.

Setting CPHA to 1 outputs the MSB not only when $\overline{CS}$ is asserted but also after the first SCK falling edge. Subsequent SCK falling edges clock out bits in an MSB − 1, MSB − 2, and so on fashion. This mode can be useful for sign extension applications.

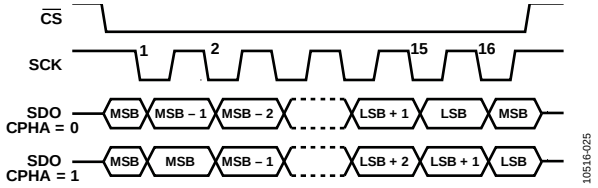


Figure 69. CPHA Details

Sampling on the SCK Falling Edge

To achieve the fastest data transfer rate, the host should sample data on the SCK falling edge, as long as there is a sufficient hold time of $\leq t_{SDOH}$ (see Figure 68). When using this method, data transfers should occur during the safe conversion time (t_{DDC}). Because this time is fixed, extending data reading or writing into the quiet conversion phase (t_{QUIET}) may cause data corruption. However, for systems that need slightly more time, t_{DDCA} (data during conversion additional) can be used.

Sampling on the SCK Rising Edge (Alternate Edge)

SPI or other alternate edge transfers typically require more time to access data because the total data transfer time of these slower hosts can be >t_{DDC}. If this is the case, the time from t_{QUIET} to the next CNV rising edge, which is known as the data access time after conversion (t_{DAC}) and is determined by the user, must be adjusted by lowering the throughput rate (CNV frequency), thus providing the necessary time. If this does not allow enough time, the data access can be broken up so that some data access occurs during this time followed by the remainder of data access occurring during the next t_{DDC} and t_{DDCA} times.

CFG Readback

The CFG result associated with the current conversion can be read back with an additional 16 SCK burst following the conversion result (see Figure 69). After the LSB of the conversion result is clocked out, the MSB of the CFG associated with that conversion follows. Subsequent SCK falling edges repeat the conversion result and CFG word. For example, when CPHA is 0, the MSB of the conversion result is output on the 32nd falling edge.

GENERAL CONSIDERATIONS

Because the time to access data is somewhat restricted, the following guidelines are useful in determining the ADAS3022 throughput, or CNV frequency, and the serial interface details. Note that in Figure 70 to Figure 72, t_{AD} is for reference purposes only and denotes a time without digital activity because such activity should not occur prior to or just after sampling.

Data Access During Conversion—Maximum Throughput

The maximum throughput rate per channel is determined mainly by the maximum SCK period of the host. When using the maximum throughput rate of 1 MSPS, the ADAS3022 has an almost symmetric period for both safe data and quiet times (~500 ns each; see Figure 70). Consequently, t_{DDC} is basically fixed and only provides the host ~500 ns to access data. Note that in Figure 70, t_{AD} is for reference purposes only and denotes a time without digital activity because such activity should not occur during the sampling edge. For 17 SCK edges (worst case), the minimum SCK frequency required to achieve a 1 MSPS (1 µs between CNV rising) aggregate throughput rate is

$$f_{SCK} \geq \frac{17}{t_{AD} + t_{DDC}} \geq 34 \text{ MHz}$$

Although additional time to access data can be attained by transferring data during t_{DDCA}, this is not recommended because the ADAS3022 performs sensitive bit decisions during this time. If t_{DDCA} is used, however, the minimum SCK frequency is

$$f_{SCK} \geq \frac{17}{t_{AD} + t_{DDC} + t_{DDCA}} \geq 25 \text{ MHz}$$

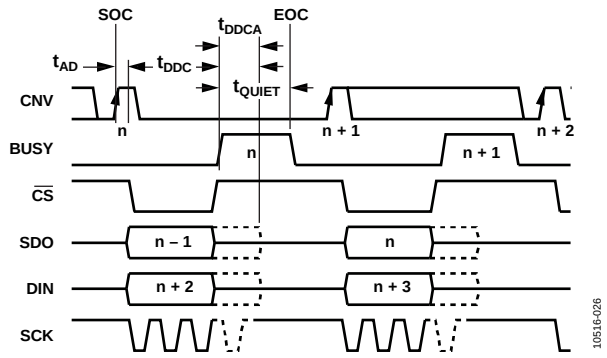


Figure 70. Data Access During Conversion

Data Access After/Spanning Conversion—Host Determined Throughput

For hosts that do not have the 34 MHz or 25 MHz SCK rates available, the maximum throughput rate cannot be achieved because the data access time after conversion, t_{DAC}, must be increased to allow more time to access data. In this case, there are three methods to access data:

- The first method is to adjust t_{DAC} for 17 SCK edges (worst case) and the additional $\overline{CS}$ to CNV setup and hold times. In this case, all data access occurs during t_{DAC}. This is the only method that can be used when using a slow host that cannot break up data into bytes or other partial data bursts.
- A second method is to break up the data into bursts that can transfer part of the data during t_{DAC} of the current conversion and the rest of the data during t_{DDC} of the next conversion. Note that $\overline{CS}$ can stay low throughout the CNV rising phase; however, serial clock activity should pause while the input is being sampled.
- A third method is to use the second method along with the additional t_{DDCA}, again noting that digital activity must cease after this time to prevent the current conversion from becoming corrupted.

In any of these methods, if the time between conversions (t_{CYC}) is exceeded for the fastest possible throughput mode (CMS = 0), the conversion results will be inaccurate. If this is the case, the fully asynchronous mode (CMS = 1) must be selected (see the Conversion Modes section for details).

Figure 71 shows a basic timing diagram for all three methods. For conversion (n), the data is read back after the end of a conversion (n), with the remainder of data read into the next (n + 1) conversion.

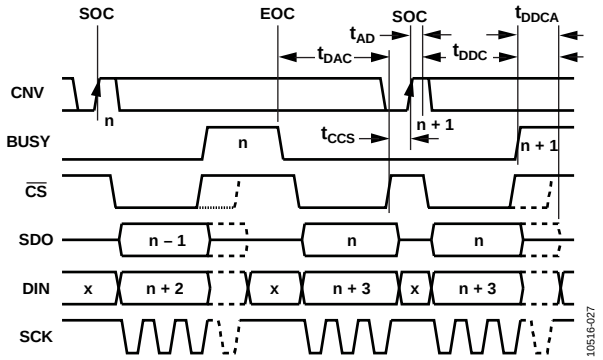
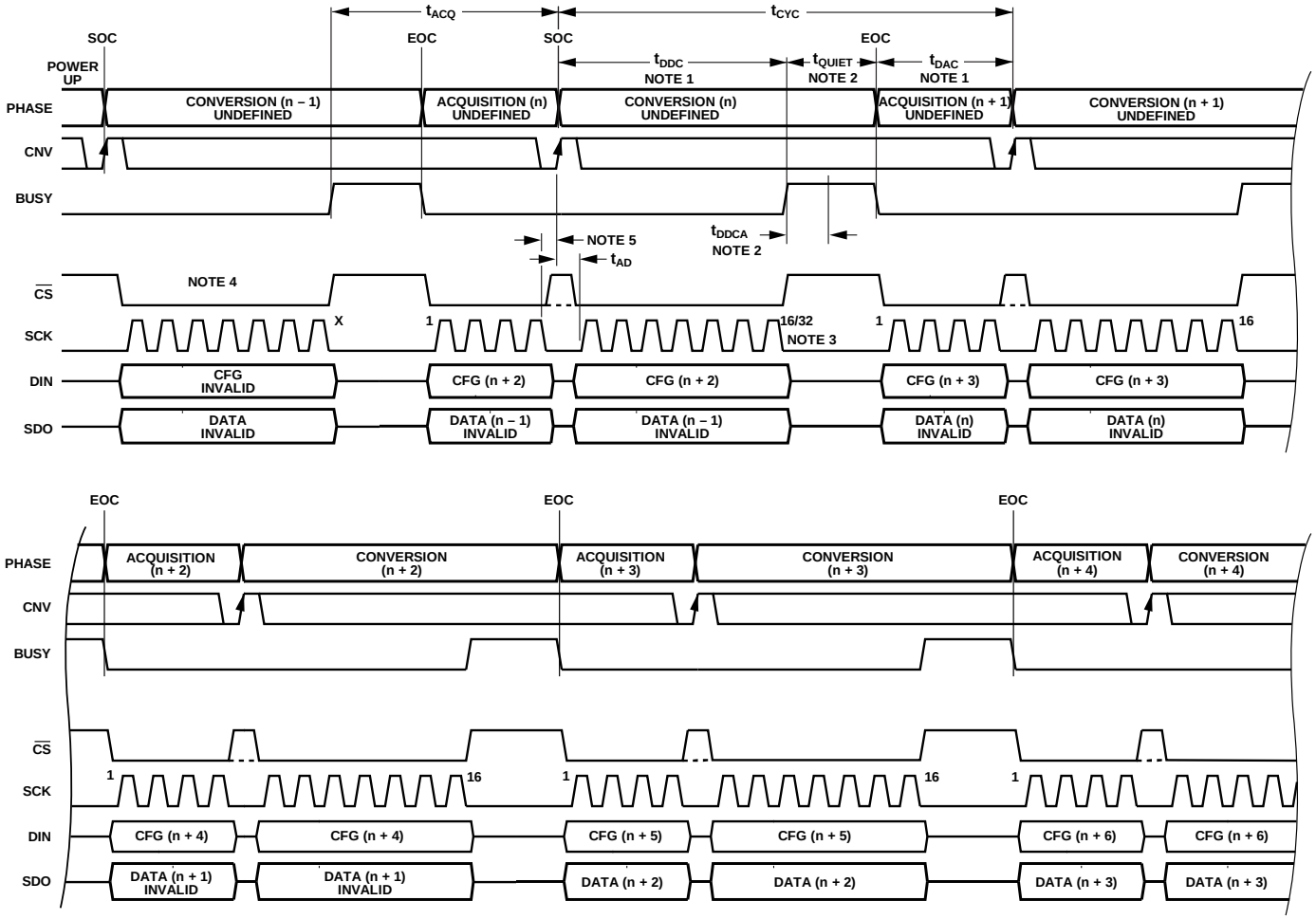


Figure 71. Data Access Spanning Conversion

GENERAL TIMING

Figure 72 is a general timing diagram showing the complete register to conversion and readback pipeline delay. The figure details the timing upon power-up or upon returning from a full power-down by use of the PD input. Figure 73 and Figure 74 show the general timing diagrams when only the auxiliary ADC input channel pair is enabled for the data read during conversion (RDC) mode and the read after conversion (RAC) mode, respectively.



NOTES
1. DATA ACCESS CAN OCCUR DURING A CONVERSION (t_{DDC}), AFTER A CONVERSION (t_{DAC}), OR BOTH DURING AND AFTER A CONVERSION. THE CONVERSION RESULT AND THE CFG REGISTER ARE UPDATED AT THE END OF A CONVERSION (EOC).
2. DATA ACCESS CAN ALSO OCCUR UP TO t_{DDCA} WHILE BUSY IS ACTIVE (SEE THE DIGITAL INTERFACE SECTION FOR DETAILS). ALL OF THE BUSY TIME CAN BE USED TO ACQUIRE DATA.
3. A TOTAL OF 16 SCK FALLING EDGES IS REQUIRED FOR A CONVERSION RESULT. AN ADDITIONAL 16 EDGES ARE REQUIRED TO READ BACK THE CFG RESULT ASSOCIATED WITH THE CURRENT CONVERSION.
4. $\overline{CS}$ CAN BE HELD LOW OR CONNECTED TO CNV. $\overline{CS}$ WITH FULL INDEPENDENT CONTROL IS SHOWN IN THIS FIGURE.
5. FOR OPTIMAL PERFORMANCE, DATA ACCESS SHOULD NOT OCCUR DURING THE SAMPLING EDGE. A MINIMUM TIME OF THE APERTURE DELAY (t_{AD}) SHOULD ELAPSE PRIOR TO DATA ACCESS.

Figure 72. General Timing Diagram

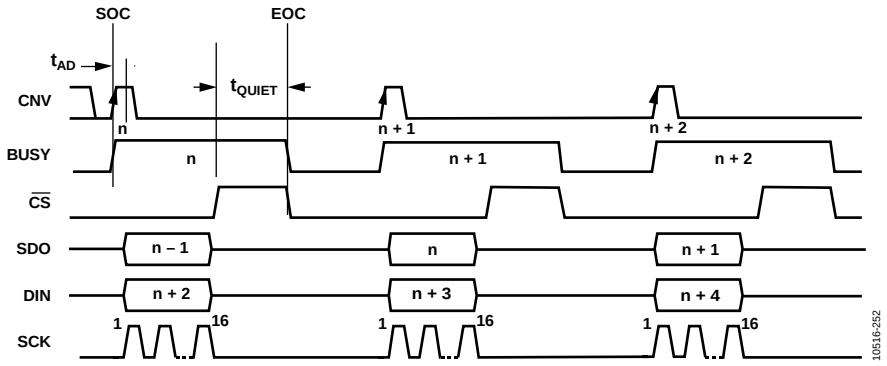


Figure 73. General Timing Diagram of AUX Input Channel Pair (RDC)

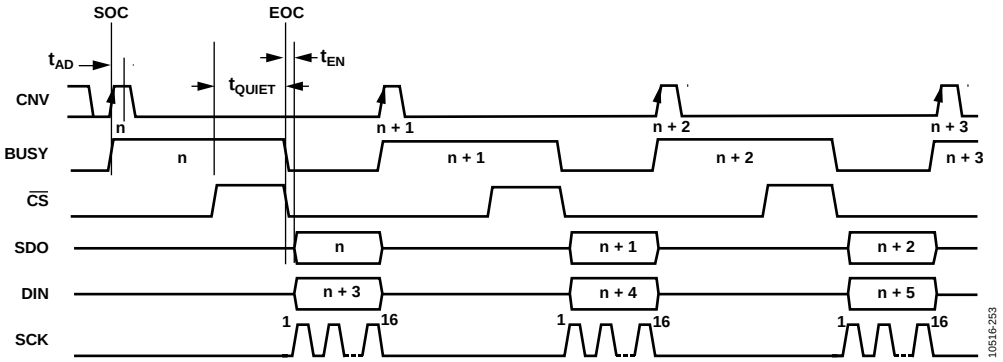


Figure 74. General Timing Diagram of AUX Input Channel Pair (RAC)

CONFIGURATION REGISTER

The configuration register, CFG, is a 16-bit, programmable register for selecting all of the ADAS3022 user-programmable options (see Table 11). The register is loaded when data is read back for the first 16 SCK rising edges and is updated at the next EOC. Note that there is always a two-deep delay (n + 2) when writing CFG and when reading back CFG for the setting associated with the current conversion.

The default CFG setting is applied when the ADAS3022 returns from the reset state (RESET = high) to the operational state (RESET = low). However, when the ADAS3022 returns from the full power-down state (PD = high) to an enabled state (PD = low), the default CFG setting is not applied, and at least two dummy conversions are required for the user-specified CFG setting to take effect. Therefore, the default value is CFG[15:0] = 0x8FCF. This sets the ADAS3022 as follows:

- Overwrites contents of CFG register
- Selects the IN0 input channel referenced to COM
- Configures the PGIA gain to 0.20 (±20.48 V)
- Selects the multiplexer input
- Disables the internal channel sequencer
- Disables the temperature sensor
- Enables the internal reference
- Selects normal conversion mode
- Selects SPI interface mode

Table 10. Configuration Register, CFG; Default Value = 0x8FCF (1000 1111 1100 1111)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG	INx	INx	INx	COM	RSV	PGIA	PGIA	PGIA	MUX	SEQ	SEQ	TEMPB	REFEN	CMS	CPHA

Table 11. Configuration Register Bit Description

Bits	Bit Name	Description			
15	CFG	Configuration update. 0 = keep current configuration settings. 1 = overwrite contents of register (default).			
[14:12]	INx	Input channel selection in binary fashion. See the Multiplexer section.			
		Bit 14	**Bit 13**	**Bit 12**	**Channel**
		0	0	0	IN0 (default)
		…	…	…	
		1	1	1	IN7
11	COM	IN[7:0] common channel input. AUX+ and AUX− are not referenced to COM. 0 = channels are referenced in differential pairs: IN0/IN1, IN2/IN3, IN4/IN5, and IN6/IN7 (see the On Demand Conversion Mode section). 1 = each channel is referenced to a common sense, COM (default).			
10	RSV	Reserved. Setting or clearing this bit has no effect.			
[9:7]	PGIA	Programmable gain selection (see the Input Structure section). In basic sequencer modes, this register configures the range for all channels. In advanced sequencer mode, this register sets the range for IN0 (COM = 1) or the IN0/IN1 pair (COM = 0). See the Advanced Mode section for the PGIA configurations of individual channels or channel pairs.			
		Bit 9	**Bit 8**	**Bit 7**	**Absolute Input Voltage Range**
		0	0	0	±24.576 V
		0	0	1	±10.24 V
		0	1	0	±5.12 V
		0	1	1	±2.56 V
		1	0	0	±1.28 V
		1	0	1	±0.64 V
		1	1	0	Not used
		1	1	1	±20.48 V (default)
6	MUX	Multiplexer/auxiliary channel input (see the Auxiliary Input Channel section). 0 = selects auxiliary channel on AUX± inputs as active channel. 1 = uses the selected analog front end (AFE) channel/channel pair (default).			

Bits	Bit Name	Description		
[5:4]	SEQ	Channel sequencer. Allows for scanning channels sequentially from IN0 to INx. INx is the last channel converted prior to resetting the sequence back to IN0 and is specified by the channel selected in the INx[2:0] configuration bits (see the On Demand Conversion Mode section).		
		Bit 5	**Bit 4**	**Function**
		0	0	Disable sequencer (default)
		0	1	Update configuration during basic sequence
		1	0	Initialize advanced sequencer
		1	1	Initialize basic sequencer
3	TEMPB	Temperature sensor enable control (see the On Demand Conversion Mode section). 0 = internal temperature sensor enabled. 1 = internal temperature sensor disabled (default).		
2	REFEN	Internal reference selection (see the Pin Configuration and Function Descriptions and Voltage Reference Input/Output sections for more information). 0 = disables the internal reference. The internal reference buffer is disabled by pulling REFIN to ground. 1 = enables the internal reference (default).		
1	CMS	Conversion mode select (see the Conversion Modes section). 0 = uses the warp mode for conversions with a time between conversion restriction. 1 = uses the normal mode for conversions (default).		
0	CPHA	MSB select (see the CPHA section). 0 = asserting $\overline{CS}$ after the end of a conversion places the MSB on SDO, and the first SCK falling edge places (MSB − 1) on SDO. 1 = asserting $\overline{CS}$ after the end of a conversion places the MSB on SDO, and the first SCK falling edge repeats MSB on SDO (default).		

ON DEMAND CONVERSION MODE

When the channel sequencer is disabled, the input channels can be selected for the on demand conversions based on the MUX and TEMPB bit settings, as shown in Table 12. For example, the only internal TEMP sensor channel conversions in this mode can be obtained by setting the MUX = TEMPB = 0.

Table 12. Input Channel Select

MUX	TEMPB	Output
1	1	INx[14:12] Channels
1	0	Invalid
0	1	AUX± Input Channels
0	0	Internal Temperature Sensor Channel

CHANNEL SEQUENCER DETAILS

The ADAS3022 includes a channel sequencer, which is useful for scanning channels in a sequential order. Channels are scanned individually with reference to COM or as pairs and can also include the auxiliary channel pair and/or the internal temperature sensor measurement. After the last programmed measurement is sampled, the ADAS3022 sequencer is reset to the first channel (IN0) or channel pair (IN0/IN1) and repeats the sequence until the sequencer is disabled or an asynchronous RESET or PD occurs.

When the channel sequencer is enabled, for all differential pairs, the positive terminals are the even channels (IN0, IN2, IN4, and IN6), and the negative terminals are, conversely, the odd channels (IN1, IN3, IN5, and IN7). When the channel sequencer is disabled, the user can assign either positive or negative terminals to even or odd channels for all differential pairs, depending on the INx[14:12] settings. For example, if INx[14:12] = 001 when using the IN0/IN1 pair, IN1 is the positive input and IN0 is the negative input.

Each sequence loop always starts with IN0 or IN0/IN1 and terminates with either the last channel/channel pair set in the INx bits, the temperature sensor, or the auxiliary input channel, depending on the configuration word. Table 13 provides a quick reference for how the device responds to the programmed configuration. For the first case, the channel sequencer scans Channel IN0 through Channel IN3 in a repeated fashion. Note that the last conversion is corrupted when exiting the sequencer.

Table 13. Typical Channel Sequencer Example

INx[14:12]	COM	MUX	TEMPB	End of Sequence
011	1	1	1	IN3 (to COM)
111	1	1	1	IN7 (to COM)
11x	0	1	1	IN6 to IN7
111	1	1	0	TEMPB
111	1	0	1	AUX±
111	1	0	0	AUX±

INx and COM Inputs (MUX = 1, TEMPB = 1)

To use individual INx channels with reference to COM or pairs of INx channels in a sequence without converting the AUX or temperature sensor channels, the MUX and TEMPB bits must be set to 1. The last channel to be converted in the sequence is specified by the channel set in the INx bits. After the last channel is scanned, the next conversion starts over at IN0 or IN0/IN1. For paired channels, the channels are paired depending on the last channel set in INx. Note that the channels are always paired with the positive input on the even channels (IN0, IN2, IN4, IN6) and the negative input on the odd channels (IN1, IN3, IN5, IN7). Therefore, setting INx to 110 or 111 scans all pairs with the positive inputs dedicated to IN0, IN2, IN4, and IN6. For example, to scan four single channels, set INx to 011, COM to 1, and MUX to 1, which results in a sequence order of IN0, IN1, IN2, IN3, IN0, IN1, IN2, and IN3.

INx and COM Inputs with AUX Inputs (MUX = 0, TEMPB = 1)

To use individual INx channels with reference to COM or pairs of INx channels with the AUX inputs in a sequence, the MUX bit must be set to 0 to append the AUX channel to the end of the sequence (after the channel set in INx is scanned). Note that the AUX input is a pair, whereas the INx channel can be referenced to COM or pairs of INx channels. For example, to scan four single channels and the AUX inputs, set INx to 011, COM to 1, and MUX to 0, which results in a sequence order of IN0, IN1, IN2, IN3, AUX, IN0, IN1, IN2, IN3, AUX, and so on.

INx and COM Inputs with Temperature Sensor (MUX = 1, TEMPB = 0)

To append the temperature sensor conversion to the end of the input channel sequence, the TEMPB bit must be set low in the configuration word. Note that the temperature sensor requires at least 5 µs between conversions. The data is output in straight binary format.

INx and COM Inputs with AUX Inputs and Temperature Sensor (MUX = 0, TEMPB = 0)

Both temperature sensor conversions and auxiliary channel conversions can be appended to the end of the input sequence by setting the MUX and TEMPB bits in the CFG register. For example, to scan all input channels with respect to COM, the temperature sensor, and the auxiliary channel at once, the user must set INx to 111, COM to 1, MUX to 0, and TEMPB to 0. The resulting sequence would be IN0, IN1, IN2, IN3, IN4, IN5, IN6, IN7, temperature sensor, and AUX.

Sequencer Modes

The ADAS3022 has two sequencer modes, which are configured with the SEQ bits: basic mode and advanced mode. Basic mode can be used when all channels are configured with the same PGIA range. Advanced mode allows individual channel ranges to be programmed using two additional advanced sequence registers, ASR0 and ASR1. The SEQ bits are used to enable the sequencer. Setting SEQ to 01, 10, or 11 specifies which sequencer mode is used. Depending on the mode, basic or advanced sequencing determines the next data into DIN.

Note that for any sequencer update there exists a two-deep delay when writing the register for the setting to take effect.

Basic Sequencer Mode (SEQ = 11)

The basic mode is useful for systems that use the same PGIA range on all channels. In basic sequencer mode, all that is required is a single CFG word to place the ADAS3022 in an automatically scanned mode. On the second conversion following the EOC for sequencer CFG, the sequencer starts.

After the CFG for basic sequence updates, DIN must be held low for at least the MSB during the data readback or a new CFG word will update, disabling the sequencer.

Update During Sequence (SEQ = 01)

Some of the CFG settings, such as PGIA and CMS, can be updated during a sequence. Writing a new CFG word with the appropriate bits to be changed for the (n + 2) conversion updates the sequencer from that point; all channels then use, for example, the new PGIA value. Note that changing bits in INx for the last channel or changing COM reinitializes the sequencer at the (n + 2) conversion. A more practical method is to use the advanced sequencer mode as described in the Advanced Sequencer Mode (SEQ = 10) section.

Advanced Sequencer Mode (SEQ = 10)

The advanced mode is useful for systems that require different gains for different individual INx inputs or different pairs of INx inputs. In this mode, two additional registers are used to program the various gain settings. After the initial CFG word enabling the advanced sequencer mode is written, the ADAS3022 expects to receive at least one additional data transfer for the first advanced sequencer register, ASR0, or both advanced sequencer registers, depending on how many channels are in the sequence. Each ASR requires a conversion and a corresponding EOC to load the data into the device. The user cannot simply write 48 bits all at once because, as with all CFG word transfers, only the first 16 bits are latched and updated at EOC.

Note that the PGIA setting for IN0 or IN0/IN1 is written in the initial CFG register, and if using pairs of INx channels, only ASR0 is required. After the CFG and the associated advanced sequencer registers are updated, DIN must be held low for at least the MSB of subsequent data transfers; otherwise, the advanced sequencer mode will be aborted.

Table 14. Advanced Sequencer Register 0

Bits	Function
15	ASR0 write enable 0 = update ASR0 following CFG for advanced sequencer 1 = enters normal CFG update
[14:11]	Reserved
[10:8]	PGIA for IN1 or IN2/IN3
7	Reserved
[6:4]	PGIA for IN2 or IN4/IN5
3	Reserved
[2:0]	PGIA for IN3 or IN6/IN7

Table 15. Advanced Sequencer Register 1

Bits	Function
15	ASR1 write enable 0 = update ASR1 following ASR0 1 = enters normal CFG update
[14:12]	PGIA for IN4
11	Reserved
[10:8]	PGIA for IN5
7	Reserved
[6:4]	PGIA for IN6
3	Reserved
[2:0]	PGIA for IN7

OUTLINE DIMENSIONS

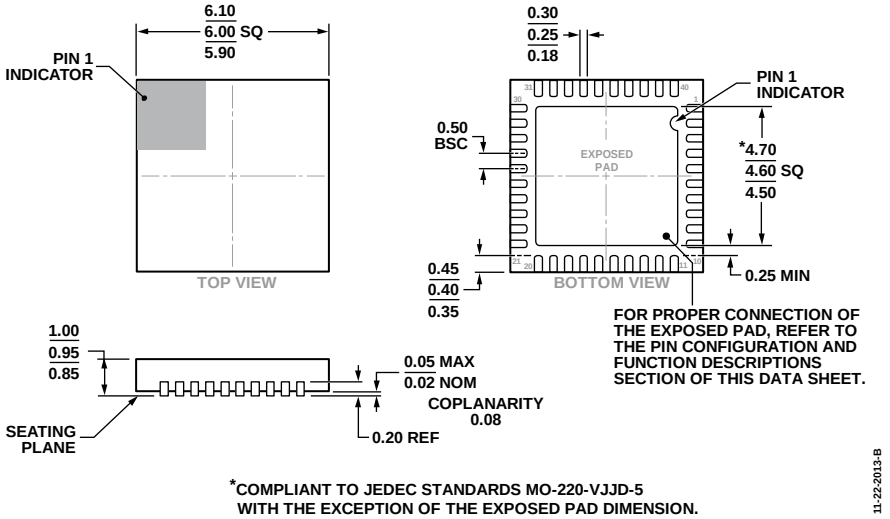


Figure 75. 40-Lead Lead Frame Chip Scale Package (LFCSP_VQ)
6 mm × 6 mm Body, Very Thin Quad
(CP-40-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADAS3022BCPZ	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-40-15
ADAS3022BCPZ-RL7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-40-15
EVAL-ADAS3022EDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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