



Features

The MAX4003 is available in an 8-bump chip-scale package (UCSP™), an 8-pin μ MAX package, and an 8-pin thin QFN package. The device consumes 5.9mA with a 3.0V supply and only 13 μ A when the device is in shutdown.

- Cellular Handsets (TDMA, CDMA, GPRS, GSM)
- TSSI for Wireless Terminal Devices
- Transmitter Power Measurement and Control
- RSSI for Fiber Modules

UCSP is a trademark of Maxim Integrated Products, Inc.

- ◆ Complete RF Detector
- ◆ Frequency Range from 100MHz to 2500MHz
- ◆ Input Range of -58dBV to -13dBV
(-45dBm to 0dBm into 50Ω)
- ◆ Fast Response: 70ns in 10dB Steps
- ◆ Low-Current Consumption: 5.9mA at $V_{CC} = 3.0V$
- ◆ 13μA (typ) Shutdown Current
- ◆ Available in 8-Bump UCSP or 8-Pin μMAX and Thin QFN Packages

PART	TEMP RANGE	PIN/BUMP-PACKAGE	TOP MARK
MAX4003EBL-T	-40°C to +85°C	8 UCSP-8	ABV
MAX4003EUA	-40°C to +85°C	8 μ MAX	—
MAX4003ETA-T	-40°C to +85°C	8 Thin QFN-EP	ADG

The image shows two pin configurations for the MAX4003 IC. The left diagram is the TOP VIEW (UCSP package) showing a 3x3 grid of pins with labels: RFIN, SHDN, GND, VCC, CLPF, and OUT. The right diagram is the TOP VIEW (MAX package) showing a 4-pin configuration: RFIN, SHDN, GND, CLPF, VCC, OUT, and N.C.

TOP VIEW (UCSP)

Pin 1: RFIN
Pin 2: SHDN
Pin 3: GND
Pin 4: VCC
Pin 5: CLPF
Pin 6: OUT
Pin 7: GND

TOP VIEW (MAX)

Pin 1: RFIN
Pin 2: SHDN
Pin 3: GND
Pin 4: CLPF
Pin 5: VCC
Pin 6: OUT
Pin 7: N.C.

The schematic diagram illustrates the internal architecture of the MAX4003 precision centred level shifter. The circuit is powered by V_{CC} and GND , with a shutdown control input \overline{SHDN} . The input signal $RFIN$ passes through a resistor and a diode (DET) to the first of four cascaded 10dB gain stages. Each stage is followed by a diode (DET) connected to an offset compensation (OFFSET COMP) circuit. The signal then passes through a fifth 10dB gain stage and a diode (DET) to a 9mV gain stage. The output of the 9mV stage is connected to an output delay block and a 1X buffer stage. A low-noise bandgap reference is connected to the 9mV stage and the 1X buffer. The final output is filtered by a CLPF. The MAX4003 logo is shown at the bottom right.

100MHz to 2500MHz, 45dB RF Detector in a UCSP

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND-0.3V to +5.25V
 SHDN, CLPF to GND-0.3V to (V_{CC} + 0.3V)
 RFIN+6dBm
 OUT Short Circuit to GND 10s
 Continuous Power Dissipation (T_A = +70°C)
 8-Bump UCSP (derate 4.7mW/°C above +70°C)379mW

8-Pin μMAX (derate 4.5mW/°C above +70°C)362mW
 8-Pin Thin QFN (derate 24.4mW/°C above +70°C) ...1951mW
 Operating Temperature Range-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +150°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V, V_{SHDN} = V_{CC}, C_{CLPF} = 0.1μF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V _{CC}		2.7		5.0	V
Supply Current	I _{CC}	V _{CC} = 5.0V		5.9	10	mA
				13	30	μA
Shutdown Input Current	I _{SHDN}	V _{SHDN} = 3.0V		5	20	μA
		V _{SHDN} = 0V		-0.01	±5	
Logic High Threshold Voltage	V _{IH}		1.8			V
Logic Low Threshold Voltage	V _{IL}				0.8	V
DETECTOR OUTPUT						
Voltage Range	V _{OUT}	RFIN = 0dBm		1.45		V
		RFIN = -45dBm		0.36		
Output Voltage in Shutdown	V _{OUT}	V _{SHDN} = 0V		1		mV
Output-Referred Noise		f _o = 150kHz		8		nV/√Hz
Small-Signal Bandwidth	BW	C _{CLPF} = 150pF		8		MHz
Slew Rate		V _{OUT} = 0.36V to 1.45V, C _{CLPF} = 150pF		5		V/μs

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AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 3.0V$, $V_{SHDN} = V_{CC}$, $C_{CLPF} = 0.1\mu F$, $f_{RF} = 100MHz$ to $2500MHz$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

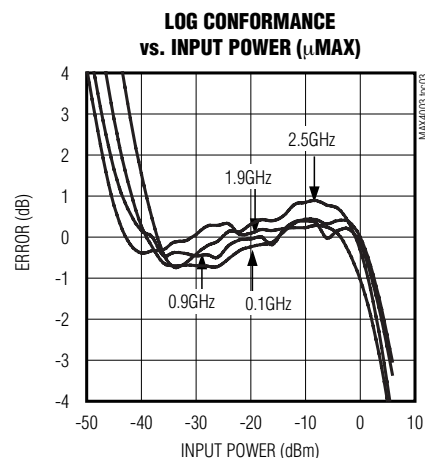
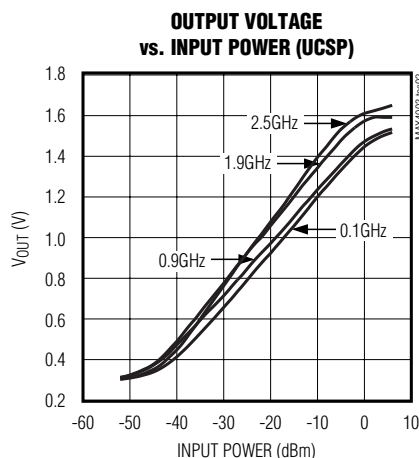
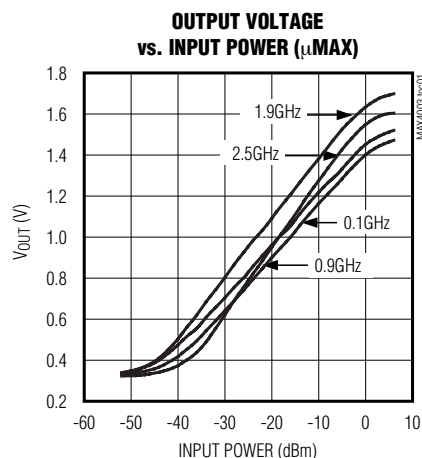
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Input Frequency Range	f_{RF}		100		2500	MHz
RF Input Voltage Range	V_{RF}	(Note 2)	-58		-13	dBV
Equivalent RF Input Power Range	P_{RF}	With 50Ω termination (Note 2)	-45		0	dBm
Logarithmic Slope		$f_{RF} = 100MHz$, $T_A = +25^\circ C$	22.8	25.5	28.2	mV/dB
		$f_{RF} = 100MHz$	22.5		28.5	
		$f_{RF} = 900MHz$		25.0		
		$f_{RF} = 1900MHz$		29.0		
Logarithmic Intercept	P_X	$f_{RF} = 100MHz$, $T_A = +25^\circ C$	-62.3	-57	-51.7	dBm
		$f_{RF} = 100MHz$	-64		-50	
		$f_{RF} = 900MHz$		-57		
		$f_{RF} = 1900MHz$		-56		
RFIN Input Impedance	R_{IN}			2		k Ω
	C_{IN}			0.5		pF

Note 1: All devices are 100% production tested at $T_A = +25^\circ C$ and are guaranteed by design for $T_A = -40^\circ C$ to $+85^\circ C$ as specified. All production AC tests are done at 100MHz.

Note 2: Typical minimum and maximum range of the detector.

Typical Operating Characteristics

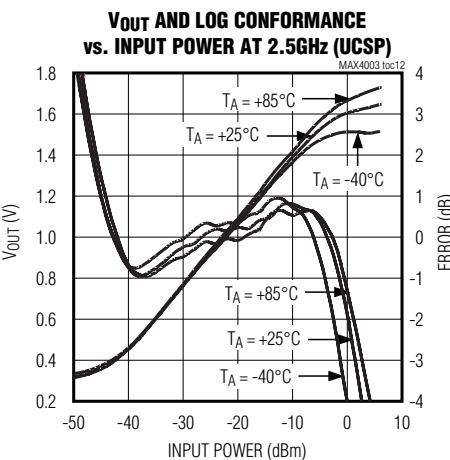
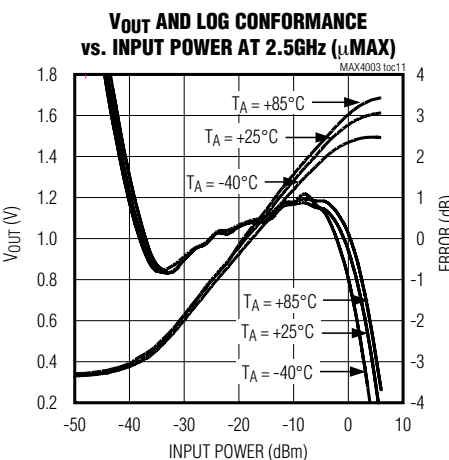
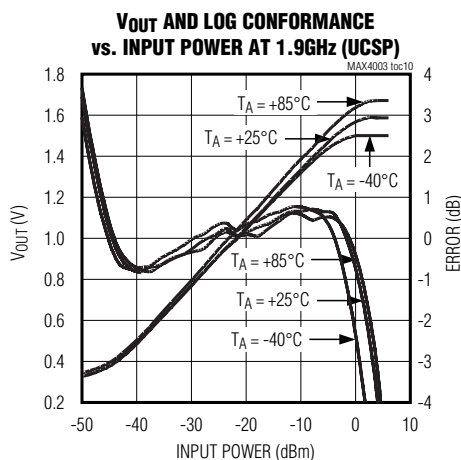
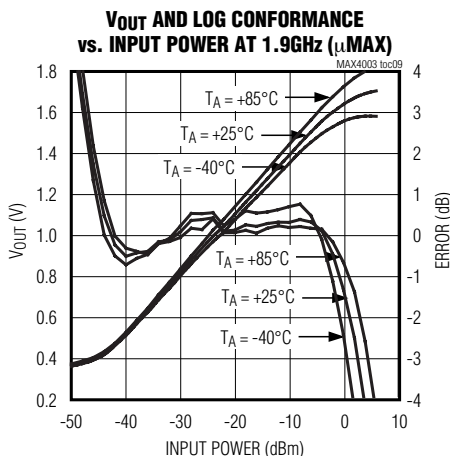
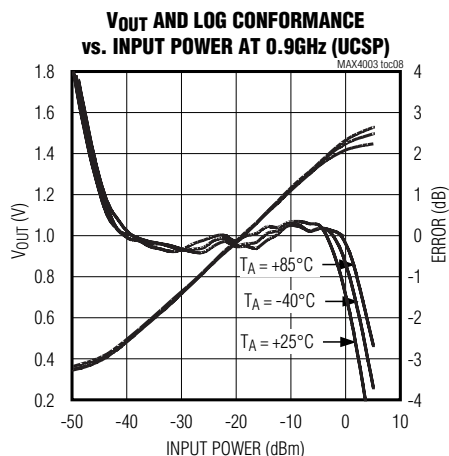
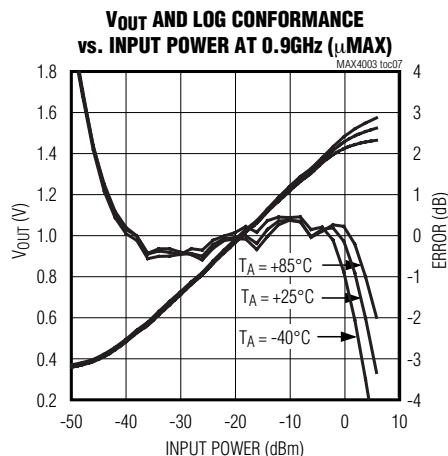
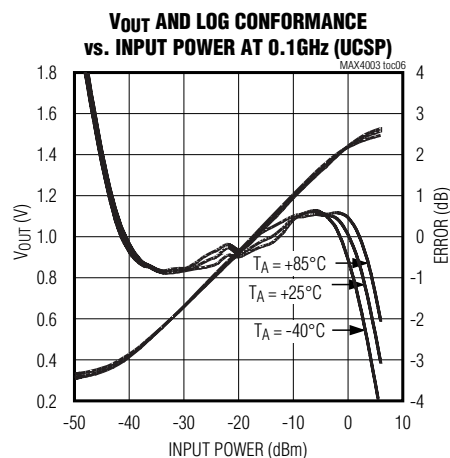
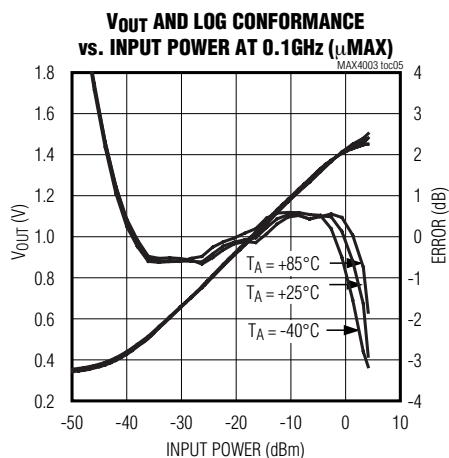
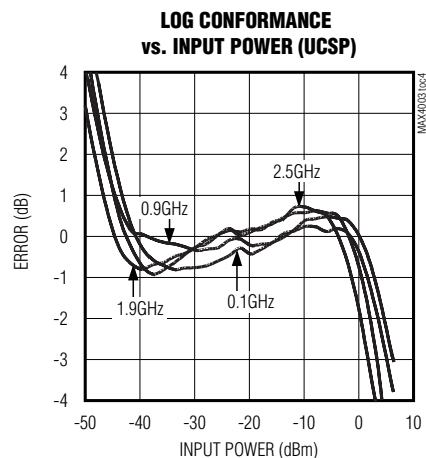
($V_{CC} = V_{SHDN} = 3.0V$, $C_{CLPF} = 0.1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)



100MHz to 2500MHz, 45dB RF Detector in a UCSP

Typical Operating Characteristics (continued)

($V_{CC} = V_{SHDN} = 3.0V$, $C_{CLPF} = 0.1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

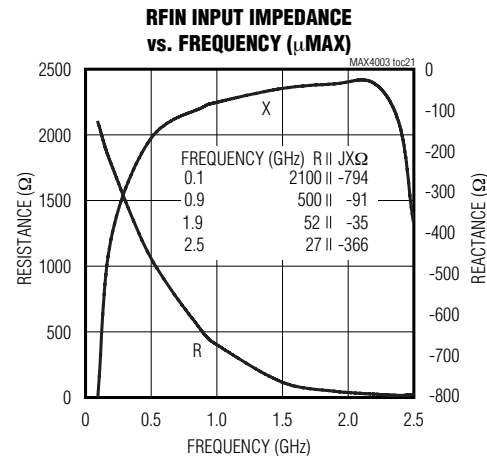
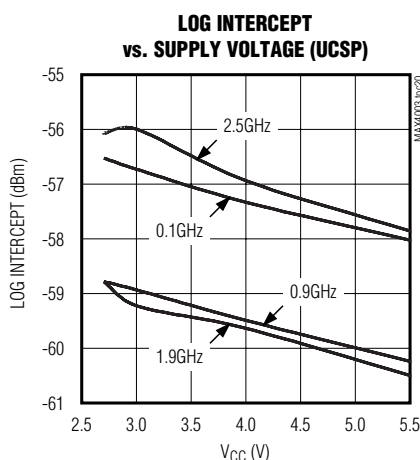
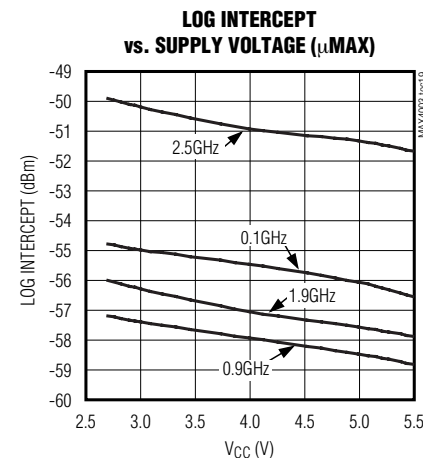
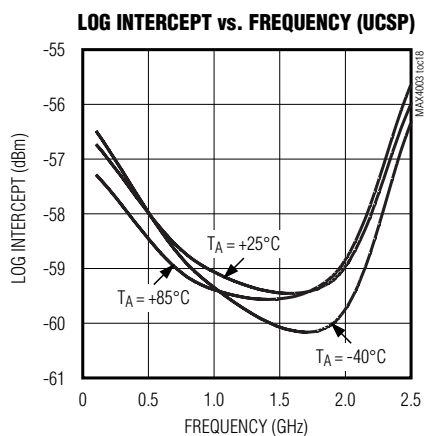
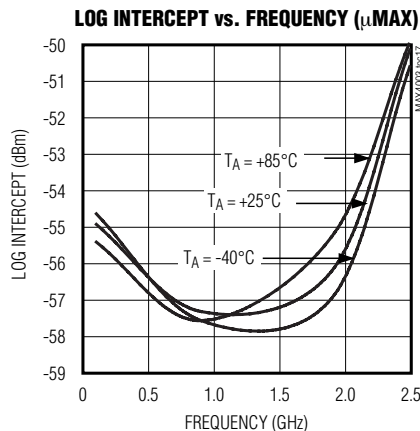
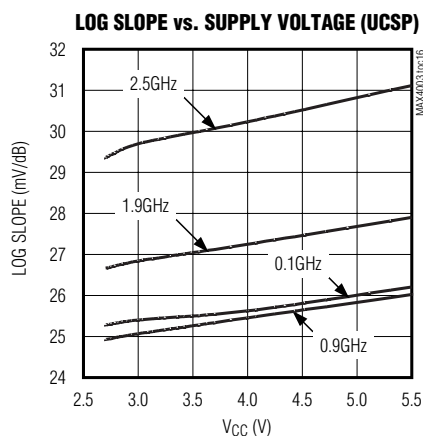
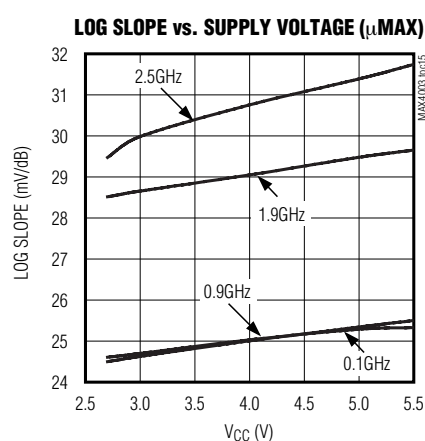
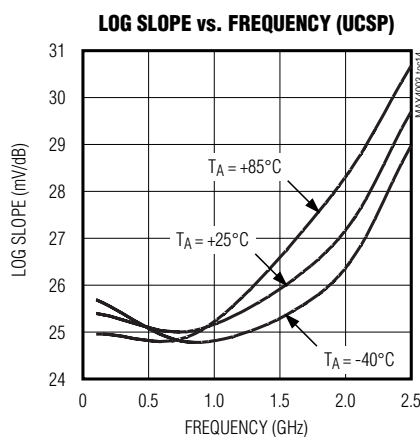
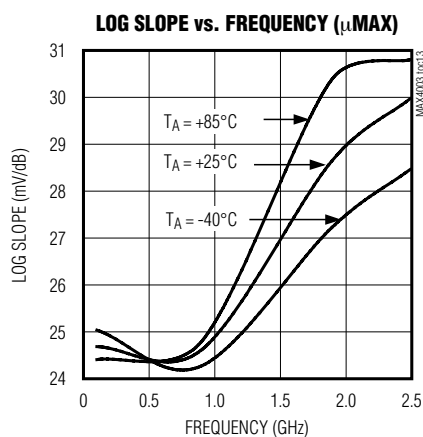


100MHz to 2500MHz, 45dB RF Detector in a UCSP

MAX4003

Typical Operating Characteristics (continued)

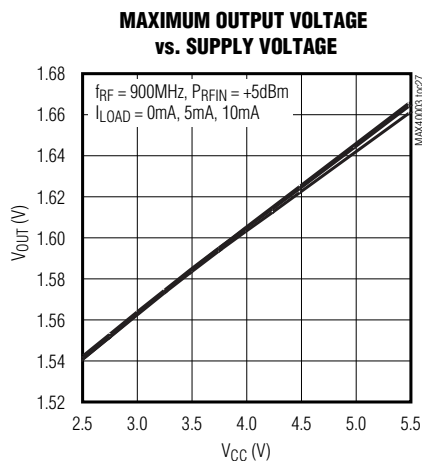
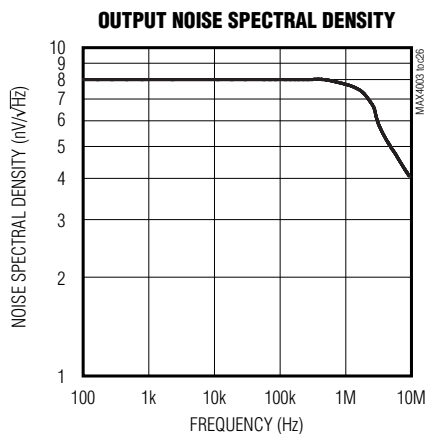
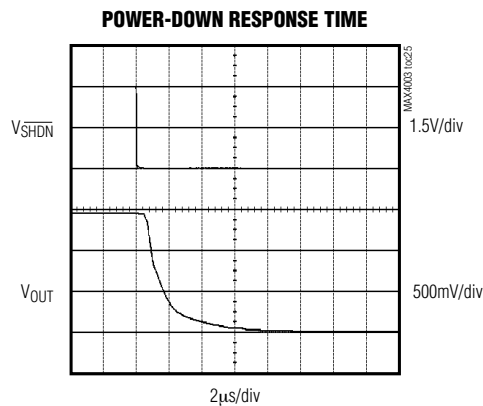
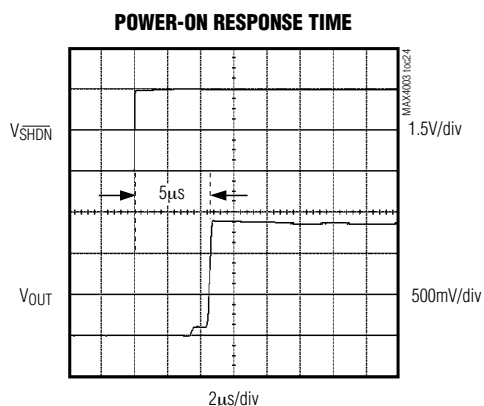
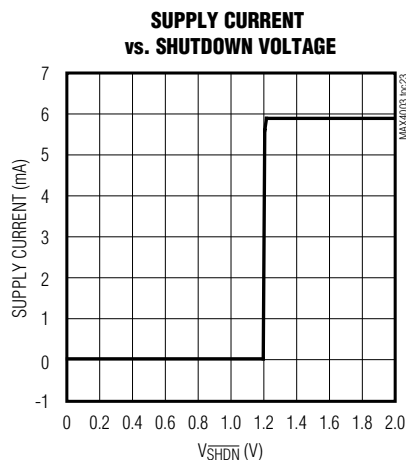
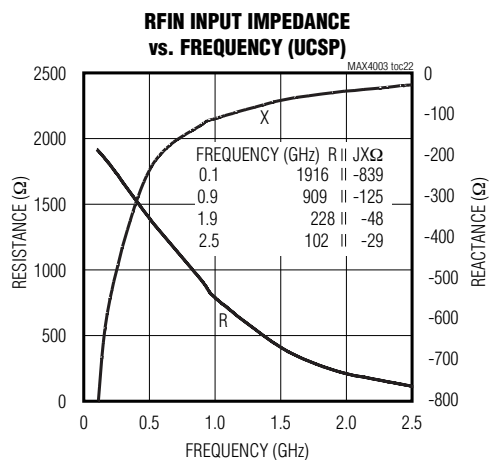
($V_{CC} = V_{SHDN} = 3.0V$, $C_{CLPF} = 0.1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)



100MHz to 2500MHz, 45dB RF Detector in a UCSP

Typical Operating Characteristics (continued)

($V_{CC} = V_{SHDN} = 3.0V$, $C_{CLPF} = 0.1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

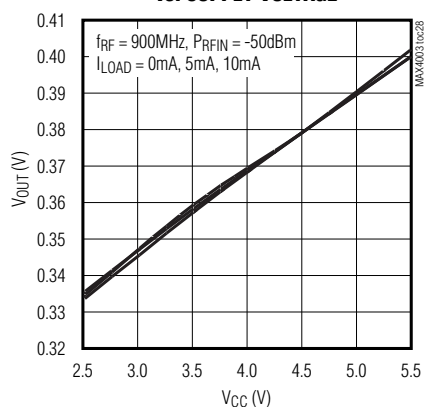


100MHz to 2500MHz, 45dB RF Detector in a UCSP

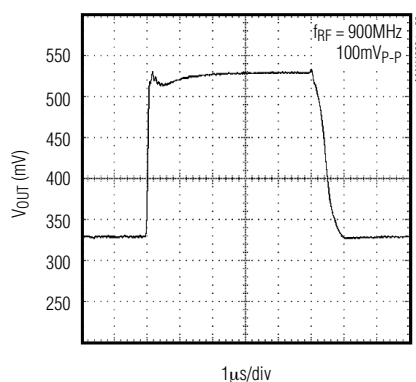
Typical Operating Characteristics (continued)

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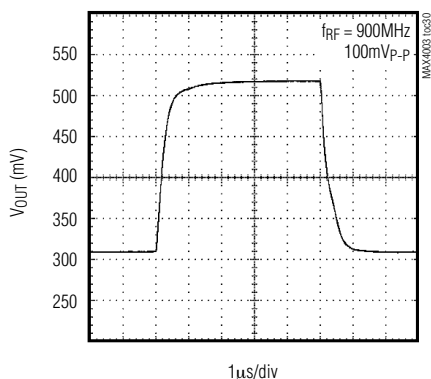
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vs. SUPPLY VOLTAGE**



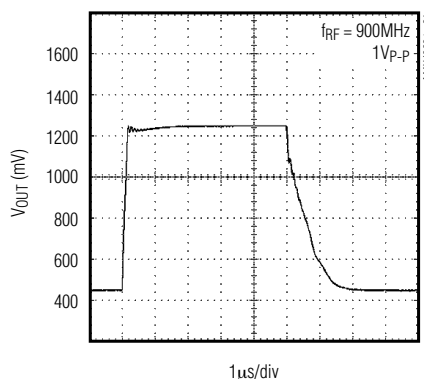
**SMALL-SIGNAL STEP RESPONSE
($C_{CLPF} = 150pF$)**



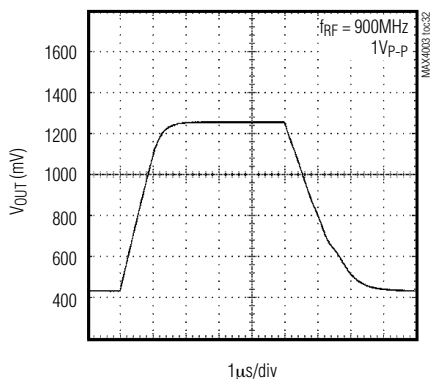
**SMALL-SIGNAL STEP RESPONSE
($C_{CLPF} = 1000pF$)**



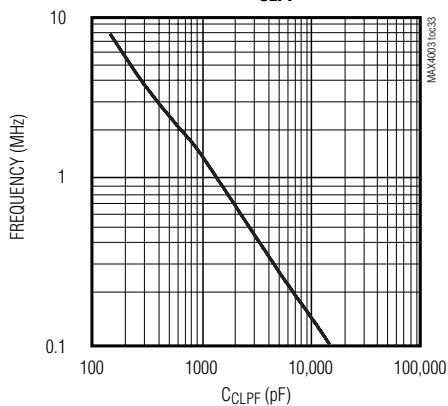
**LARGE-SIGNAL STEP RESPONSE
($C_{CLPF} = 150pF$)**



**LARGE-SIGNAL STEP RESPONSE
($C_{CLPF} = 1000pF$)**



**SMALL-SIGNAL BANDWIDTH
vs. C_{CLPF}**



100MHz to 2500MHz, 45dB RF Detector in a UCSP

Pin Description

PIN		NAME	DESCRIPTION
μ MAX/ Thin QFN	UCSP		
1	A1	RFIN	RF Input. Requires off-chip 50 Ω impedance match.
2	A2	SHDN	Shutdown Input. A logic LOW on SHDN shuts down the entire IC.
3, 5	A3, C3	GND	Ground. Connect to PC board ground plane.
4	B3	CLPF	Lowpass Filter Connection. Connect external capacitor between CLPF and GND to set the control-loop bandwidth.
6	—	N.C.	No Connection. Leave this pin unconnected or connect to GND.
7	C2	OUT	Detector Output. Connect this buffer output to baseband ADC.
8	B1, C1	VCC	Supply Voltage. Bypass with capacitor as close to the pin as possible. The bypass capacitor must not share its ground vias with any other branches.

Detailed Description

The MAX4003 logarithmic amplifier comprises four main amplifier/limiter stages, each with a small-signal gain of 10dB. The output stage of each amplifier/limiter stage is applied to a full-wave rectifier (detector). A detector stage also precedes the first stage. In total, five detectors, each separated by 10dB, comprise the logarithmic amplifier strip (see *Functional Diagram*).

A portion of the PA output power is coupled into RFIN of the logarithmic amplifier detector through a directional coupler, and is applied to the logarithmic amplifier strip. Each detector stage generates a rectified current, and these currents are summed to form a logarithmic function. The detected output is applied to a high-gain transconductance (g_m) stage, which is buffered and then applied to OUT. OUT is applied to an ADC typically found in the baseband IC which, in turn, controls the

PA biasing with its DAC output (Figure 1).

In a control loop, the detector output voltage range is approximately 0.36V for the minimum input signal, -45dBm, to 1.45V at the maximum input range, 0dBm. The logarithmic intercept of the detector output with respect to the RF input can be obtained by drawing a best fit line of the Output Voltage vs. RF Input Power graph. The logarithmic slope is defined as the change in the detector output vs. the change in RF input. The MAX4003 slope at low frequencies is approximately 25.5mV/dB. Variation in temperature and supply voltage does not alter the slope significantly, as shown in the *Typical Operating Characteristics*.

Applications Information

Filter Capacitor and Transient Response

In general, the choice of filter only partially determines the time-domain response of a PA detector loop. However, some simple conventions may be applied to discuss transient response. A large filter capacitor, CCLPF, dominates time-domain response, but the loop bandwidth remains a factor of the PA gain-control range (see *Typical Operating Characteristics*). The bandwidth is maximized at power outputs near the center of the PA's range and minimized at the low and high power levels, when the slope of the gain control curve is lowest.

A smaller valued CCLPF results in an increased-loop bandwidth inversely proportional to the capacitor value. Inherent phase lag in the PA's control path, usually caused by parasitics at the OUT pin, ultimately results in the addition of complex poles in the AC loop equation. To avoid this secondary effect, experimentally determine the lowest usable CCLPF for the power ampli-

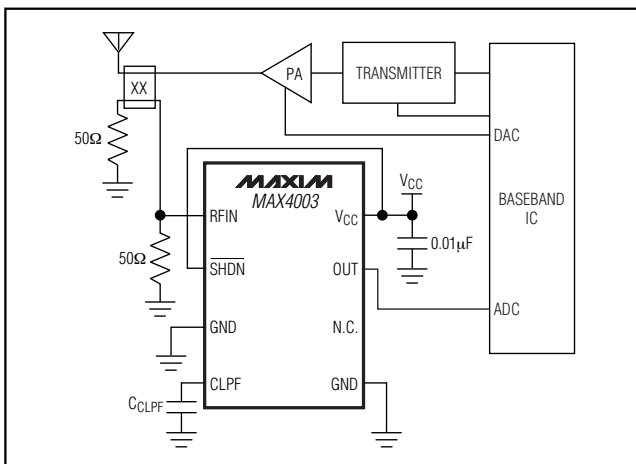


Figure 1. MAX4003 Typical Application Circuit

100MHz to 2500MHz, 45dB RF Detector in a UCSP

fier of interest. This requires full consideration of the intricacies of the PA detector control function. The worst-case condition, where the PA output is smallest (gain function is steepest), should be used because the PA control function is nonlinear. An additional zero can be added to improve loop dynamics by placing a resistor in series with CCLPF.

Waveform Considerations

Although the input level of the MAX4003 is specified in dBm, the logarithmic amplifier actually responds to rectified voltage signals rather than a true RMS power. It is important to realize that input signals with identical root-mean-square power but with unique waveforms result in different logarithmic outputs.

Differing signal waveforms result in either an upward or downward shift in the logarithmic intercept. However, the logarithmic slope remains the same.

Layout Considerations

As with any RF circuit, the MAX4003 circuit layout affects performance. To ensure maximum power transfer between 50Ω sources and the MAX4003 input, suitable matching networks should be implemented. The VCC input should be bypassed as close as possible to the device with multiple vias connecting the capacitor to the ground plane.

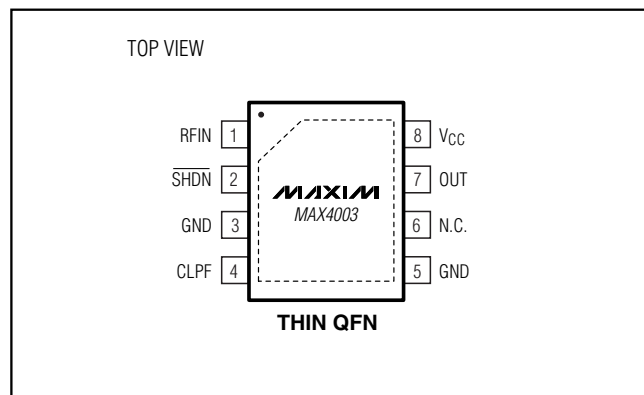
UCSP Reliability

The UCSP represents a unique package that greatly reduces board space compared to other packages. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP. This form factor may not perform equally to a packaged product through traditional mechanical reliability tests. Performance through operating life test and moisture resistance remains uncompromised as it is primarily determined by the wafer fabrication process. Mechanical stress performance is a greater consideration for a UCSP. UCSP solder joint contact integrity must be considered since the package is attached through direct solder contact to the user's PC board. Testing done to characterize the UCSP reliability performance shows that it can perform reliably through environmental stresses. Results of environmental stress tests and additional usage data and recommendations are detailed in the UCSP application note found on Maxim's website, www.maxim-ic.com.

Chip Information

TRANSISTOR COUNT: 358

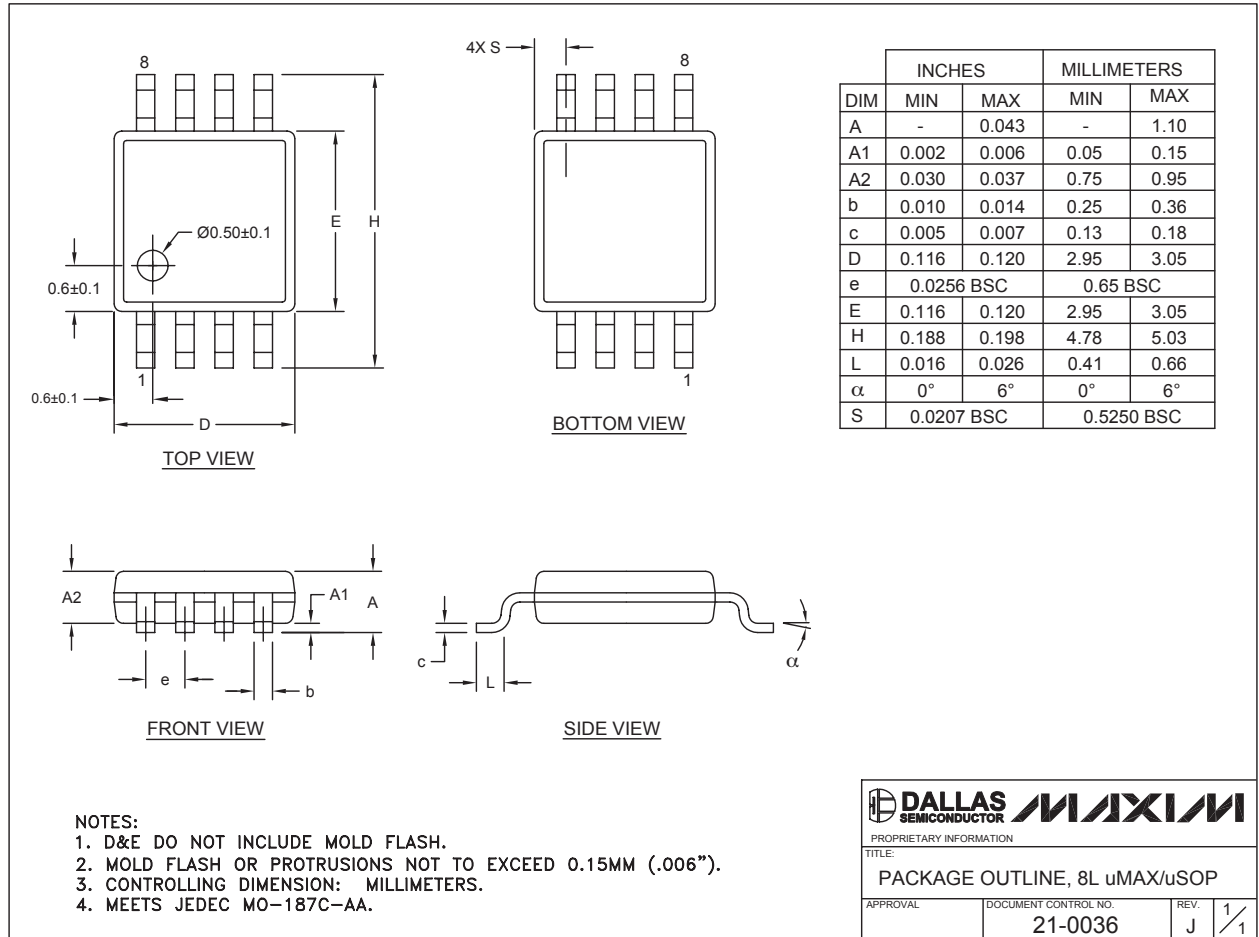
Pin Configurations (continued)



100MHz to 2500MHz, 45dB RF Detector in a UCSP

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

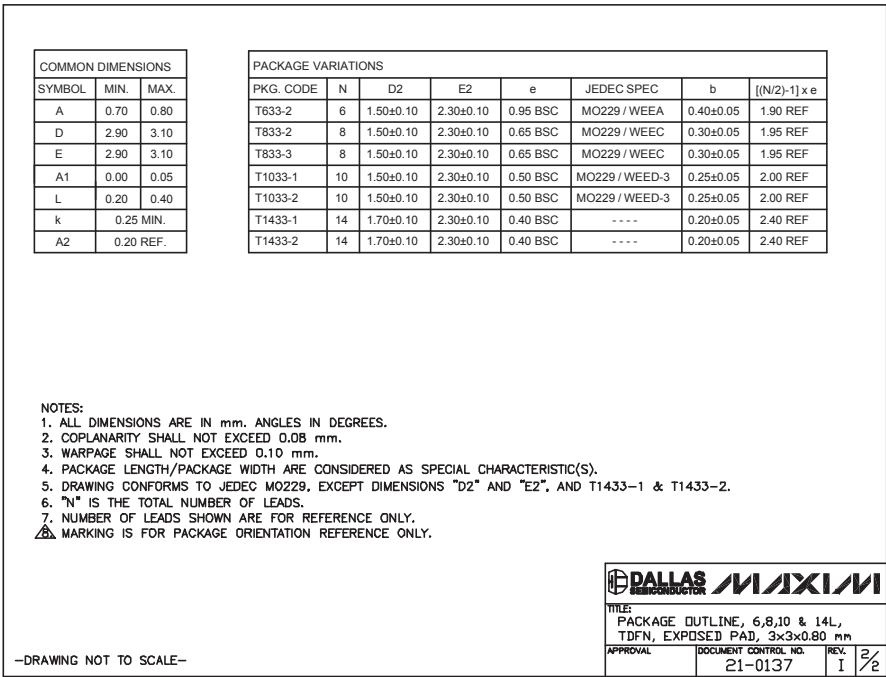
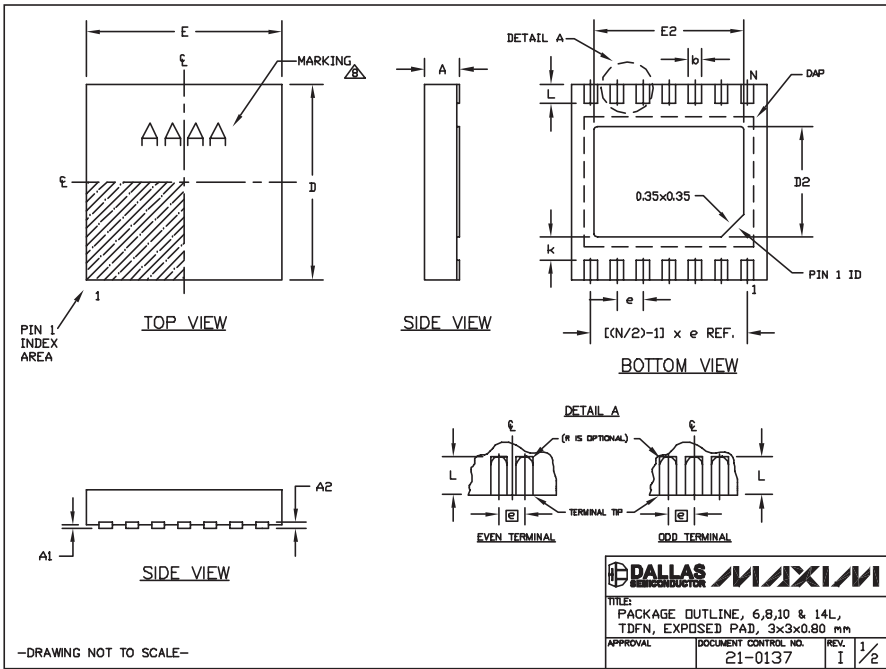


8LUMAXDEPS

100MHz to 2500MHz, 45dB RF Detector in a UCSP

Package Information (continued)

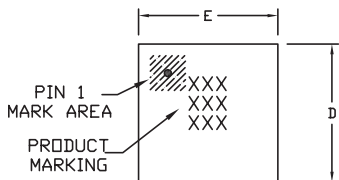
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



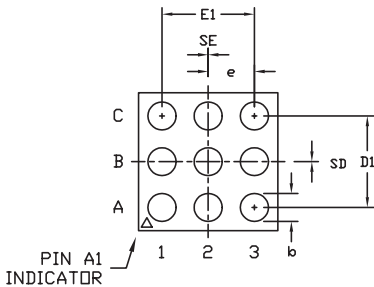
100MHz to 2500MHz, 45dB RF Detector in a UCSP

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



TOP VIEW

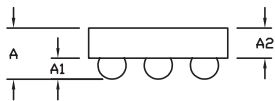


BOTTOM VIEW

COMMON DIMENSIONS	
A	0.62±0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	∅0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3
B9-7	1.52±0.05	1.52±0.05	A2, B1, B2, B3, C2

- NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



SIDE VIEW

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE, 3x3 UCSP			
APPROVAL	DOCUMENT CONTROL NO. 21-0093	REV. K	1/1

9LUCSP, 3x3.EPS

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