

# NTR3C21NZ

## Power MOSFET

20 V, 3.6 A, Single N-Channel  
2.4 x 2.9 x 1.0 mm SOT-23 Package

### Features

- Advanced Trench Technology
- Ultra-Low  $R_{DS(on)}$  in SOT-23 Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Power Load Switch
- Power Management

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	20	V
Gate-to-Source Voltage			$V_{GS}$	$\pm 8$	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	$I_D$	3.6	A
		$T_A = 85^{\circ}\text{C}$		2.6	
	$t \leq 5\text{ s}$	$T_A = 25^{\circ}\text{C}$		6.5	
Power Dissipation (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	$P_D$	0.47	W
	$t \leq 5\text{ s}$			1.56	
Pulsed Drain Current	$t_p = 10\text{ }\mu\text{s}$		$I_{DM}$	13.2	A
Operating Junction and Storage Temperature			$T_J$ , $T_{STG}$	-55 to 150	$^{\circ}\text{C}$
Source Current (Body Diode) (Note 2)			$I_S$	2.2	A
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)			$T_L$	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	264	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 5 \text{ s}$ (Note 1)	$R_{\theta JA}$	80	

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).
2. Pulse Test: pulse width  $\leq 300 \text{ ms}$ , duty cycle  $\leq 2\%$ .

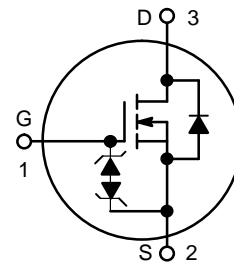


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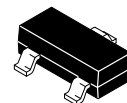
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$V_{(BR)DS}$	$R_{DS(on)}$ Max	$I_D$ MAX
20 V	24 m $\Omega$ @ 4.5 V	3.6 A
	26 m $\Omega$ @ 3.7 V	
	29 m $\Omega$ @ 3.3 V	
	33 m $\Omega$ @ 2.5 V	
	55 m $\Omega$ @ 1.8 V	

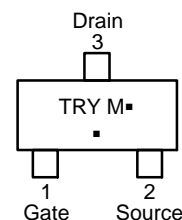
### N-Channel MOSFET



### MARKING DIAGRAM & PIN ASSIGNMENT



SOT-23  
CASE 318  
STYLE 21



TRY = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
NTR3C21NZT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
NTR3C21NZT5G	SOT-23 (Pb-Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTR3C21NZ

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA, ref to 25°C		21.6		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 20 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 85°C		5.0	μA
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±8 V			±10	μA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	0.45		1.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			2.7		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A		18	24	mΩ
		V <sub>GS</sub> = 3.7 V, I <sub>D</sub> = 4 A		18.5	26	
		V <sub>GS</sub> = 3.3 V, I <sub>D</sub> = 3 A		19	29	
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 2 A		20	33	
		V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 1 A		25	55	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 3 A		20		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 16 V		1540		pF
Output Capacitance	C <sub>oss</sub>			105		
Reverse Transfer Capacitance	C <sub>rss</sub>			86		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 16 V, I <sub>D</sub> = 5 A		17.8		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			2.1		
Gate-to-Source Charge	Q <sub>GS</sub>			3.0		
Gate-to-Drain Charge	Q <sub>GD</sub>			0.8		

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 16 V, I <sub>D</sub> = 5 A, R <sub>G</sub> = 6.0 Ω		7.0		ns
Rise Time	t <sub>r</sub>			14		
Turn-Off Delay Time	t <sub>d(off)</sub>			420		
Fall Time	t <sub>f</sub>			4670		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.0 A	T <sub>J</sub> = 25°C		0.7	1.0	V
			T <sub>J</sub> = 125°C		0.56		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 ms, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

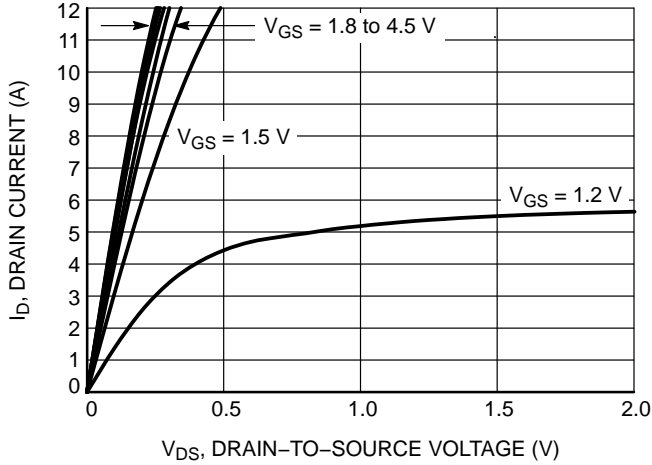


Figure 1. On-Region Characteristics

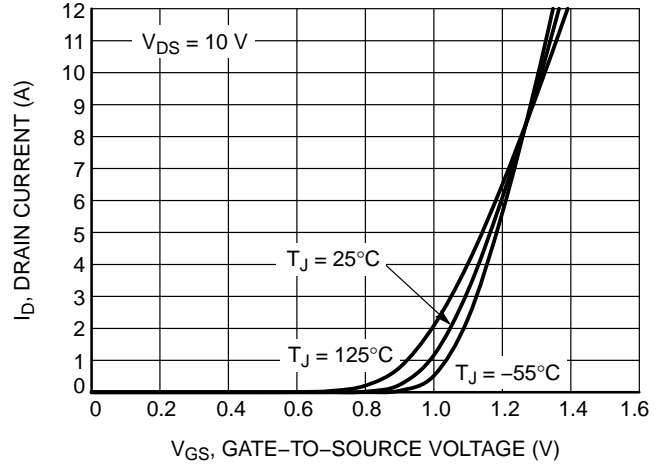


Figure 2. Transfer Characteristics

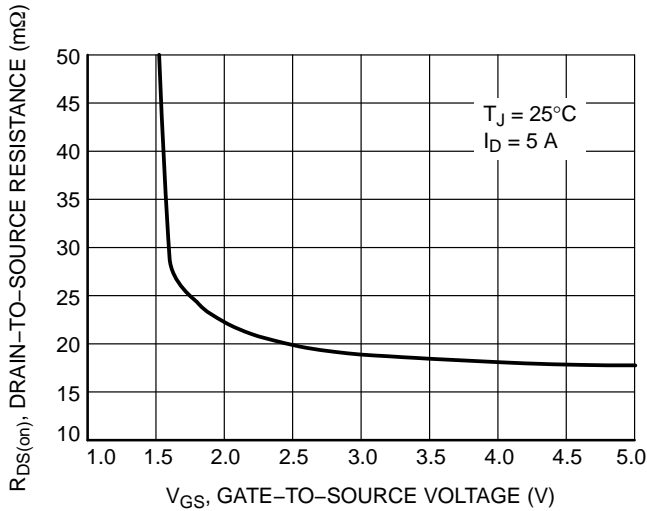


Figure 3. On-Resistance vs. Gate-to-Source Voltage

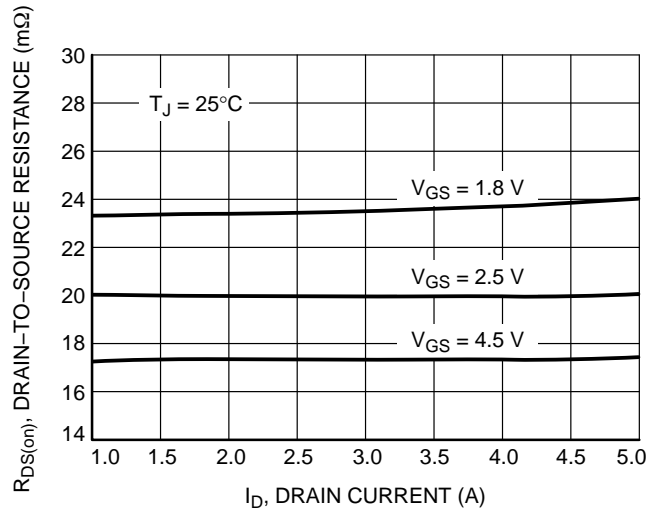


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

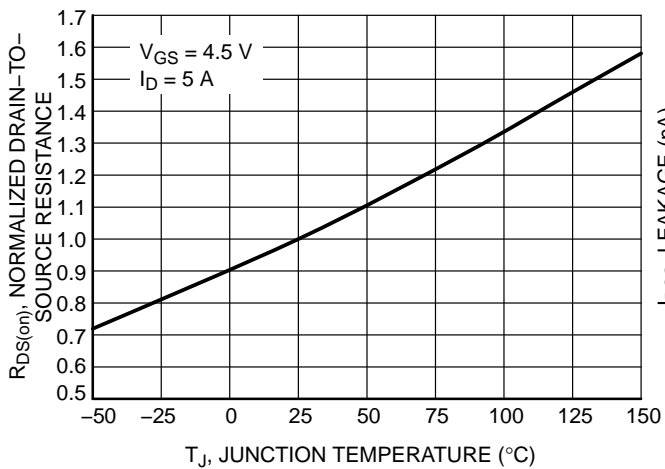


Figure 5. On-Resistance Variation with Temperature

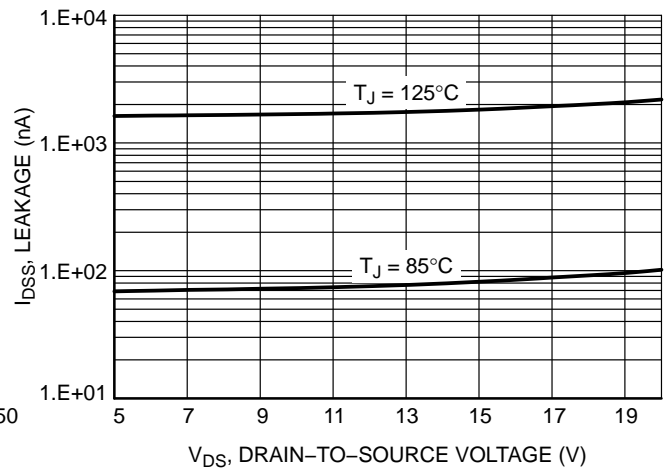


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTR3C21NZ

## TYPICAL CHARACTERISTICS

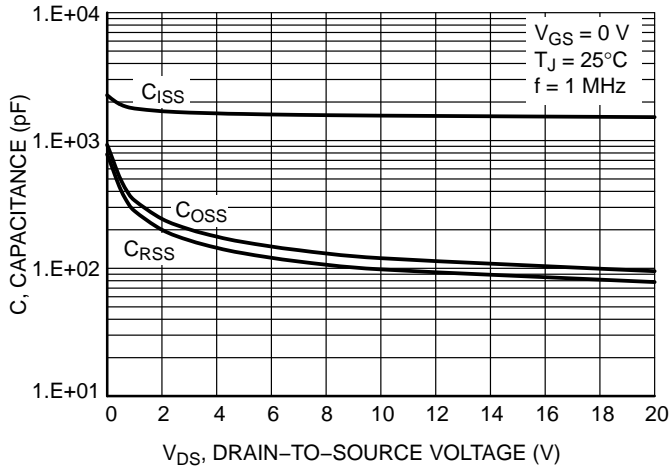


Figure 7. Capacitance Variation

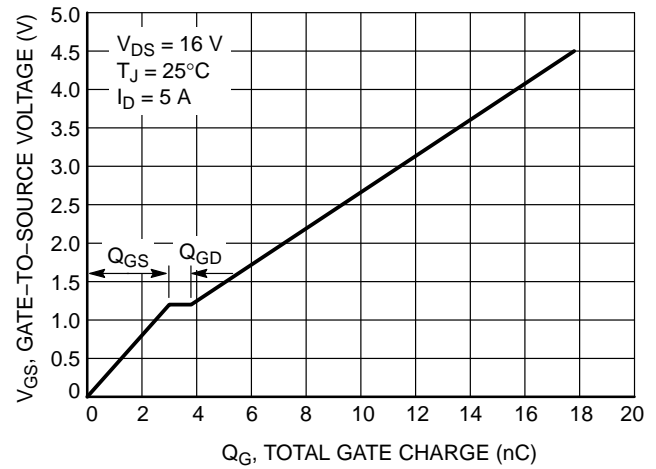


Figure 8. Gate-to-Source vs. Total Charge

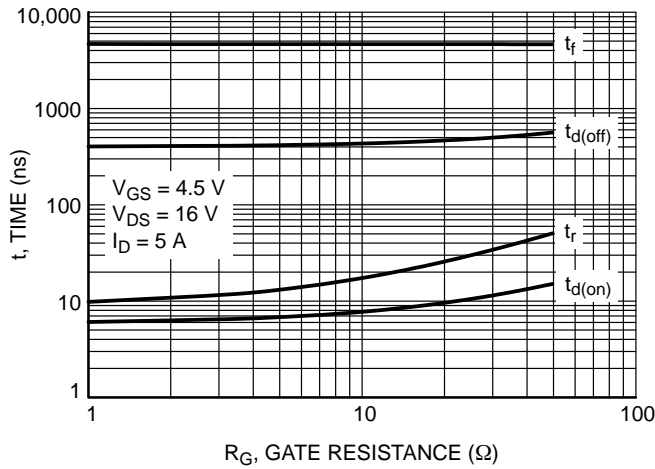


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

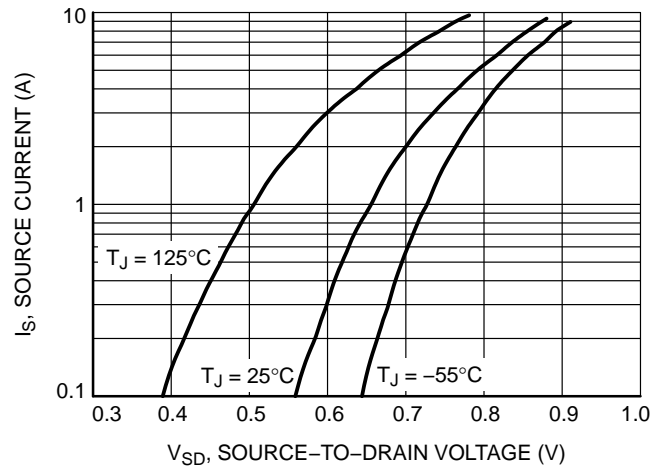


Figure 10. Diode Forward Voltage vs. Current

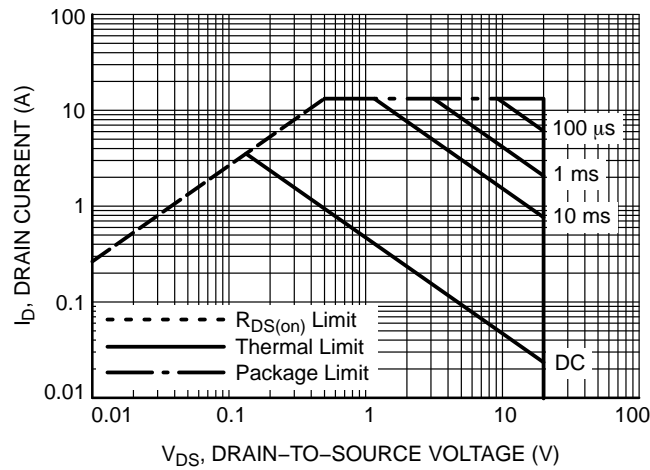


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NTR3C21NZ

## TYPICAL CHARACTERISTICS

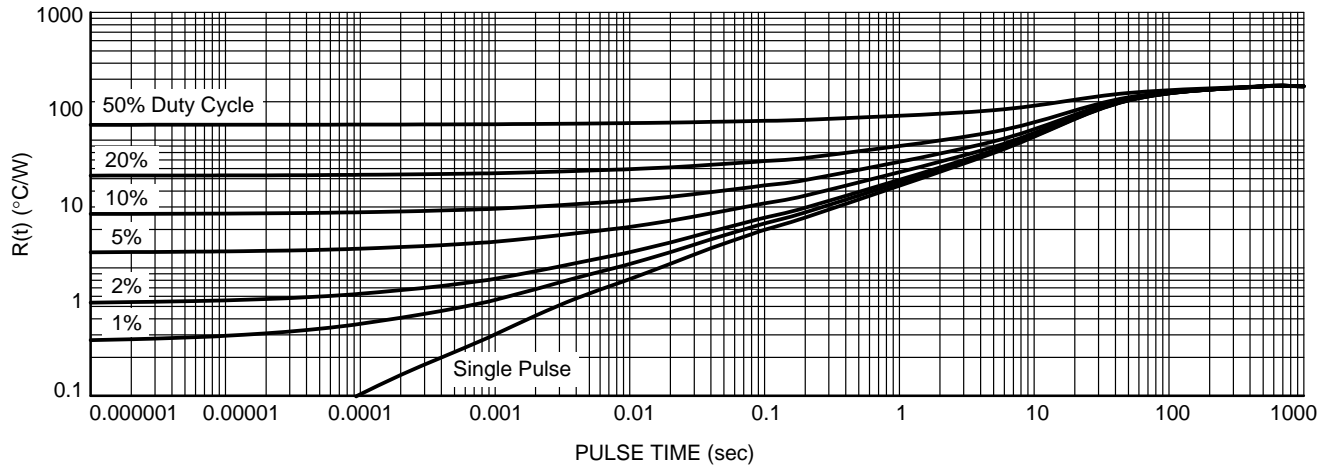
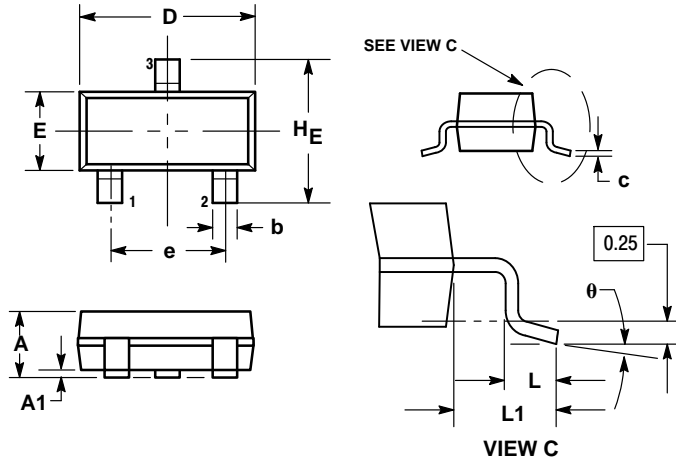


Figure 12. FET Thermal Response

# NTR3C21NZ

## PACKAGE DIMENSIONS

### SOT-23 (TO-236) CASE 318-08 ISSUE AP



#### NOTES:

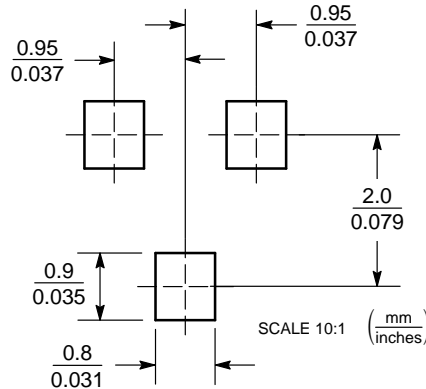
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	—	10°	0°	—	10°


#### STYLE 21:

1. GATE
2. SOURCE
3. DRAIN

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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