PWM LED Driver and Boost, Flyback and SEPIC Controller

FEATURES

- **True Color PWM™ Delivers Constant Color with 3000:1 Dimming Ratio**
- **Fully Integrated Load FET Driver for PWM Dimming Control of High Power LEDs**
- **100:1 Dimming from Analog Inputs**
- **Wide FB Voltage Range: 0V to 1.23V**
- **Constant Current or Constant Voltage Regulation**
- Low Shutdown Current: I_Q = 20µA
- 1% 1.23V Internal Voltage Reference
- 2% RUN Pin Threshold with 100mV Hysteresis
- Programmable Operating Frequency (20kHz to 1MHz) with One External Resistor
- Synchronizable to an External Clock Up to 1.3f_{OSC}
- Internal 7V Low Dropout Voltage Regulator
- Programmable Output Overvoltage Protection
- Programmable Soft-Start
- Can be Used in a No R_{SENSE}™ Mode for V_{DS} < 36V
- 16-Lead DFN and TSSOP Packages

APPLICATIONS

- High Voltage LED Arrays
- Telecom Power Supplies
- 42V Automotive Systems
- 24V Industrial Controls
- IP Phone Power Supplies

DESCRIPTION

The LTC®3783 is a current mode LED driver and boost, flyback and SEPIC controller that drives both an N-channel power MOSFET and an N-channel load PWM switch. When using an external load switch, the PWMIN input not only drives PWMOUT, but also enables controller GATE switching and error amplifier operation, allowing the controller to store load current information while PWMIN is low. This feature (patent pending) provides extremely fast, true PWM load switching with no transient overvoltage or undervoltage issues; LED dimming ratios of 3000:1 can be achieved digitally, avoiding the color shift normally associated with LED current dimming. The FBP pin allows analog dimming of load current, further increasing the effective dimming ratio by 100:1 over PWM alone.

In applications where output load current must be returned to V_{IN}, optional constant current/constant voltage regulation controls either output (or input) current or output voltage and provides a limit for the other. I_{LIM} provides a 10:1 analog dimming ratio.

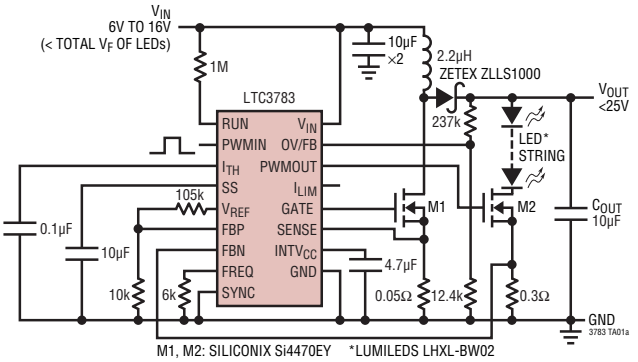
For low- to medium-power applications, No R_{SENSE} mode can utilize the power MOSFET's on-resistance to eliminate the current-sense resistor, thereby maximizing efficiency.

The IC's operating frequency can be set with an external resistor over a 20kHz to 1MHz range and can be synchronized to an external clock using the SYNC pin.

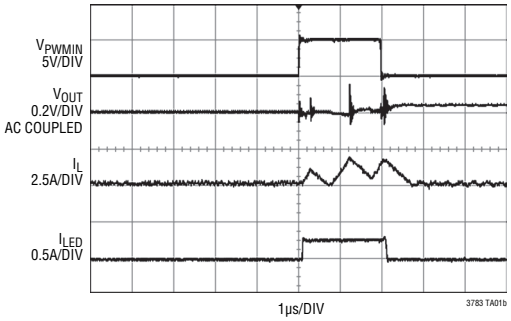
The LTC3783 is available in the 16-lead DFN and TSSOP packages.

TYPICAL APPLICATION

350mA PWM LED Boost Application



Typical Waveforms

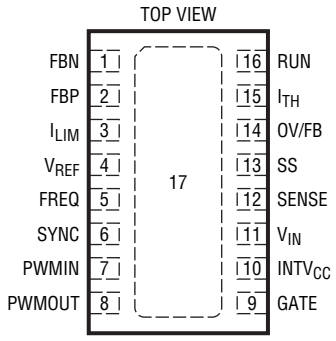


ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}, SENSE, FBP, FBN Voltages ..... –0.3V to 42V
$INTV_{CC}$ Voltage..... –0.3V to 9V
$INTV_{CC}$ Output Current..... 75mA
GATE Output Current..... 50mA (RMS)
PWMOUT Output Current..... 25mA (RMS)
V_{REF} Ouput Current..... 1mA
GATE, PWMOUT Voltages .....–0.3V to (V_{INTVCC} + 0.3V)
I_{TH}, I_{LIM}, SS Voltages..... –0.3V to 2.7V
RUN, SYNC, PWMIN Voltages..... –0.3V to 7V
FREQ, V_{REF}, OV/FB Voltages..... –0.3V to 1.5V

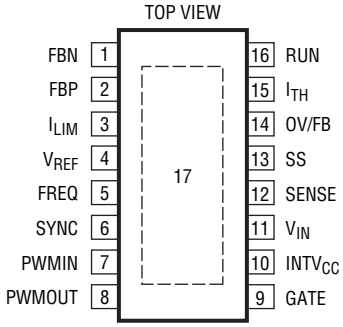
Operating Temperature Range (Note 2)
LTC3783E..... –40°C to 85°C
LTC3783I..... –40°C to 125°C
Junction Temperature (Note 3) ..... –40°C to 125°C
Storage Temperature Range
DFN Package..... –65°C to 125°C
TSSOP Package..... –65°C to 150°C
Lead Temperature (Soldering, 10sec)
TSSOP Package..... 300°C

PIN CONFIGURATION



DHD PACKAGE
16-LEAD (5mm × 4mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3783EDHD#PBF	LTC3783EDHD#TRPBF	3783	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 85°C
LTC3783IDHD#PBF	LTC3783IDHD#TRPBF	3783	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 125°C
LTC3783EFE#PBF	LTC3783EFE#TRPBF	3783EFE	16-Lead Plastic TSSOP	–40°C to 85°C
LTC3783IFE#PBF	LTC3783IFE#TRPBF	3783IFE	16-Lead Plastic TSSOP	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3783EDHD	LTC3783EDHD#TR	3783	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 85°C
LTC3783IDHD	LTC3783IDHD#TR	3783	16-Lead (5mm × 4mm) Plastic DFN	–40°C to 125°C
LTC3783EFE	LTC3783EFE#TR	3783IFE	16-Lead Plastic TSSOP	–40°C to 85°C
LTC3783IFE	LTC3783IFE#TR	3783IFE	16-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 12V, V_{RUN} = 1.5V, V_{SYNC} = 0V, V_{FBP} = V_{REF}, R_T = 20k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop/Whole System							
V_{IN}	Input Voltage Range			3		36	V
I_Q	Input Voltage Supply Current Continuous Mode Shutdown Mode	(Note 4) $V_{OV/FB}$ = 1.5V, V_{ITH} = 0.75V V_{RUN} = 0V			 1.5 20		 mA µA
V_{RUN}^+	Rising RUN Input Threshold Voltage				1.348		V
V_{RUN}^-	Falling RUN Input Threshold Voltage			1.223	1.248	1.273	V
$V_{RUN(HYST)}$	RUN Pin Input Threshold Hysteresis				100		mV
I_{RUN}	RUN Pin Input Current				5		nA
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold			125	150	180	mV
$I_{SENSE(ON)}$	SENSE Pin Current (GATE High)	V_{SENSE} = 0V			70		µA
$I_{SENSE(OFF)}$	SENSE Pin Current (GATE Low)	V_{SENSE} = 36V			0.2		µA
I_{SS}	Soft-Start Pin Output Current	V_{SS} = 0V			-50		µA
Voltage/Temperature Reference							
V_{REF}	Reference Voltage		 ●	1.218 1.212	1.230	1.242 1.248	V V
I_{REF}	Max Reference Pin Output Current			0.5			mA
$\Delta V_{REF}/\Delta V_{IN}$	Reference Voltage Line Regulation	3V ≤ V_{IN} ≤ 36V			0.002	0.02	%/V
$\Delta V_{REF}/\Delta I_{REF}$	Reference Voltage Load Regulation	0mA ≤ I_{REF} ≤ 0.5mA			0.2	1.0	%/mA
T_{MAX}	Overtemperature SD Threshold Rising				165		°C
T_{HYST}	Overtemperature Hysteresis				25		°C
Error Amplifier							
$I_{OV/FB}$	OV/FB Pin Input Current				18	60	nA
$\Delta V_{OV/FB(OV)}$	OV/FB Overvoltage Lockout Threshold	$V_{OV/FB(OV)}$ – $V_{OV/FB(NOM)}$ in %, V_{FBP} ≤ V_{REF}			7		%
$V_{OV/FB(FB)}$	OV/FB Pin Regulation Voltage	2.5V < V_{FBP} < 36V		1.212	1.230	1.248	V
I_{FBP}, I_{FBN}	Error Amplifier Input Current	0V ≤ V_{FBP} ≤ V_{REF} 2.5V < V_{FBP} < 36V			–0.4 50		µA µA
$V_{FBP} – V_{FBN}$	Error Amplifier Offset Voltage (Note 5)	0V ≤ V_{FBP} ≤ V_{REF} 2.5V < V_{FBP} ≤ 36V (V_{ILIM} = V_{REF}) 2.5V < V_{FBP} ≤ 36V (V_{ILIM} = 0.123V)		–3	 100 10	3	mV mV mV
g_m	Error Amplifier Transconductance	V_{FBP} ≤ V_{REF} 2.5V < V_{FBP} < 36V			1.7 14		mmho mmho
A_{VOL}	Error Amplifier Open-Loop Gain			500			V/V
Oscillator							
f_{OSC}	Oscillator Frequency Oscillator Frequency Range	R_{FREQ} = 20kΩ		250 20	300	350 1000	kHz kHz
D_{MAX}	Maximum Duty Cycle			85	90	97	%
f_{SYNC}/f_{OSC}	Recommended Max SYNC Freq Ratio	f_{OSC} = 300kHz (Note 6)			1.25	1.3	
$t_{SYNC(MIN)}$	SYNC Minimum Input Pulse Width	V_{SYNC} = 0V to 5V			25		ns
$t_{SYNC(MAX)}$	SYNC Maximum Input Pulse Width	V_{SYNC} = 0V to 5V			$0.8/f_{OSC}$		ns
$V_{IH(SYNC)}$	SYNC Input Voltage High Level			1.2			V
$V_{HYST(SYNC)}$	SYNC Input Voltage Hysteresis				0.5		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 12V, V_{RUN} = 1.5V, V_{SYNC} = 0V, V_{FBP} = V_{REF} , R_T = 20k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{SYNC}	SYNC Input Pull-Down Resistance				100		kΩ
$t_{ON(MIN)}$	Minimum On-Time	With Sense Resistor, 10mV Overdrive No R_{SENSE} Mode			170 300		ns ns
Low Dropout Regulator							
V_{INTVCC}	$INTV_{CC}$ Regulator Output Voltage	$V_{OV/FB}$ = 1.5V	●	6.5	7	7.5	V
UVLO	$INTV_{CC}$ Undervoltage Lockout Thresholds	Rising $INTV_{CC}$ Falling $INTV_{CC}$ Hysteresis		 1.8	2.3 2.1 0.2	2.5	V V V
$\frac{\Delta V_{INTVCC}}{\Delta V_{IN}}$	$INTV_{CC}$ Line Regulation	12V ≤ V_{IN} ≤ 36V			2	6	mV/V
$\Delta V_{LDO(LOAD)}$	$INTV_{CC}$ Load Regulation	0 ≤ I_{INTVCC} ≤ 10mA		–1	–0.1		%
$V_{DROPOUT}$	$INTV_{CC}$ Dropout Voltage	V_{IN} = 7V, I_{INTVCC} = 10mA			300	500	mV
$I_{INTVCC(SD)}$	Bootstrap Mode $INTV_{CC}$ Supply Current in Shutdown	V_{SENSE} = 0V V_{SENSE} = 7V			25 15		µA µA
GATE/PWMOUT Drivers							
$t_{r(GATE)}$	GATE Driver Output Rise Time	C_L = 3300pF (Note 7)			15		ns
$t_{f(GATE)}$	GATE Driver Output Fall Time	C_L = 3300pF (Note 7)			8		ns
$I_{PK(GATE,RISE)}$	GATE Driver Peak Current Sourcing	V_{GATE} = 0V			0.5		A
$I_{PK(GATE,FALL)}$	GATE Driver Peak Current Sinking	V_{GATE} = 7V			1		A
V_{PWMIN}	PWMIN Pin Input Threshold Voltages	Rising PWMIN Falling PWMIN Hysteresis			1.6 0.8 0.8		V V V
R_{PWMIN}	PWMIN Input Pull-Up Resistance				100		kΩ
$t_{r(PWMOUT)}$	PWMOUT Driver Output Rise Time	C_L = 3300pF (Note 7)			30		ns
$t_{f(PWMOUT)}$	PWMOUT Driver Output Fall Time	C_L = 3300pF (Note 7)			16		ns
$I_{PK(PWMOUT,RISE)}$	PWMOUT Driver Peak Current Sourcing	V_{PWMOUT} = 0V			0.25		A
$I_{PK(PWMOUT,FALL)}$	PWMOUT Driver Peak Current Sinking	V_{PWMOUT} = 7V			0.50		A

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3783E is guaranteed to meet performance specifications over the 0°C to 85°C operating temperature range. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3783I is guaranteed to meet performance specifications over the full –40°C to 125°C operating temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet 43°C/W)$ for the DFN

$T_J = T_A + (P_D \bullet 38°C/W)$ for the TSSOP

Note 4: The dynamic input supply current is higher due to power MOSFET gate charging ($Q_G \bullet f_{OSC}$). See Operation section.

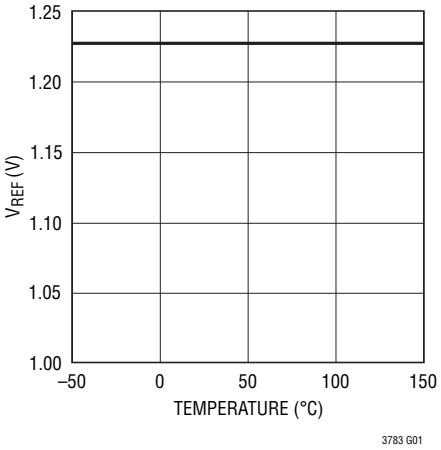
Note 5: The LTC3783 is tested in a feedback loop which servos V_{FBN} to V_{FBP} = V_{VREF} with the I_{TH} pin forced to the midpoint of its voltage range (0.3V ≤ V_{ITH} ≤ 1.2V; midpoint = 0.75V).

Note 6: In a synchronized application, the internal slope compensation is increased by 25%. Synchronizing to a significantly higher ratio will reduce the effective amount of slope compensation, which could result in sub-harmonic oscillation for duty cycles greater than 50%

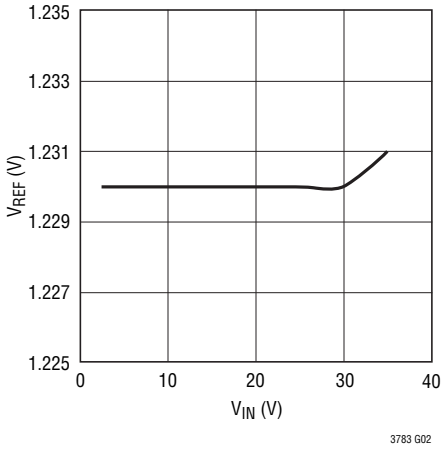
Note 7: Rise and fall times are measured at 10% and 90% levels.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

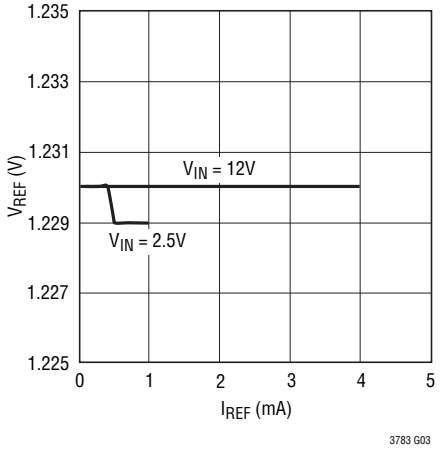
V_{REF} vs Temperature



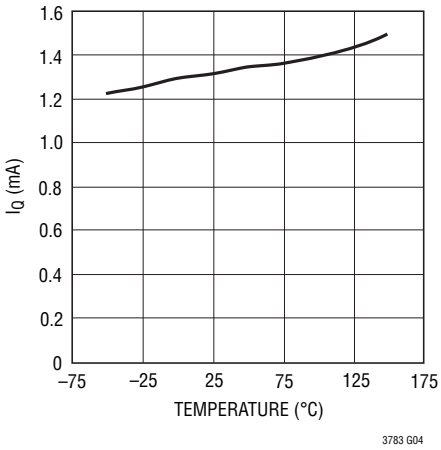
V_{REF} Line Regulation



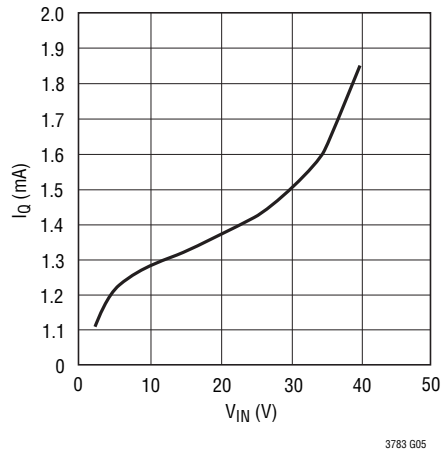
V_{REF} Load Regulation



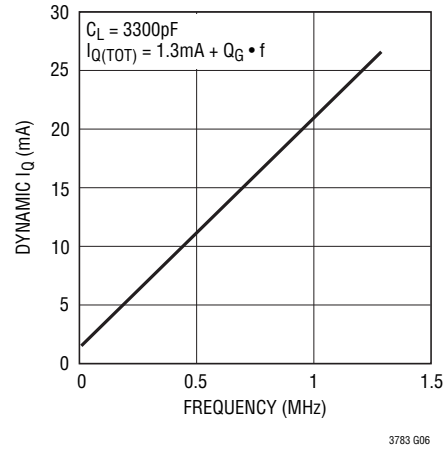
I_Q vs Temperature (PWMIN Low)



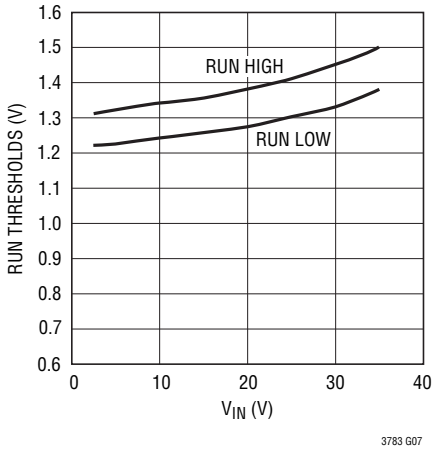
I_Q vs V_{IN} (PWMIN Low)



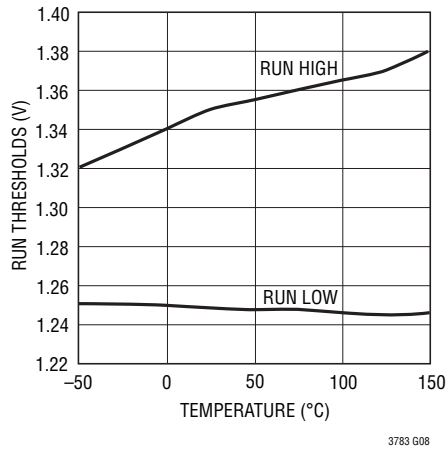
Dynamic I_Q vs Frequency



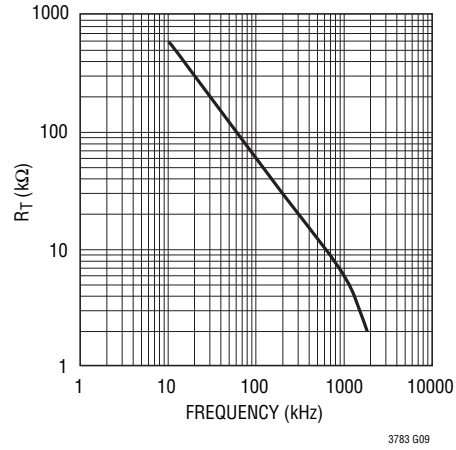
RUN Thresholds vs V_{IN}



RUN Thresholds vs Temperature

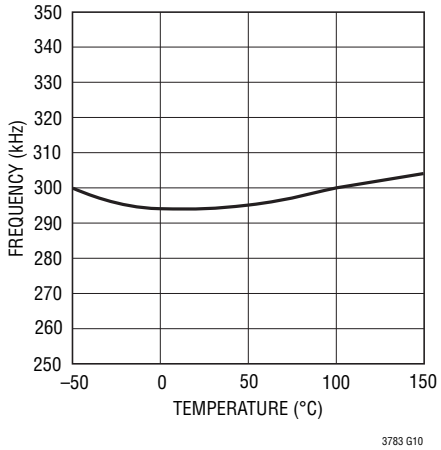


R_T vs Frequency



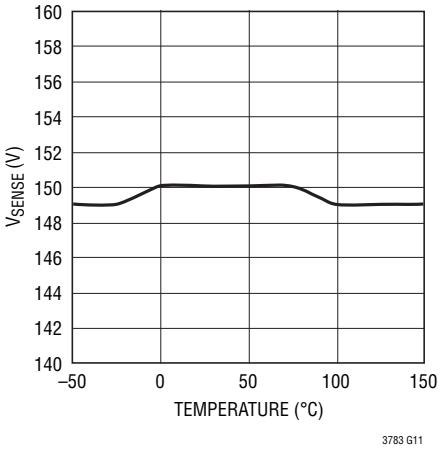
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

Frequency vs Temperature



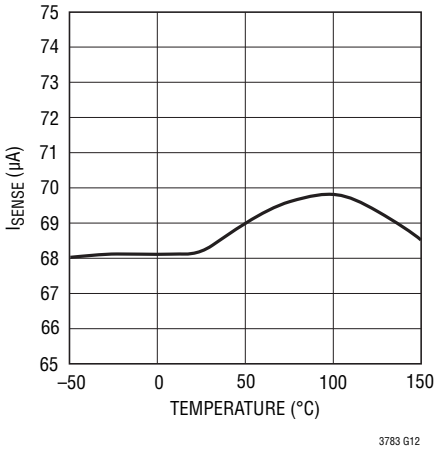
3783 G10

Maximum V_{SENSE} vs Temperature



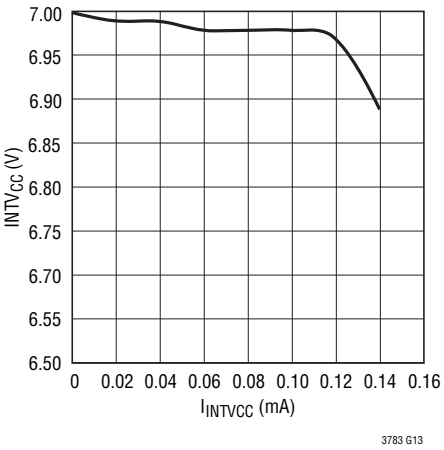
3783 G11

I_{SENSE} vs Temperature



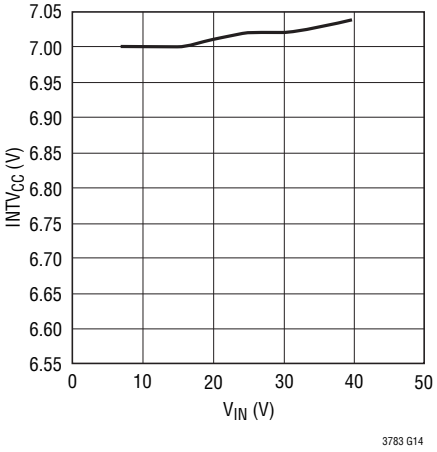
3783 G12

$INTV_{CC}$ Load Regulation



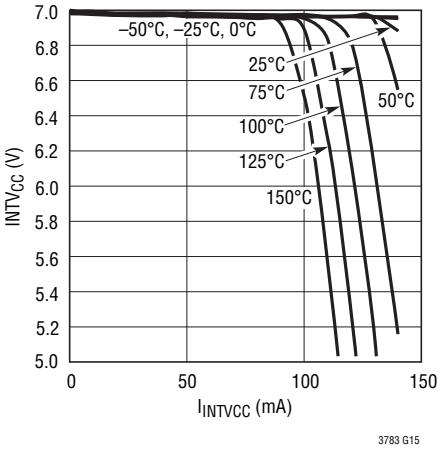
3783 G13

$INTV_{CC}$ Line Regulation



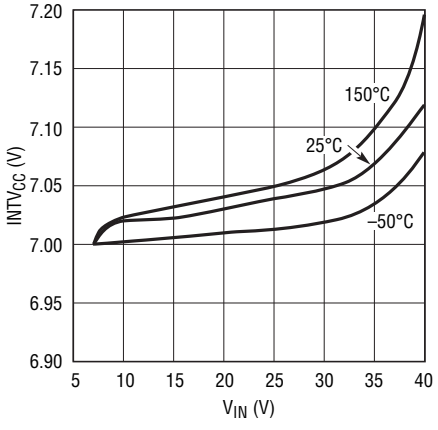
3783 G14

$INTV_{CC}$ Load Regulation Over Temperature



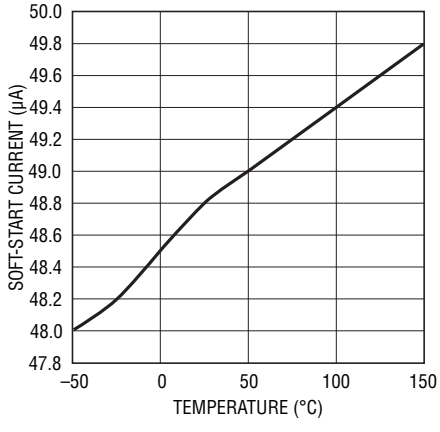
3783 G15

$INTV_{CC}$ Line Regulation vs Temperature



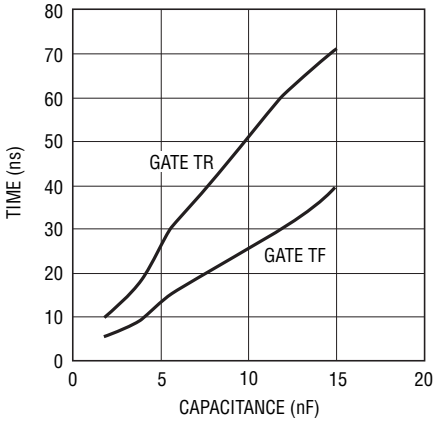
3783 G16

I_{SS} Soft-Start Current vs Temperature



3783 G17

Gate Rise/Fall Time vs Capacitance



3783 G18

PIN FUNCTIONS

FBN (Pin 1): Error Amplifier Inverting Input/Negative Current Sense Pin. In voltage mode ($V_{FBP} \leq V_{VREF}$), this pin senses feedback voltage from either the external resistor divider across V_{OUT} for output voltage regulation, or the grounded sense resistor under the load for output current regulation. In constant current/constant voltage mode ($V_{FBP} > 2.5V$), connect this pin to the negative side of the current-regulating resistor. Nominal voltage for this pin in regulation is either V_{FBP} or ($V_{FBP} – 100mV$) for $V_{ILIM} = 1.23V$, depending on operational mode (voltage or constant current/constant voltage) set by the voltage at V_{FBP}.

FBP (Pin 2): Error Amplifier Noninverting Input/Positive Current Sense Pin. This pin voltage determines the control loop's feedback mode (voltage or constant current/constant voltage), the threshold of which is approximately 2V. In voltage mode ($V_{FBP} \leq V_{REF}$), this pin represents the desired voltage which the regulated loop will cause FBN to follow. In constant current/constant voltage mode ($V_{FBP} > 2.5V$), connect this pin to the positive side of the load current-sensing resistor. The acceptable input ranges for this pin are 0V to 1.23V (voltage mode) and 2.5V to 36V (constant current/constant voltage mode).

I_{LIM}(Pin 3): Current Limit Pin. Sets current sense resistor offset voltage ($V_{FBP} – V_{FBN}$) in constant current mode regulation (i.e., when $V_{FBP} > 2.5V$). Offset voltage is 100mV when $V_{ILIM} = 1.23V$ and decreases proportionally with V_{ILIM}. Nominal voltage range for this pin is 0.1V to 1.23V.

V_{REF} (Pin 4): Reference Voltage Pin. Provides a buffered version of the internal bandgap voltage, which can be connected to FBP either directly or with attenuation. Nominal voltage for this pin is 1.23V. This pin should never be bypassed by a capacitor to GND. Instead, a 10k resistor to GND should be used to lower pin impedance in noisy systems.

FREQ (Pin 5): A resistor from the FREQ pin to ground programs the operating frequency of the chip. The nominal voltage at the FREQ pin is 0.615V.

SYNC (Pin 6): This input allows for synchronizing the operating frequency to an external clock and has an internal 100k pull-down resistor.

PWMIN (Pin 7): PWM Gate Driver Input. Internal 100k pull-up resistor. While PWMIN is low, PWMOUT is low, GATE stops switching and the external I_{TH} network is disconnected, saving the I_{TH} state.

PWMOUT (Pin 8): PWM Gate Driver Output. Used for constant current dimming (LED load) or for output disconnect (step-up power supply).

GATE (Pin 9): Main Gate Driver Output for the Boost Converter.

$INTV_{CC}$ (Pin 10): Internal 7V Regulator Output. The main and PWM gate drivers and control circuits are powered from this voltage. Decouple this pin locally to the IC ground with a minimum of 4.7µF low ESR ceramic capacitor.

V_{IN} (Pin 11): Main Supply Pin. Must be closely decoupled to ground.

SENSE (Pin 12): Current Sense Input for the Control Loop. Connect this pin to the drain of the main power MOSFET for V_{DS} sensing and highest efficiency for $V_{SENSE} \leq 36V$. Alternatively, the SENSE pin may be connected to a resistor in the source of the main power MOSFET. Internal leading-edge blanking is provided for both sensing methods.

SS (Pin 13): Soft-Start Pin. Provides a 50µA pull-up current, enabled and reset by RUN, which charges an optional external capacitor. This voltage ramp translates into a corresponding current limit ramp through the main MOSFET.

OV/FB (Pin 14): Overvoltage Pin/Voltage Feedback Pin. In voltage mode ($V_{FBP} \leq V_{REF}$), this input, connected to V_{OUT} through a resistor network, sets the output voltage at which GATE switching is disabled in order to prevent an overvoltage situation. Nominal threshold voltage for the OV pin is 1.32V (V_{REF} + 7%) with 20mV hysteresis. In current/voltage mode ($V_{FBP} > 2.5V$), this pin senses V_{OUT} through a resistor divider and brings the loop into voltage regulation such that pin voltage approaches $V_{REF} = 1.23V$, provided the loop is not regulating the load current (e.g., [$V_{FBP} – V_{FBN}$] < 100mV for $I_{LIM} = 1.23V$).

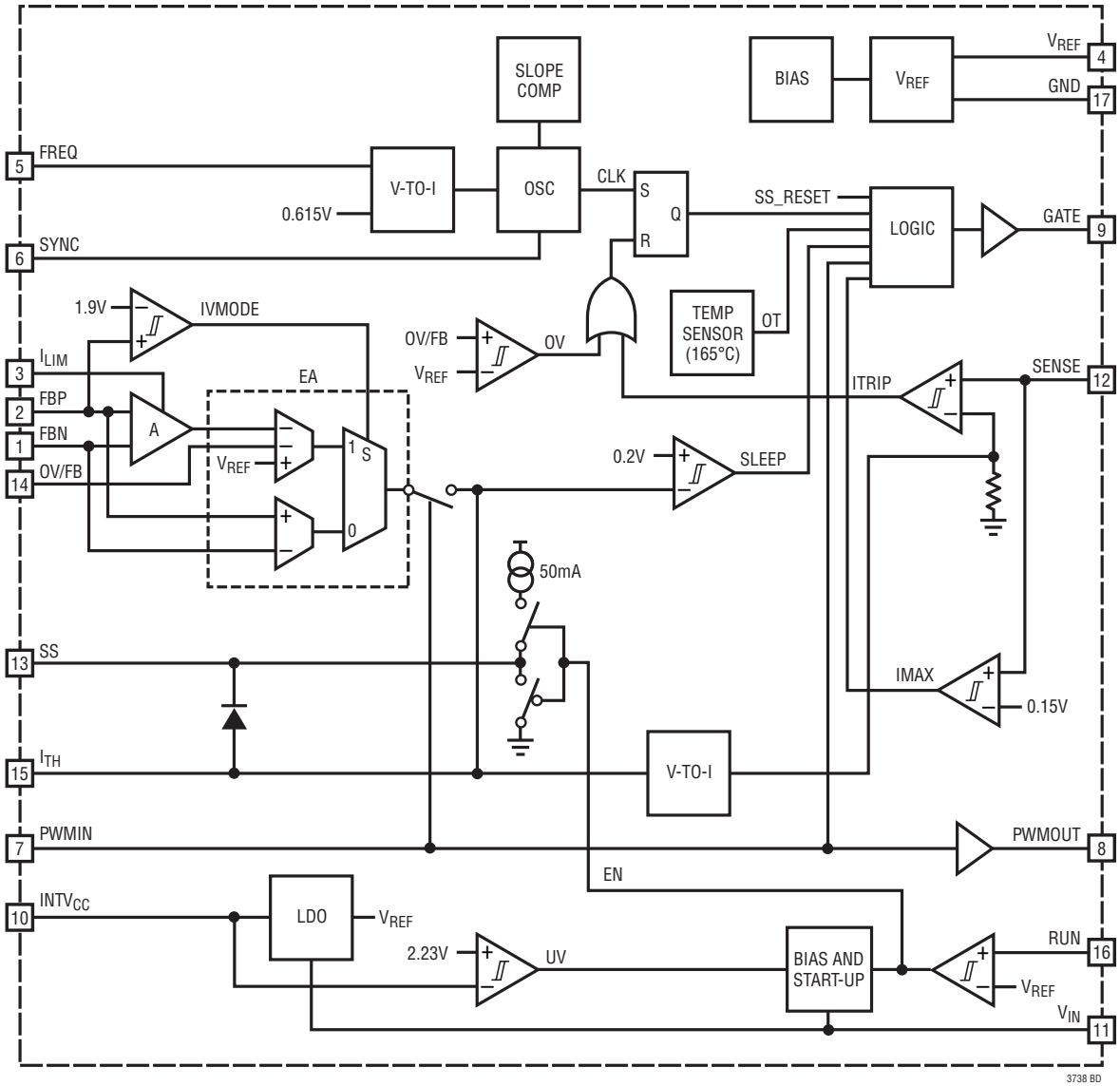
PIN FUNCTIONS

I_{TH} (Pin 15): Error Amplifier Output/Compensation Pin. The current comparator input threshold increases with this control voltage, which is the output of the g_m type error amplifier. Nominal voltage range for this pin is 0V to 1.40V.

RUN (Pin 16): The RUN pin provides the user with an accurate means for sensing the input voltage and programming the start-up threshold for the converter. The falling RUN pin threshold is nominally 1.248V and the comparator has 100mV hysteresis for noise immunity. When the RUN pin is grounded, the IC is shut down and the V_{IN} supply current is kept to a low value (20µA typ).

Exposed Pad (Pin 17): Ground Pin. Solder to PCB ground for electrical contact and rated thermal performance.

BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3783 is a constant frequency, current mode controller for PWM LED as well as DC/DC boost, SEPIC and flyback converter applications. In constant current LED applications, the LTC3783 provides an especially wide PWM dimming range due to its unique switching scheme, which allows PWM pulse widths as short as several converter switching periods.

For voltage feedback circuit operation (defined by $V_{FBP} \leq$ 1.23V), please refer to the Block Diagram of the IC and the Typical Application on the first page of this data sheet. In normal operation with PWMIN high, the power MOSFET is turned on (GATE goes high) when the oscillator sets the PWM latch, and is turned off when the ITRIP current comparator resets the latch. Based on the error voltage represented by ($V_{FBP} – V_{FBN}$), the error amplifier output signal at the I_{TH} pin sets the ITRIP current comparator input threshold. When the load current increases, a fall in the FBN voltage relative to the reference voltage at FBP causes the I_{TH} pin to rise, causing the ITRIP current comparator to trip at a higher peak inductor current value. The average inductor current will therefore rise until it equals the load current, thereby maintaining output regulation.

When PWMIN goes low, PWMOUT goes low, the I_{TH} switch opens and GATE switching is disabled. Lowering PWMOUT and disabling GATE causes the output capacitor C_{OUT} to hold the output voltage constant in the absence of load current. Opening the I_{TH} switch stores the correct load current value on the I_{TH} capacitor C_{ITH}. As a result, when PWMIN goes high again, both I_{TH} and V_{OUT} are instantly at the appropriate levels.

In voltage feedback operation, an overvoltage comparator, OV, senses when the OV/FB pin exceeds the reference voltage by 7% and provides a reset pulse to the main RS latch. Because this RS latch is reset-dominant, the power MOSFET is actively held off for the duration of an output overvoltage condition.

For constant current/constant voltage regulation operation (defined by $V_{FBP} > 2.5V$), please refer to the Block Diagram of the IC and Figure 11. Loop operation is similar to the voltage feedback, except FBP and FBN now sense the voltage across sense resistor R_L in series with the load. The I_{TH} pin now represents the error from the desired differential set voltage, from 10mV to 100mV, for I_{LIM} values of 0.123V to 1.23V. That is, with V_{ILIM} = 1.23V, the loop will regulate such that $V_{FBP} – V_{FBN}$ = 100mV; lower values of I_{LIM} attenuate the difference proportionally. PWMIN is still functional as above, but will only work properly if load current can be disconnected by the PWMOUT signal.

In constant current/constant voltage operation, the OV/FB pin becomes a voltage feedback pin, which causes the loop to regulate such that $V_{OV/FB}$ = 1.23V, provided the above current-sense voltage is not reached. In this way, the loop regulates either voltage or current, whichever parameter hits its preset limit first.

The nominal operating frequency of the LTC3783 is programmed using a resistor from the FREQ pin to ground and can be controlled over a 20kHz to 1MHz range. In addition, the internal oscillator can be synchronized to an external clock applied to the SYNC pin and can be locked to a frequency between 100% and 130% of its nominal value. When the SYNC pin is left open, it is pulled low by an internal 100k resistor. With no load, or an extremely light one, the controller will skip pulses in order to maintain regulation and prevent excessive output ripple.

The RUN pin controls whether the IC is enabled or is in a low current shutdown state. A micropower 1.248V reference and RUN comparator allow the user to program the supply voltage at which the IC turns on and off (the RUN comparator has 100mV of hysteresis for noise immunity). With the RUN pin below 1.248V, the chip is off and the input supply current is typically only 20µA.

OPERATION

The SS pin provides a soft-start current to charge an external capacitor. Enabled by RUN, the soft-start current is 50µA, which creates a positive voltage ramp on V_{SS} to which the internal I_{TH} is limited, avoiding high peak currents on start-up. Once V_{SS} reaches 1.23V, the full I_{TH} range is established.

The LTC3783 can be used either by sensing the voltage drop across the power MOSFET or by connecting the SENSE pin to a conventional shunt resistor in the source of the power MOSFET, as shown in the Typical Application on the first page of this data sheet. Sensing the voltage across the power MOSFET maximizes converter efficiency and minimizes the component count, but limits the output voltage to the maximum rating for this pin (36V). By connecting the SENSE pin to a resistor in the source of the power MOSFET, the user is able to program output voltages significantly greater than 36V, limited only by other components' breakdown voltages.

Externally Synchronized Operation

When an external clock signal drives the SYNC pin at a rate faster than the chip's internal oscillator, the oscillator will synchronize to it. When the oscillator's internal logic circuitry detects a synchronizing signal on the SYNC pin, the internal oscillator ramp is terminated early and the slope compensation is increased by approximately 25%. As a result, in applications requiring synchronization, it is recommended that the nominal operating frequency of the IC be programmed to be about 80% of the external clock frequency. Attempting to synchronize to too high an external frequency (above $1.3f_{OSC}$) can result in inadequate slope compensation and possible subharmonic oscillation (or jitter).

The external clock signal must exceed 2V for at least 25ns, and should have a maximum duty cycle of 80%, as shown in Figure 1. The MOSFET turn-on will synchronize to the rising edge of the external clock signal.

Programming the Operating Frequency

The choice of operating frequency and inductor value is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET and diode switching losses. However, lower frequency operation requires more inductance for a given amount of load current.

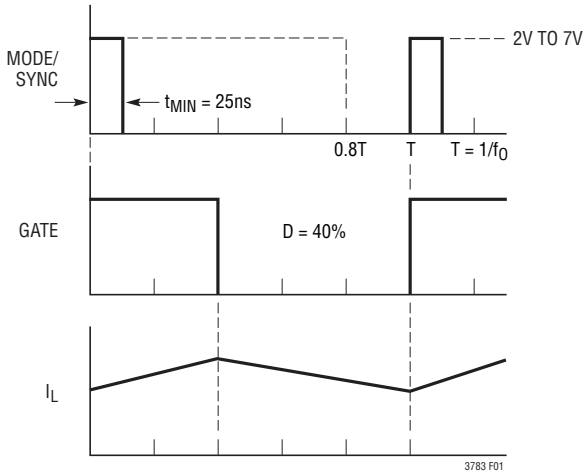


Figure 1. MODE/SYNC Clock Input and Switching Waveforms for Synchronized Operation

The LTC3783 uses a constant frequency architecture that can be programmed over a 20kHz to 1MHz range with a single external resistor from the FREQ pin to ground, as shown in the application on the first page of this data sheet. The nominal voltage on the FREQ pin is 0.615V, and the current that flows out of the FREQ pin is used to charge and discharge an internal oscillator capacitor. The oscillator frequency is trimmed to 300kHz with R_T = 20k. A graph for selecting the value of R_T for a given operating frequency is shown in Figure 2.

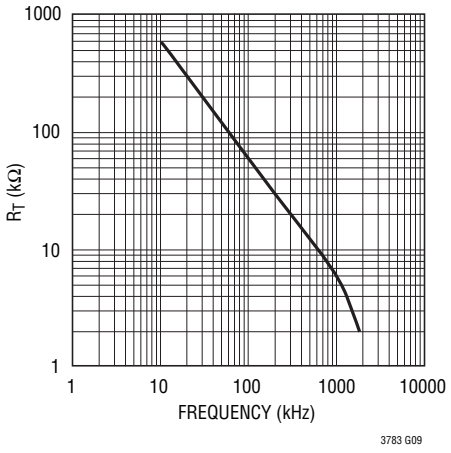


Figure 2. Timing Resistor (R_T) Value

OPERATION

$INTV_{CC}$ Regulator Bypassing and Operation

An internal, P-channel low dropout voltage regulator produces the 7V supply which powers the gate drivers and logic circuitry within the LTC3783 as shown in Figure 3. The $INTV_{CC}$ regulator can supply up to 50mA and must be bypassed to ground immediately adjacent to the IC pins with a minimum of 4.7µF low ESR or ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate driver.

For input voltages that don't exceed 8V (the absolute maximum rating for $INTV_{CC}$ is 9V), the internal low dropout regulator in the LTC3783 is redundant and the $INTV_{CC}$ pin can be shorted directly to the V_{IN} pin. With the $INTV_{CC}$ pin shorted to V_{IN}, however, the divider that programs the regulated $INTV_{CC}$ voltage will draw 15µA from the input supply, even in shutdown mode. For applications that require the lowest shutdown mode input supply current, do not connect the $INTV_{CC}$ pin to V_{IN}. Regardless of whether the $INTV_{CC}$ pin is shorted to V_{IN} or not, it is always necessary to have the driver circuitry bypassed with a 4.7µF low ESR ceramic capacitor to ground immediately adjacent to the $INTV_{CC}$ and GND pins.

In an actual application, most of the IC supply current is used to drive the gate capacitance of the power MOSFET. As a result, high input voltage applications in which a large power MOSFET is being driven at high frequencies can cause the LTC3783 to exceed its maximum junction temperature rating. The junction temperature can be estimated using the following equations:

$$I_{Q(TOT)} = I_Q + f \bullet Q_G$$

$$P_{IC} = V_{IN} \bullet (I_Q + f \bullet Q_G)$$

$$T_J = T_A + P_{IC} \bullet \theta_{JA}$$

The total quiescent current $I_{Q(TOT)}$ consists of the static supply current (I_Q) and the current required to charge and discharge the gate of the power MOSFET. The 16-lead FE package has a thermal resistance of θ_{JA} = 38°C/W and the DHD package has an θ_{JA} = 43°C/W

As an example, consider a power supply with V_{IN} = 12V and V_{OUT} = 25V at I_{OUT} = 1A. The switching frequency is 300kHz, and the maximum ambient temperature is 70°C. The power MOSFET chosen is the Si7884DP, which has a maximum $R_{DS(ON)}$ of 10mΩ (at room temperature) and

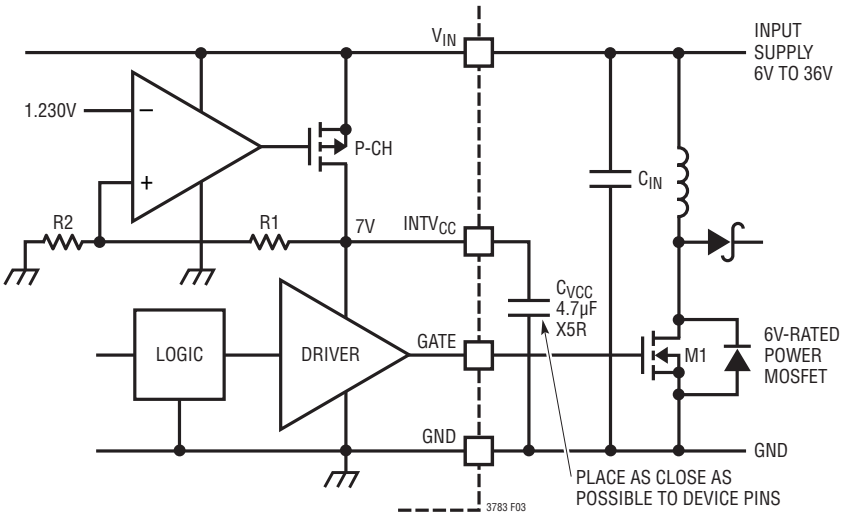


Figure 3. Bypassing the LDO Regulator and Gate Driver Supply

OPERATION

a maximum total gate charge of 35nC (the temperature coefficient of the gate charge is low).

$I_{Q(TOT)}$ = 1.2mA + 35nC • 300kHz = 12mA

P_{IC} = 12V • 12mA = 144mW

T_J = 70°C + 110°C/W • 144mW = 86°C

This demonstrates how significant the gate charge current can be when compared to the static quiescent current in the IC.

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked when operating in a continuous mode at high V_{IN}. A tradeoff between the operating frequency and the size of the power MOSFET may need to be made in order to maintain a reliable IC junction temperature. Prior to lowering the operating frequency, however, be sure to check with the power MOSFET manufacturers for the latest low Q_G, low $R_{DS(ON)}$ devices. Power MOSFET manufacturing technologies are continually improving, with newer and better-performing devices being introduced almost monthly.

Output Voltage Programming

In constant voltage mode, in order to regulate the output voltage, the output voltage is set by a resistor divider according to the following formula:

$$V_{OUT} = V_{FBP} \bullet \left(1 + \frac{R2}{R1}\right)$$

where $0 \le V_{FBP} \le 1.23V$. The external resistor divider is connected to the output as shown in Figure 4, allowing remote voltage sensing. The resistors R1 and R2 are typically chosen so that the error caused by the 500nA input bias current flowing out of the FBN pin during normal operation is less than 1%, which translates to a maximum R1 value of about 25k at V_{FBP} = 1.23V. For lower FBP voltages, R1 must be reduced accordingly to maintain accuracy, e.g., R1 < 2k for 1% accuracy when V_{FBP} = 100mV. More accuracy can be achieved with lower resistances, at the expense of increased dissipation and decreased light load efficiency.

A similar analysis applies to the V_{FBP} resistive divider, if one is used:

$$V_{FBP} = V_{REF} \bullet \frac{R3}{R3+R4}$$

where R3 is subject to a similar 500nA bias current.

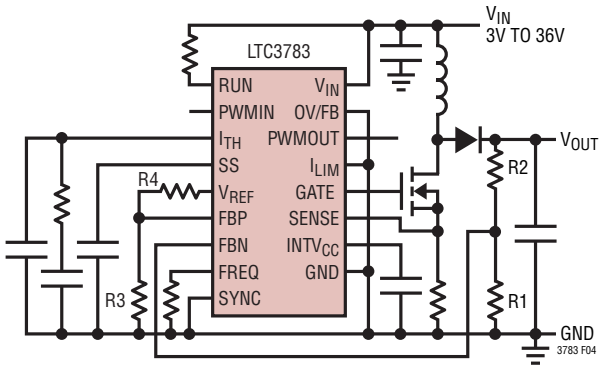


Figure 4. LTC3783 Boost Application

Programming Turn-On and Turn-Off Thresholds with the RUN Pin

The LTC3783 contains an independent, micropower voltage reference and comparator detection circuit that remains active even when the device is shut down, as shown in Figure 5. This allows users to accurately program an input voltage at which the converter will turn on and off. The falling threshold on the RUN pin is equal to the internal reference voltage of 1.248V. The comparator has 100mV of hysteresis to increase noise immunity.

The turn-on and turn-off input voltage thresholds are programed using a resistor divider according to the following formulas:

$$V_{IN(OFF)} = 1.248V \bullet \left(1 + \frac{R2}{R1}\right)$$

$$V_{IN(ON)} = 1.348V \bullet \left(1 + \frac{R2}{R1}\right)$$

The resistor R1 is typically chosen to be less than 1M.

OPERATION

For applications where the RUN pin is only to be used as a logic input, the user should be aware of the 7V Absolute Maximum Rating for this pin! The RUN pin can be connected to the input voltage through an external 1M resistor, as shown in Figure 5c, for "always on" operation.

Soft-Start Capacitor Selection

For proper soft-start operation, the LTC3783 should have a sufficiently large soft-start capacitor, C_{SS}, attached to the SS pin. The minimum soft-start capacitor size can be estimated on the basis of output voltage, capacitor size and load current. In addition, PWM operation reduces the effective SS capacitor value by the dimming ratio.

$$C_{SS(MIN)} > \frac{2 \bullet \text{dimming ratio} \bullet 50\mu A \bullet C_{OUT} \bullet V_{OUT} \bullet R_{DS(ON)/SENSE}}{150mV \bullet 1.2V}$$

assuming 50% ripple current, where $R_{DS(ON)/SENSE}$ represents either the $R_{DS(ON)}$ of the switching MOSFET or R_{SENSE}, whichever is used on the SENSE pin. Dimming ratio is described by $1/D_{PWM}$ as shown in Figure 6.

Application Circuits

A basic LTC3783 PWM-dimming LED application is shown on the first page of this data sheet.

Operating Frequency and PWM Dimming Ratio

The minimum operating frequency, f_{OSC}, required for proper operation of a PWM dimming application depends on the minimum PWM frequency, f_{PWM}, the dimming ratio $1/D_{PWM}$, and N, the number of f_{OSC} cycles per PWM cycle:

$$f_{OSC} > \frac{N \bullet f_{PWM}}{D_{PWM}}$$

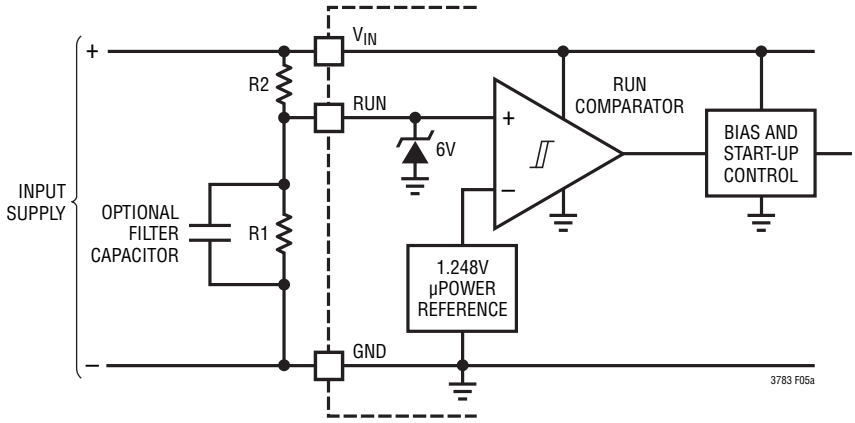


Figure 5a. Programming the Turn-On and Turn-Off Thresholds Using the RUN Pin

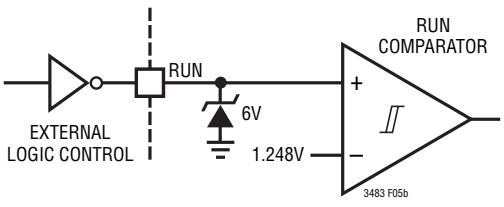


Figure 5b. On/Off Control Using External Logic

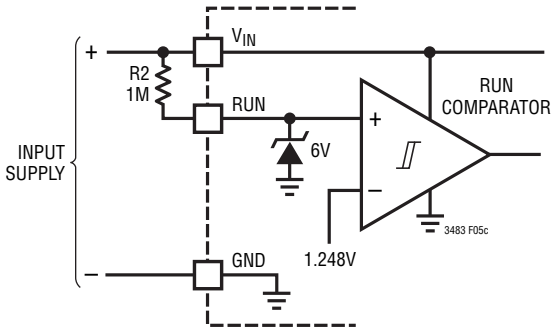


Figure 5c. External Pull-Up Resistor on RUN Pin for "Always On" Operation

OPERATION

Figure 6 illustrates these various quantities in relation to one another.

Typically, in order to avoid visible flicker, f_{PWM} should be greater than 120Hz. Assuming inductor and capacitor sizing which is close to discontinuous operation, 2 f_{OSC} cycles are sufficient for proper PWM operation. Thus, within the 1MHz rated maximum f_{OSC}, a dimming ratio of $1/D_{PWM}$ = 3000 is possible.

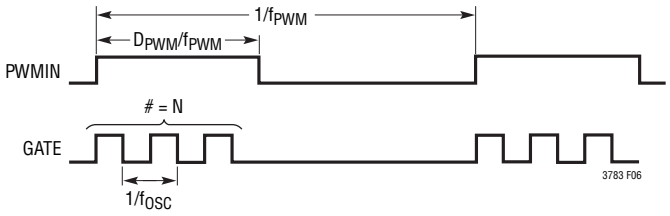


Figure 6. PWM Dimming Parameters

Boost Converter: Duty Cycle Considerations

For a boost converter operating in a continuous conduction mode (CCM), the duty cycle of the main switch is:

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D}$$

where V_D is the forward voltage of the boost diode. For converters where the input voltage is close to the output voltage, the duty cycle is low, and for converters that develop a high output voltage from a low input voltage, the duty cycle is high. The maximum output voltage for a boost converter operating in CCM is:

$$V_{OUT(MAX)} = \frac{V_{IN(MIN)}}{1 - D_{MAX}} - V_D$$

The maximum duty cycle capability of the LTC3783 is typically 90%. This allows the user to obtain high output voltages from low input supply voltages.

Boost Converter: The Peak and Average Input Currents

The control circuit in the LTC3783 is measuring the input current (either by using the $R_{DS(ON)}$ of the power MOSFET or by using a sense resistor in the MOSFET source), so the output current needs to be reflected back to the input in order to dimension the power MOSFET properly. Based on the fact that, ideally, the output power is equal to the input power, the maximum average input current is:

$$I_{IN(MAX)} = \frac{I_{OUT(MAX)}}{1 - D_{MAX}}$$

The peak input current is:

$$I_{IN(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{OUT(MAX)}}{1 - D_{MAX}}$$

The maximum duty cycle, D_{MAX}, should be calculated at minimum V_{IN}.

Boost Converter: Ripple Current ΔI_L and the 'χ' Factor

The constant 'χ' in the equation above represents the percentage peak-to-peak ripple current in the inductor, relative to its maximum value. For example, if 30% ripple current is chosen, then χ = 0.3, and the peak current is 15% greater than the average.

For a current mode boost regulator operating in CCM, slope compensation must be added for duty cycles above 50% in order to avoid subharmonic oscillation. For the LTC3783, this ramp compensation is internal. Having an internally fixed ramp compensation waveform, however, does place some constraints on the value of the inductor and the operating frequency. If too large an inductor is used, the resulting current ramp (ΔI_L) will be small relative to the internal ramp compensation (at duty cycles above 50%), and the converter operation will approach voltage mode (ramp compensation reduces the gain of the current loop). If too small an inductor is used, but the converter is still operating in CCM (near critical conduction mode), the internal ramp compensation may be inadequate to prevent subharmonic oscillation. To ensure good current mode gain and to avoid subharmonic oscillation, it is recommended that the ripple current in the inductor fall in the range of 20% to 40% of the maximum average current. For example, if the maximum average input current is 1A, choose a ΔI_L between 0.2A and 0.4A, and correspondingly a value 'χ' between 0.2 and 0.4.

OPERATION

Boost Converter: Inductor Selection

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value can be determined using the following equation:

$$L = \left(\frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \right) \bullet D_{MAX}$$

where:

$$\Delta I_L = \frac{\chi \bullet I_{OUT(MAX)}}{1 - D_{MAX}}$$

Remember that most boost converters are not short-circuit protected. Under a shorted output condition, the inductor current is limited only by the input supply capability. For applications requiring a step-up converter that is short-circuit protected, please refer to the applications section covering SEPIC converters.

The minimum required saturation current of the inductor can be expressed as a function of the duty cycle and the load current, as follows:

$$I_{L(SAT)} > \left(1 + \frac{\chi}{2} \right) \bullet \frac{I_{OUT(MAX)}}{1 - D_{MAX}}$$

The saturation current rating for the inductor should be checked at the minimum input voltage (which results in the highest inductor current) and maximum output current.

Boost Converter: Operating in Discontinuous Mode

Discontinuous mode operation occurs when the load current is low enough to allow the inductor current to run out during the off-time of the switch, as shown in Figure 7. Once the inductor current is near zero, the switch and diode capacitances resonate with the inductance to form damped ringing at 1MHz to 10MHz. If the off-time is long enough, the drain voltage will settle to the input voltage.

Depending on the input voltage and the residual energy in the inductor, this ringing can cause the drain of the power MOSFET to go below ground where it is clamped by the body diode. This ringing is not harmful to the IC and it has not been shown to contribute significantly to EMI. Any attempt to damp it with a snubber will degrade the efficiency.

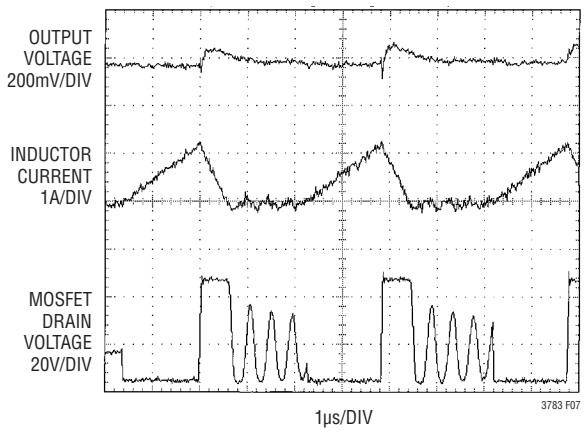


Figure 7. Discontinuous Mode Waveforms

Boost Converter: Power MOSFET Selection

The power MOSFET can serve two purposes in the LTC3783: it represents the main switching element in the power path, and its $R_{DS(ON)}$ can represent the current sensing element for the control loop. Important parameters for the power MOSFET include the drain-to-source breakdown voltage BV_{DSS}, the threshold voltage $V_{GS(TH)}$, the on-resistance $R_{DS(ON)}$ versus gate-to-source voltage, the gate-to-source and gate-to-drain charges Q_{GS} and Q_{GD}, respectively, the maximum drain current $I_{D(MAX)}$ and the MOSFET's thermal resistances θ_{JC} and θ_{JA}.

The gate drive voltage is set by the 7V $INTV_{CC}$ low drop regulator. Consequently, 6V rated MOSFETs are required in most high voltage LTC3783 applications. If low input voltage operation is expected (e.g., supplying power from a lithium-ion battery or a 3.3V logic supply), then sublogic-level threshold MOSFETs should be used. Pay close attention to the BV_{DSS} specifications for the MOSFETs relative to the maximum actual switch voltage in the application. Many logic-level devices are limited to 30V or less, and the switch node can ring during the turn-off of the MOSFET due to layout parasitics. Check the switching waveforms of the MOSFET directly across the drain and source terminals using the actual PC board layout for excessive ringing.

OPERATION

During the switch on-time, the IMAX comparator limits the absolute maximum voltage drop across the power MOSFET to a nominal 150mV, regardless of duty cycle. The peak inductor current is therefore limited to 150mV/$R_{DS(ON)}$. The relationship between the maximum load current, duty cycle, and the $R_{DS(ON)}$ of the power MOSFET is:

$$R_{DS(ON)} < 150mV \bullet \frac{1-D_{MAX}}{\left(1+\frac{\chi}{2}\right)\bullet I_{OUT(MAX)} \bullet \rho_T}$$

The ρ_T term accounts for the temperature coefficient of the $R_{DS(ON)}$ of the MOSFET, which is typically 0.4%/°C. Figure 8 illustrates the variation of normalized $R_{DS(ON)}$ over temperature for a typical power MOSFET.

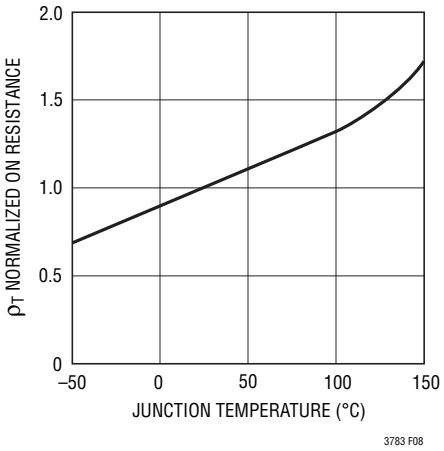


Figure 8. Normalized $R_{DS(ON)}$ vs Temperature

Another method of choosing which power MOSFET to use is to check what the maximum output current is for a given $R_{DS(ON)}$, since MOSFET on-resistances are available in discrete values.

$$I_{O(MAX)} = 150mV \bullet \frac{1-D_{MAX}}{\left(1+\frac{\chi}{2}\right)\bullet R_{DS(ON)} \bullet \rho_T}$$

It is worth noting that the 1 - D_{MAX} relationship between $I_{O(MAX)}$ and $R_{DS(ON)}$ can cause boost converters with a wide input range to experience a dramatic range of maximum input and output currents. This should be taken into consideration in applications where it is important to limit the maximum current drawn from the input supply, and also to avoid triggering the 150mV IMAX comparator, as this condition can result in excessive noise.

Calculating Power MOSFET Switching and Conduction Losses and Junction Temperatures

In order to calculate the junction temperature of the power MOSFET, the power dissipated by the device must be known. This power dissipation is a function of the duty cycle, the load current, and the junction temperature itself (due to the positive temperature coefficient of its $R_{DS(ON)}$. As a result, some iterative calculation is normally required to determine a reasonably accurate value. Since the controller is using the MOSFET as both a switching and a sensing element, care should be taken to ensure that the converter is capable of delivering the required load current over all operating conditions (line voltage and temperature), and for the worst-case specifications for $V_{SENSE(MAX)}$ and the $R_{DS(ON)}$) of the MOSFET listed in the manufacturer's data sheet.

The power dissipated by the MOSFET in a boost converter is:

$$P_{FET} = \left(\frac{I_{OUT(MAX)}}{1-D_{MAX}}\right)^2 \bullet R_{DS(ON)} \bullet D_{MAX} \bullet \rho_T + k \bullet V_{OUT}^{1.85} \bullet \left(\frac{I_{OUT(MAX)}}{1-D_{MAX}}\right) \bullet C_{RSS} \bullet f$$

The first term in the equation above represents the I^2R losses in the device, and the second term, the switching losses. The constant k = 1.7 is an empirical factor inversely related to the gate drive current and has the dimension of 1/current.

OPERATION

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P_{FET} \bullet \theta_{JA}$$

The θ_{JA} to be used in this equation normally includes the θ_{JC} for the device plus the thermal resistance from the case to the ambient temperature (θ_{CA}). This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

Boost Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with low forward drop and low reverse leakage is desired. The output diode in a boost converter conducts current during the switch off-time. The peak reverse voltage that the diode must withstand is equal to the regulator output voltage. The average forward current in normal operation is equal to the output current, and the peak current is equal to the peak inductor current.

$$I_{D(PEAK)} = I_{L(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{OUT(MAX)}}{1 - D_{MAX}}$$

The power dissipated by the diode is:

$$P_D = I_{OUT(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet \theta_{JA}$$

The θ_{JA} to be used in this equation normally includes the θ_{JC} for the device plus the thermal resistance from the board to the ambient temperature in the enclosure.

Remember to keep the diode lead lengths short and to observe proper switch-node layout (see Board Layout Checklist) to avoid excessive ringing and increased dissipation.

Boost Converter: Output Capacitor Selection

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct component for a given output ripple voltage. The effects of these three parameters (ESR, ESL and bulk C) on the output voltage ripple waveform are illustrated in Figure 9 for a typical boost converter.

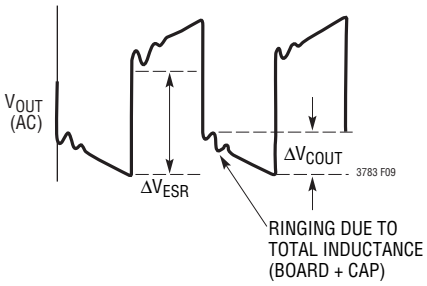


Figure 9. Output Ripple Voltage

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step and the charging/discharging ΔV. For the purpose of simplicity we will choose 2% for the maximum output ripple, to be divided equally between the ESR step and the charging/discharging ΔV. This percentage ripple will change, depending on the requirements of the application, and the equations provided below can easily be modified.

For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} < 0.01 \bullet \frac{V_{OUT}}{I_{IN(PEAK)}}$$

where:

$$I_{IN(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{OUT(MAX)}}{1 - D_{MAX}}$$

For the bulk C component, which also contributes 1% to the total ripple:

$$C_{OUT} > \frac{I_{OUT(MAX)}}{0.01 \bullet V_{OUT} \bullet f}$$

OPERATION

For many designs it is possible to choose a single capacitor type that satisfies both the ESR and bulk C requirements for the design. In certain demanding applications, however, the ripple voltage can be improved significantly by connecting two or more types of capacitors in parallel. For example, using a low ESR ceramic capacitor can minimize the ESR setup, while an electrolytic capacitor can be used to supply the required bulk C.

Once the output capacitor ESR and bulk capacitance have been determined, the overall ripple voltage waveform should be verified on a dedicated PC board (see Board Layout section for more information on component placement). Lab breadboards generally suffer from excessive series inductance (due to inter-component wiring), and these parasitics can make the switching waveforms look significantly worse than they would be on a properly designed PC board.

The output capacitor in a boost regulator experiences high RMS ripple currents. The RMS output capacitor ripple current is:

$$I_{RMS(COUT)} \; ; \; I_{OUT(MAX)} \bullet \sqrt{\frac{V_{OUT} - V_{IN(MIN)}}{V_{IN(MIN)}}}$$

Note that the ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design.

Boost Converter: Input Capacitor Selection

The input capacitor of a boost converter is less critical than the output capacitor, due to the fact that the inductor is in series with the input, and hence, the input current waveform is continuous (see Figure 10). The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 10µF to 100µF. A low ESR capacitor is recommended, although it is not as critical as for the output capacitor.

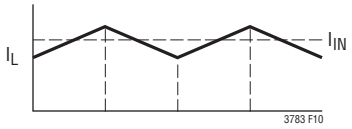


Figure 10. Inductor and Input Currents

The RMS input capacitor ripple current for a boost converter is:

$$I_{RMS(CIN)} \; ; \; 0.3 \bullet \frac{V_{IN(MIN)}}{L \bullet f} \bullet D_{MAX}$$

Please note that the input capacitor can see a very high surge current when a battery is suddenly connected to the input of the converter, and solid tantalum capacitors can fail catastrophically under these conditions. Be sure to specify surge-tested capacitors!

Boost Converter Design Example

The design example given here will be for the circuit shown in Figure 1. The input voltage is 12V, and the output voltage is 25V at a maximum load current of 0.7A (1A peak).

1. The duty cycle is:

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D} = \frac{25 + 0.4 - 12}{25 + 0.4} = 53\%$$

2. The operating frequency is chosen to be 1MHz to maximize the PWM dimming range. From Figure 2, the resistor from the FREQ pin to ground is 6k.

3. An inductor ripple current of 40% of the maximum load current is chosen, so the peak input current (which is also the minimum saturation current) is:

$$I_{IN(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{OUT(MAX)}}{1 - D_{MAX}} = 1.2 \bullet \frac{0.7}{1 - 0.53} = 1.8A$$

The inductor ripple current is:

$$\Delta I_L = \chi \bullet \frac{I_{OUT(MAX)}}{1 - D_{MAX}} = 0.4 \bullet \frac{0.7}{1 - 0.53} = 0.6A$$

OPERATION

And so the inductor value is:

$$L = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX} = \frac{12V}{0.6A \bullet 1MHz} \bullet 0.53 = 11\mu H$$

4. R_{SENSE} should be:

$$R_{SENSE} = \frac{0.5 \bullet V_{SENSE(MAX)}}{I_{IN(PEAK)}} = \frac{0.5 \bullet 150mV}{1.8A} = 42m\Omega$$

5. The diode for this design must handle a maximum DC output current of 0.7A and be rated for a minimum reverse voltage of V_{OUT}, or 25V. A 1A, 40V diode from Zetex was chosen for its specifications, especially low leakage at higher temperatures, which is important for maintaining dimming range.

6. Voltage and value permitting, the output capacitor usually consists of some combination of low ESR ceramics. Based on a maximum output ripple voltage of 1%, or 250mV, the bulk C needs to be greater than:

$$C_{OUT} > \frac{I_{OUT(MAX)}}{0.01 \bullet V_{OUT} \bullet f} = \frac{0.7A}{0.01 \bullet 25V \bullet 1MHz} = 3\mu F$$

The RMS ripple current rating for this capacitor needs to exceed:

$$I_{RMS(COUT)} = I_{OUT(MAX)} \bullet \sqrt{\frac{V_{OUT} - V_{IN(MIN)}}{V_{IN(MIN)}}}$$

$$= 0.7A \bullet \sqrt{\frac{25V - 12V}{12V}} = 0.7A$$

Based on value and ripple current, and taking physical size into account, a surface mount ceramic capacitor is a good choice. A 4.7µF TDK C5750X7R1H475M will satisfy all requirements in a compact package.

7. The soft-start capacitor should be:

$$C_{SS(MIN)} > \frac{2 \bullet \text{dimming ratio} \bullet 50\mu A \bullet C_{OUT} \bullet V_{OUT} \bullet R_{DS(ON)/SENSE}}{150mV \bullet 1.2V}$$

$$> \frac{2 \bullet 3000 \bullet 50\mu A \bullet 4.7\mu F \bullet 25V \bullet 42m\Omega}{150mV \bullet 1.2V} = 8\mu F$$

8. The choice of an input capacitor for a boost converter depends on the impedance of the source supply and the amount of input ripple the converter will safely tolerate. For this particular design and lab setup, 20µF was found to be satisfactory.

PC Board Layout Checklist

1. In order to minimize switching noise and improve output load regulation, the GND pad of the LTC3783 should be connected directly to 1) the negative terminal of the $INTV_{CC}$ decoupling capacitor, 2) the negative terminal of the output decoupling capacitors, 3) the bottom terminals of the sense resistors or the source of the power MOSFET, 4) the negative terminal of the input capacitor, and 5) at least one via to the ground plane immediately under the exposed pad. The ground trace on the top layer of the PC board should be as wide and short as possible to minimize series resistance and inductance.

2. Beware of ground loops in multiple layer PC boards. Try to maintain one central ground node on the board and use the input capacitor to avoid excess input ripple for high output current power supplies. If the ground plane is to be used for high DC currents, choose a path away from the small-signal components.

3. Place the C_{VCC} capacitor immediately adjacent to the $INTV_{CC}$ and GND pins on the IC package. This capacitor carries high di/dt MOSFET gate-drive currents. A low ESR and ESL 4.7µF ceramic capacitor works well here.

4. The high di/dt loop from the bottom terminal of the output capacitor, through the power MOSFET, through the boost diode and back through the output capacitors should be kept as tight as possible to reduce inductive ringing. Excess inductance can cause increased stress on the power MOSFET and increase HF noise on the output. If low ESR ceramic capacitors are used on the output to reduce output noise, place these capacitors close to the boost diode in order to keep the series inductance to a minimum.

OPERATION

5. Check the stress on the power MOSFET by measuring its drain-to-source voltage directly across the device terminals (reference the ground of a single scope probe directly to the source pad on the PC board). Beware of inductive ringing which can exceed the maximum specified voltage rating of the MOSFET. If this ringing cannot be avoided and exceeds the maximum rating of the device, either choose a higher voltage device or specify an avalanche-rated power MOSFET.

6. Place the small-signal components away from high frequency switching nodes. All of the small-signal components should be placed on one side of the IC and all of the power components should be placed on the other. This also allows the use of a pseudo-Kelvin connection for the signal ground, where high di/dt gate driver currents flow out of the IC ground pad in one direction (to bottom plate of the $INTV_{CC}$ decoupling capacitor) and small-signal currents flow in the other direction.

7. If a sense resistor is used in the source of the power MOSFET, minimize the capacitance between the SENSE pin trace and any high frequency switching nodes. The LTC3783 contains an internal leading-edge blanking time of approximately 160ns, which should be adequate for most applications.

8. For optimum load regulation and true remote sensing, the top of the output resistor should connect independently to the top of the output capacitor (Kelvin connection), staying away from any high dV/dt traces. Place the divider resistors near the LTC3783 in order to keep the high impedance FBN node short.

9. For applications with multiple switching power converters connected to the same input supply, make sure that the input filter capacitor for the LTC3783 is not shared with any other converters. AC input current from another converter could cause substantial input voltage ripple, and this could interfere with the operation of the LTC3783. A few inches of PC trace or wire (L ~ 100nH) between the C_{IN} of the LTC3783 and the actual source V_{IN} should be sufficient to prevent current-sharing problems.

Returning the Load to V_{IN}: A Single Inductor Buck-Boost Application

As shown in Figure 11, due to its available high side current sensing mode, the LTC3783 is also well-suited to a boost converter in which the load current is returned to V_{IN}, hence providing a load voltage ($V_{OUT} – V_{IN}$) which can be greater or less than the input voltage V_{IN}. This configuration allows for complete overlap of input and output voltages, with the disadvantages that only the load current, and not the load voltage, can be tightly regulated. The switch must be rated for a $V_{DS(MAX)}$ equal to $V_{IN} + V_{LOAD}$.

The design of this circuit resembles that of the boost converter above, and the procedure is much the same, except V_{OUT} is now ($V_{IN} + V_{LOAD}$), and the duty cycles and voltages must be adjusted accordingly.

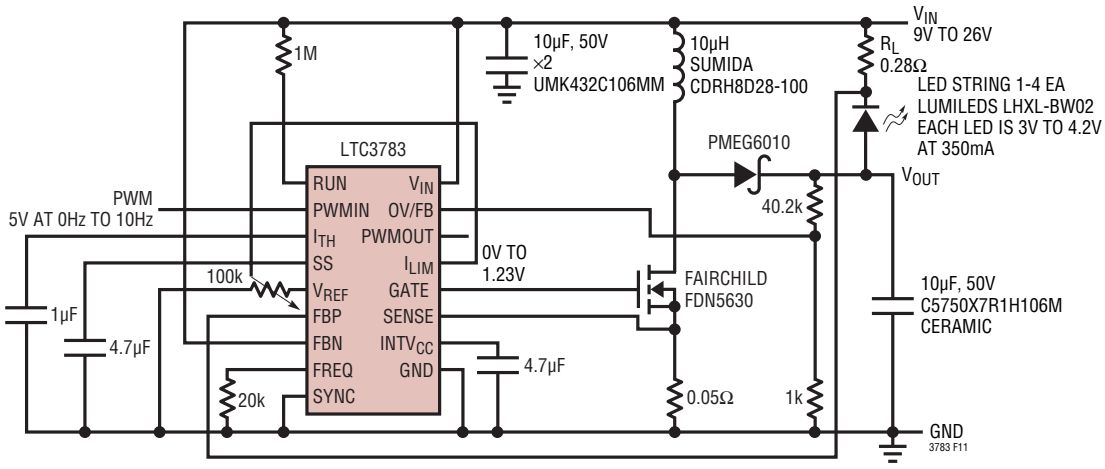


Figure 11. Single Inductor Buck-Boost Application with Analog Dimming and Low Frequency PWM Dimming

OPERATION

Similar to the boost converter, which can be dimmed via the digital PWMIN input or the analog FBP pin, the buck-boost can be dimmed via the PWMIN pin or the analog I_{LIM} pin, which adjusts the offset voltage to which the loop will drive ($V_{FBP} – V_{FBN}$). In the case of the buck-boost, however, the dimming ratio cannot be as high as in the boost converter, since there is no load switch to preserve the V_{OUT} level while PWMIN is low.

Using the LTC3783 for Buck Applications

As shown in Figure 12, high side current sensing also allows the LTC3783 to control a functional buck converter when load voltage is always sufficiently less than V_{IN}. In this scheme the input voltage to the inductor is lowered by the load voltage. The boost converter now sees a $V_{IN}' = V_{IN} – V_{LOAD}$, meaning the controller is now boosting from ($V_{IN} – V_{LOAD}$) to V_{IN}.

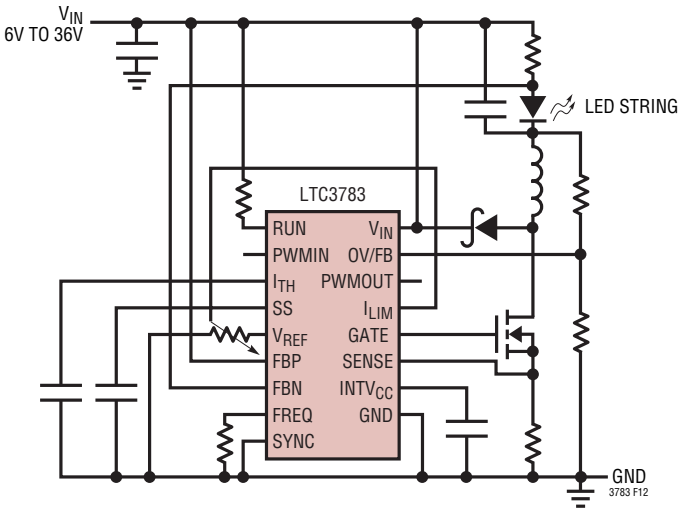
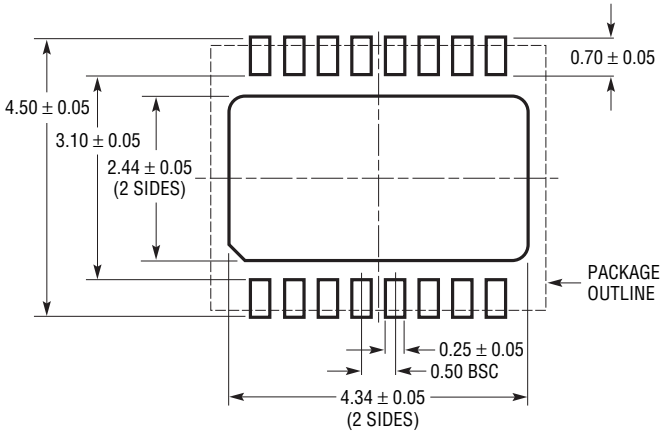


Figure 12. LED Buck Application

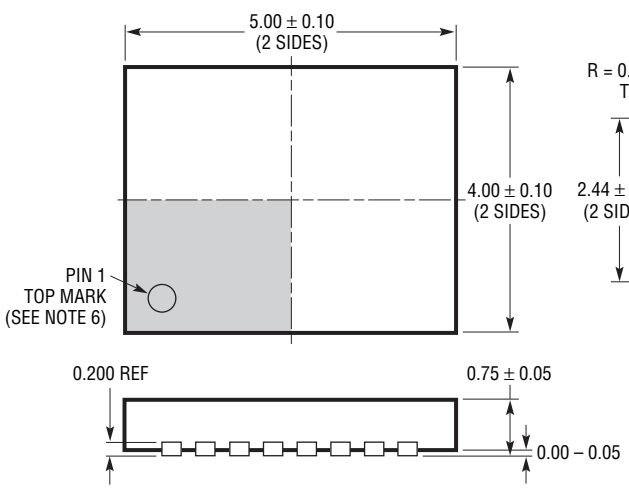
PACKAGE DESCRIPTION

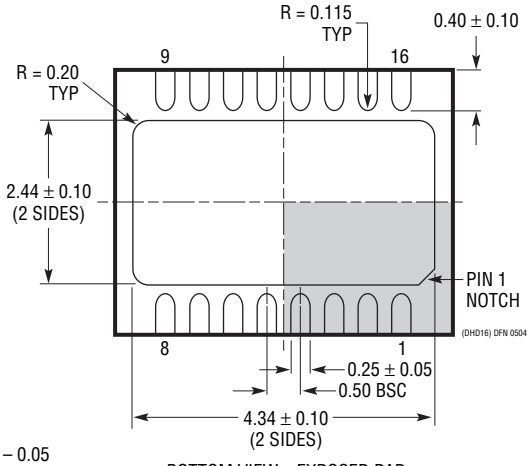
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DHD Package
16-Lead Plastic DFN (5mm × 4mm)
(Reference LTC DWG # 05-08-1707)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS





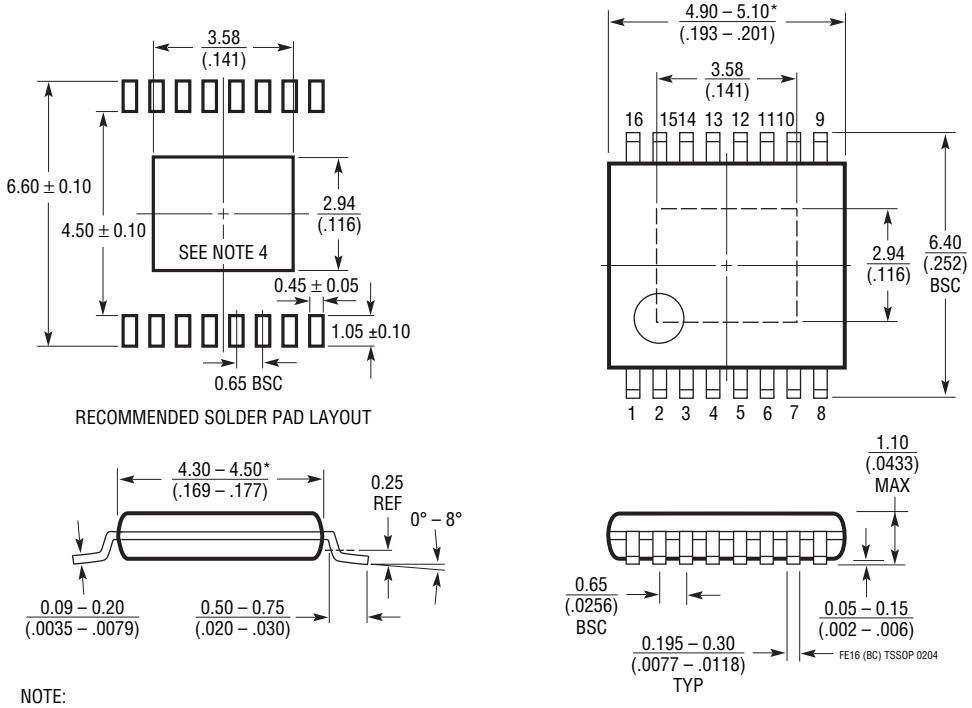
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJGD-2) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BC



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1618	Monolithic 1.4MHz Boost Regulator	Constant-Current/Constant-Voltage, 1A Switch
LTC1871	Boost, Flyback, SEPIC Controller	No R_{SENSE}, 2.5V ≤ V_{IN} ≤ 36V, 92% Duty Cycle
LT3477	3A DC/DC LED Driver with Rail-to-Rail Current Sense	2.5V ≤ V_{IN} ≤ 25V: Buck, Buck-Boost and Boost Topologies
LTC3780	High Power Buck-Boost Controller	4-Switch, 4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 30V
LTC3782	2-Phase Boost Controller	High Power, 6V ≤ V_{IN} ≤ 40V, 150kHz to 500kHz
LTC3827/LTC3827-1	Low I_Q Current Dual Controllers	2-Phase, 80µA I_Q, 0.8V ≤ V_{OUT} ≤ 10V, 4V ≤ V_{IN} ≤ 36V
LTC4002	Standalone 2A Li-Ion Battery Charger	1- and 2-Cell, 4.7V ≤ V_{IN} ≤ 22V, 3 Hour Timer

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