Ordering number : ENA1475

SANYO Semiconductors
DATA SHEET

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Bi-CMOS IC

LV5809MX — Step-down Switching Regulator

Overview

LV5809MX is a 1ch step-down switching regulator. 0.2Ω FET is incorporated on the upper side to achieve high-efficiency operation for large output current. Low-heat resistance and compact-package MFP8 (200mil) employed. Current mode control type, with superior load current response and easy phase compensation ON/OFF pin, allowing the standby mode with the current drain of 40μA or less Pulse-by-pulse over-current protection and overheat protection available for protection of load devices Soft start pin to be provided with a capacitance for soft start.

Functions

- 2.5A 1ch step-down switching regulator
- Wide input dynamic range (4.5 to 18V)
- High efficiency (90% I_{OUT} = 1A, V_{IN} = 12V, V_O = 5V)
- Standby mode
- Over-current protection
- Thermal shutdown
- Reference voltage: 0.8V
- Fixed frequency: 330kHz
- Soft start
- Compact package: MFP8 (200mil) with Exposed Pad

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum input V_{IN} voltage	V_{IN} max		20	V
BOOT pin maximum voltage	V_{BT} max		25	V
SW pin maximum voltage	V_{SW} max		V_{IN} max	V
BOOT pin-SW pin maximum voltage	V_{BS-SW} max		7	V
EN pin maximum voltage	V_{EN} max		20	V
FB, COMP, SS pin maximum voltage	Vfs max		7	V
Allowable power dissipation	Pd max	Mount on a specified board *	2.05	W
Junction temperature	Tj max		150	°C
Operating temperature	Topr		-20 to 80	°C
Storage temperature	Tstg		-40 to 150	°C

* Specified board: 46.4mm × 31.8mm ×1.7mm, glass epoxy both side.

Note: Plan the maximum voltage while including coil and surge voltages, so that the maximum voltage is not exceeded even for an instant.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{IN} pin voltage	V_{IN}		4.5 to 18	V
BOOT pin voltage	V_{BT}		-0.3 to 23	V
SW pin voltage	V_{SW}		-0.4 to V_{IN}	V
BOOT pin-SW pin maximum voltage	V_{BS-SW}		6.5	V
EN pin maximum voltage	V_{EN}		18	V
FB, COMP, SS pin voltage	V_{FSO}		6	V

Electrical Characteristics at Ta = 25°C, V_{IN} = 12V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
IC current drain at standby	$I_{CC}1$	EN=0V		40		μA
IC current drain in operation	$I_{CC}2$	EN=open		2		mA
Efficiency	Effcy	V_{IN}=12V, I_{OUT}=1A, Vo=5V, Design target *1		90		%
Reference voltage	Vref	V_{IN}=4.5V to 18V (±2%)	-2%	0.8	+2%	V
FB pin bias current	Iref	FB=0.8V application		10	100	nA
High-side ON resistance	RonH	BOOT=5V		0.2		Ω
Oscillation frequency	f_{OSC}		265	330	395	kHz
Oscillation frequency during short-circuit protection	f_{OSCS}		26	33	40	kHz
EN high-threshold voltage	Venh				2.1	V
EN low-threshold voltage	Venl		0.8			V
Maximum ON DUTY	D max			80		%
Current limit peak value 1	Ic1	V_{IN}=12V, V_{OUT}=5V, L=10μH	2.7		5.3	A
Current limit peak value 2	Ic2	V_{IN}=12V, V_{OUT}=3.3V, L=10μH	3.0		5.6	A
Current limit peak value 3	Ic3	V_{IN}=12V, V_{OUT}=1.2V, L=10μH	3.3		5.9	A
Thermal shutdown temperature	Ttsd	*Design guarantee *2		160		°C
Thermal shutdown temperature hysteresis	Dtsd	*Design guarantee *2		40		°C
Soft start current	I_{SS}	SS=0V	6	10	14	μA

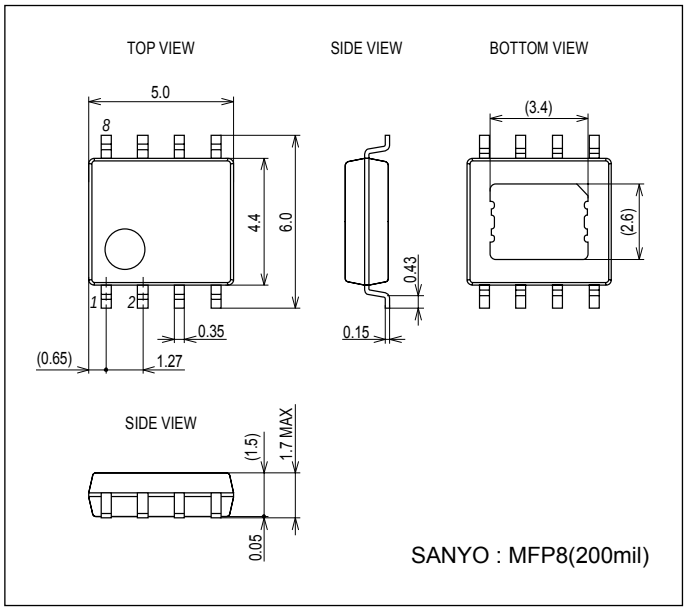
*1: Reference value (not tested before shipment)

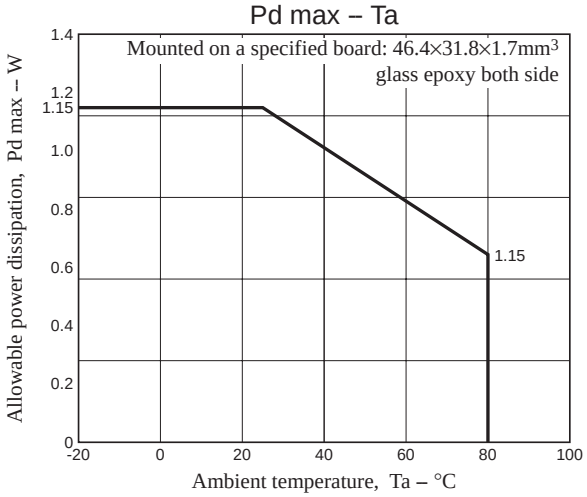
*2: Design guarantee (value guaranteed by design and not tested before shipment)

Package Dimensions

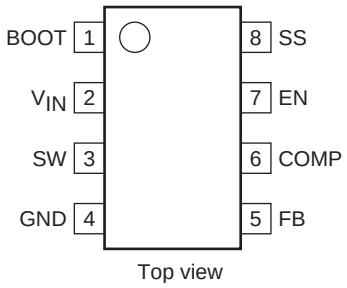
unit : mm (typ)

3372

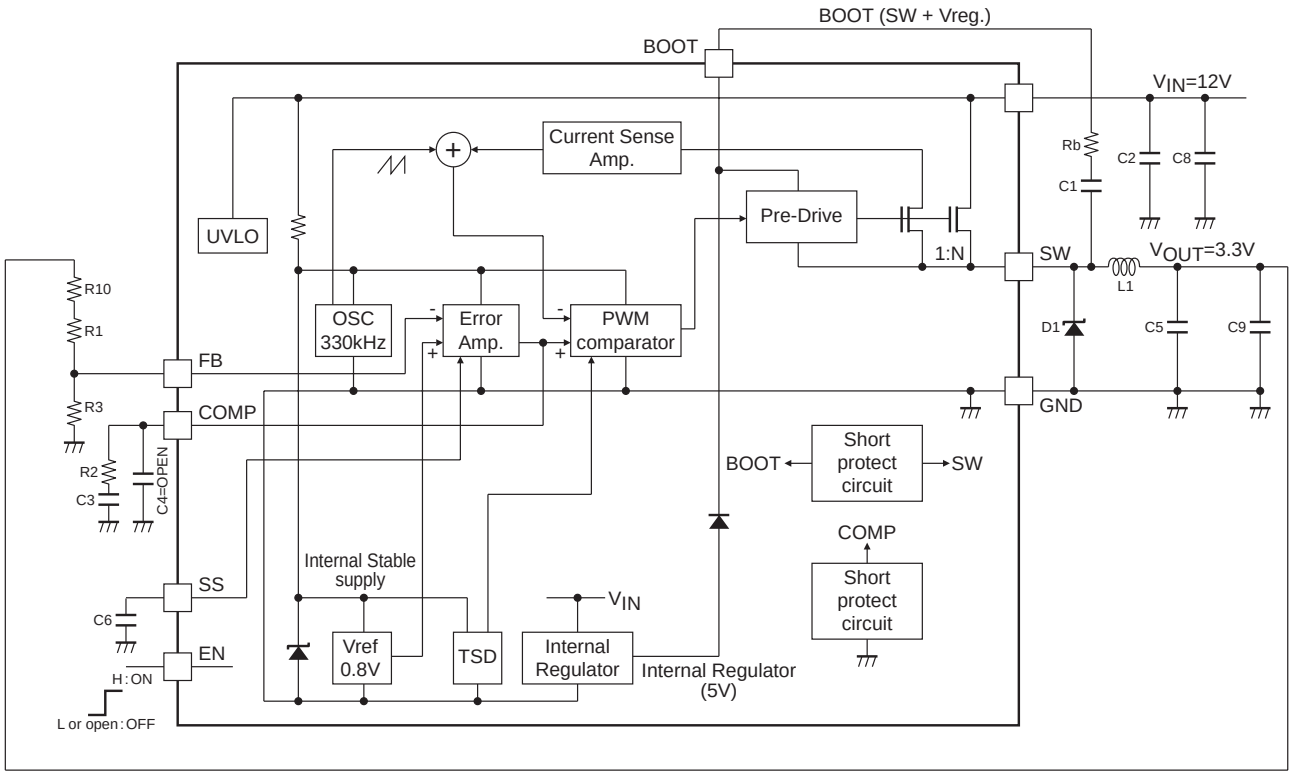




Pin Assignment

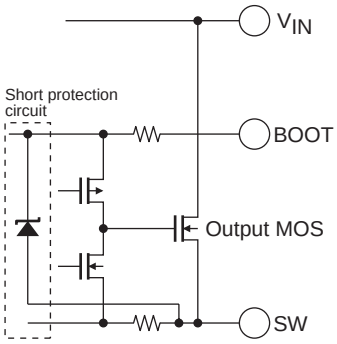
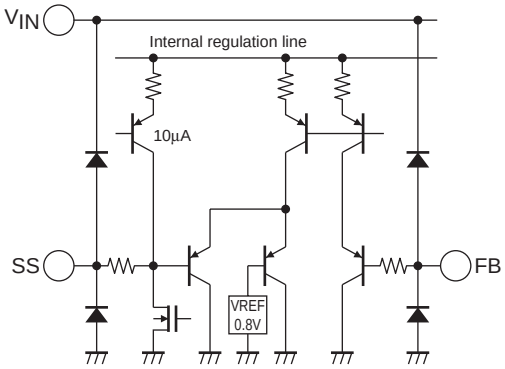
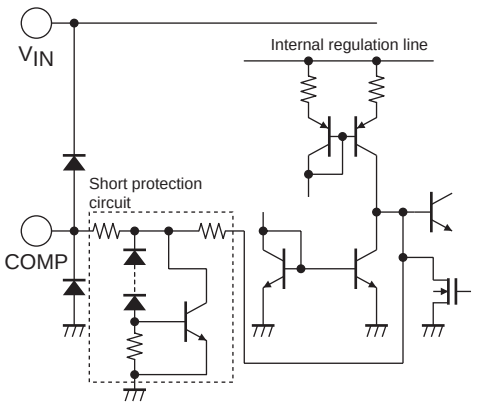
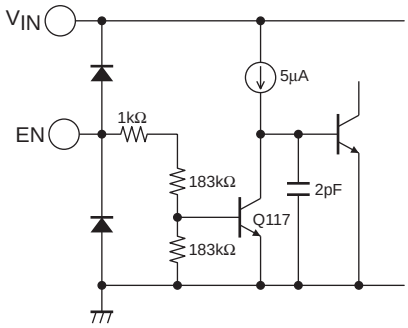


Block Diagram and Sample Application Circuit (3.3V output)



• C1,C8,C5,C9 = ceramic capacitor used.

Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	BOOT	Upper MOS transistor boot strap capacitance connection pin. Connect the boot capacitance of about 0.022μF between SW pins. To protect the SW pin's absolute maximum rating, to ensure stable operation, and to eliminate noise, the boot capacitance serial resistance (about 100Ω) Rb proves effective.	
2	V_{IN}	Input voltage pin. Connect substantially large (10μF 2 parallel or more) capacitance between this pin and GND.	
3	SW	Power switch pin. Connect the output LC filter. Connect the above capacitance between this pin and BOOT pin.	
4	GND	Ground pin.	
5	FB	Feedback pin. Sets the output voltage by means of split resistor in the section of the output voltage V_{OUT} - FB - GND. V_{OUT} setting is made as calculated below: $V_{OUT} = Vref \times \{ 1 + \frac{(R1 + R10)}{R3} \}$ Vref = 0.8V Example: 3.3V output voltage (See Block Diagram and Sample Application Circuit) $V_{OUT} = Vref \times \{ 1 + \frac{(27k + 4.3k)}{10k} \}$ =3.304V	
8	SS	Soft start pin. Sets the soft start time by means of the built-in 10μA source voltage and external soft start capacity. The soft start capacity C6 can be set as follows: $C6 = 10\mu A \times \frac{Tss}{Vref}$ Where, Tss is the soft start time and Vref is the reference voltage. Example: 1.2ms soft start time achieved $C6 = 10\mu A \times \frac{1.2ms}{0.8V} = 0.015\mu F$	
6	COMP	Phase compensation pin. Connects with the phase compensation external capacitance and resistance of DC/DC converter close loop.	
7	EN	Enable pin. Converter enabled when set to the HIGH voltage and disabled when LOW voltage or OPEN state.	

Considerations for the design

- During use with V_{IN} = 12V or less, the boot strap voltage may become deficient due to intermittent operation at no load, resulting in failure of normal operation. In this case, insert a resistance of about 500Ω between V_{OUT} and GND and avoid the intermittent operation mode during use.

- Insertion of serial beads in the Schottky diode for removal of noise may cause generation of the negative voltage deviating from the absolute maximum rating at the SW pin, resulting in failure of normal operation. In such an event, do not insert beads as above described and, instead, remove noise by means of the BOOT resistance Rb.

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