DS90LV031A

DS90LV031A 3V LVDS Quad CMOS Differential Line Driver

![Texas Instruments logo]

National Semiconductor

DS90LV031A

3V LVDS Quad CMOS Differential Line Driver

General Description

The DS90LV031A is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV031A accepts low voltage LVTTL/LVCMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 13 mW typical.

The EN and EN* inputs allow active Low or active High control of the TRI-STATE outputs. The enables are common to all four drivers. The DS90LV031A and companion line receiver (DS90LV032A) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.
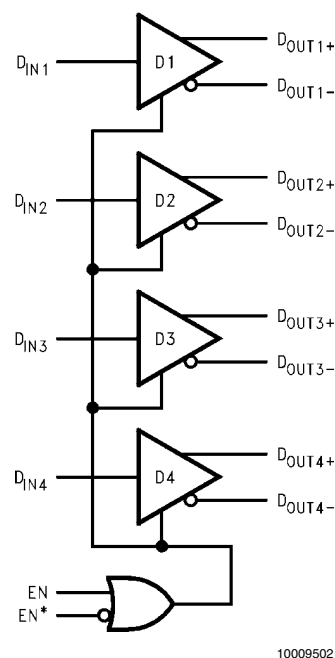
Features

■ >400 Mbps (200 MHz) switching rates
■ 0.1 ns typical differential skew
■ 0.4 ns maximum differential skew
■ 2.0 ns maximum propagation delay
■ 3.3V power supply design
■ ±350 mV differential signaling
■ Low power dissipation (13mW at 3.3V static)
■ Interoperable with existing 5V LVDS devices
■ Compatible with IEEE 1596.3 SCI LVDS standard
■ Compatible with TIA/EIA-644 LVDS standard
■ Industrial operating temperature range
■ Available in SOIC and TSSOP surface mount packaging

Connection Diagram

Dual-In-Line

10009501

**Order Number DS90LV031ATM
or DS90LV031ATMTC
See NS Package Number M16A or MTC16**
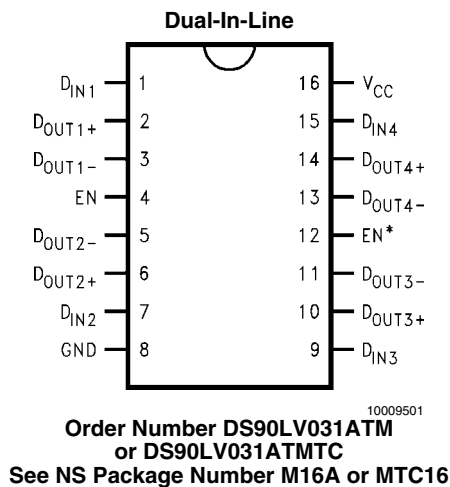
Functional Diagram

10009502

Truth Table

Enables		Input	Outputs	
EN	**EN***	D_{IN}	D_{OUT+}	D_{OUT-}
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
Input Voltage (D_{IN})	−0.3V to (V_{CC} + 0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage (D_{OUT+}, $D_{OUT−}$)	−0.3V to +3.9V
Short Circuit Duration	
(D_{OUT+}, $D_{OUT−}$)	Continuous
Maximum Package Power Dissipation @ +25°C	
M Package	1088 mW
MTC Package	866 mW
Derate M Package	8.5 mW/°C above +25°C
Derate MTC Package	6.9 mW/°C above +25°C

Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Junction Temperature	+150°C
ESD Rating (*Note 10*)	
(HBM, 1.5 kΩ, 100 pF)	≥ 6 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
Operating Free Air Temperature (T_A)				
Industrial	−40	+25	+85	°C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (*Note 2*, *Note 3*, *Note 4*)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Output Voltage	R_L = 100Ω (*Figure 1*)	$D_{OUT−}$ D_{OUT+}	250	350	450	mV
ΔV_{OD1}	Change in Magnitude of V_{OD1} for Complementary Output States				4	35	|mV|
V_{OS}	Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				5	25	|mV|
V_{OH}	Output Voltage High				1.38	1.6	V
V_{OL}	Output Voltage Low			0.90	1.03		V
V_{IH}	Input Voltage High		D_{IN}, EN, EN*	2.0		V_{CC}	V
V_{IL}	Input Voltage Low			GND		0.8	V
I_{IH}	Input Current	V_{IN} = V_{CC} or 2.5V		−10	±1	+10	µA
I_{IL}	Input Current	V_{IN} = GND or 0.4V		−10	±1	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5	−0.8		V
I_{OS}	Output Short Circuit Current	ENABLED, (*Note 11*) D_{IN} = V_{CC}, D_{OUT+} = 0V or D_{IN} = GND, $D_{OUT−}$ = 0V	$D_{OUT−}$ D_{OUT+}		−6.0	−9.0	mA
I_{OSD}	Differential Output Short Circuit Current	ENABLED, V_{OD} = 0V (*Note 11*)			−6.0	−9.0	mA
I_{OFF}	Power-off Leakage	V_{OUT} = 0V or 3.6V, V_{CC} = 0V or Open		−20	±1	+20	µA
I_{OZ}	Output TRI-STATE Current	EN = 0.8V and EN* = 2.0V V_{OUT} = 0V or V_{CC}		−10	±1	+10	µA
I_{CC}	No Load Supply Current Drivers Enabled	D_{IN} = V_{CC} or GND	V_{CC}		5.0	8.0	mA
I_{CCL}	Loaded Supply Current Drivers Enabled	R_L = 100Ω All Channels, D_{IN} = V_{CC} or GND (all inputs)			23	30	mA
I_{CCZ}	No Load Supply Current Drivers Disabled	D_{IN} = V_{CC} or GND, EN = GND, EN* = V_{CC}			2.6	6.0	mA

Switching Characteristics - Industrial

V_{CC} = +3.3V ±10%, T_A = −40°C to +85°C (*Note 3*, *Note 9*, *Note 12*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 10 pF (*Figure 2* and *Figure 3*)	0.8	1.18	2.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.8	1.25	2.0	ns
t_{SKD1}	Differential Pulse Skew It_{PHLD} − t_{PLHD}I (*Note 5*)		0	0.07	0.4	ns
t_{SKD2}	Channel-to-Channel Skew (*Note 6*)		0	0.1	0.5	ns
t_{SKD3}	Differential Part to Part Skew (*Note 7*)		0		1.0	ns
t_{SKD4}	Differential Part to Part Skew (*Note 8*)		0		1.2	ns
t_{TLH}	Rise Time			0.38	1.5	ns
t_{THL}	Fall Time			0.40	1.5	ns
t_{PHZ}	Disable Time High to Z	R_L = 100Ω, C_L = 10 pF (*Figure 4* and *Figure 5*)			5	ns
t_{PLZ}	Disable Time Low to Z				5	ns
t_{PZH}	Enable Time Z to High				7	ns
t_{PZL}	Enable Time Z to Low				7	ns
f_{MAX}	Maximum Operating Frequency (*Note 14*)		200	250		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.

Note 3: All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.

Note 4: The DS90LV031A is a current mode device and only functions within datasheet specifications when a resistive load is applied to the driver outputs typical range is (90Ω to 110Ω)

Note 5: t_{SKD1}, It_{PHLD} − t_{PLHD}I is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 6: t_{SKD2} is the Differential Channel-to-Channel Skew of any event on the same device.

Note 7: t_{SKD3}, Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

Note 8: t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as IMax − MinI differential propagation delay.

Note 9: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r ≤ 1 ns, and t_f ≤ 1 ns.

Note 10: ESD Ratings:
  HBM (1.5 kΩ, 100 pF) ≥ 6 kV

Note 11: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Note 12: C_L includes probe and jig capacitance.

Note 13: All input voltages are for one channel unless otherwise specified. Other inputs are set to GND.

Note 14: f_{MAX} generator input conditions: t_r = t_f < 1ns, (0% to 100%), 50% duty cycle, 0V to 3V. Output Criteria: duty cycle = 45%/55%, VOD > 250mV, all channels switching.
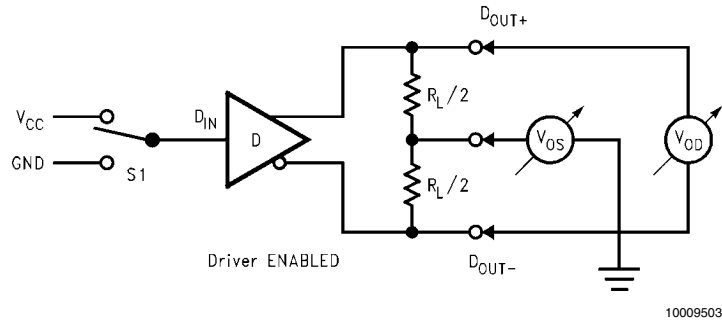
Parameter Measurement Information
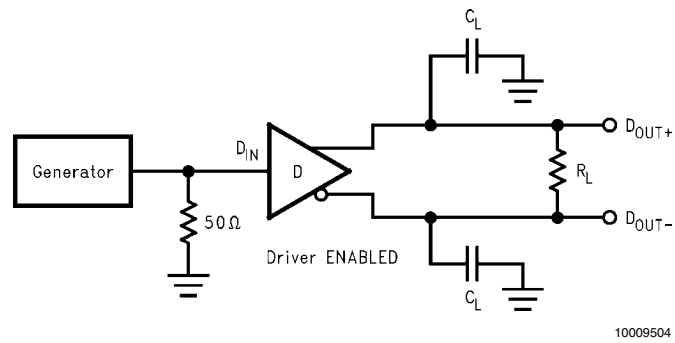

10009503

FIGURE 1. Driver V_{OD} and V_{OS} Test Circuit

10009504

FIGURE 2. Driver Propagation Delay and Transition Time Test Circuit

10009505

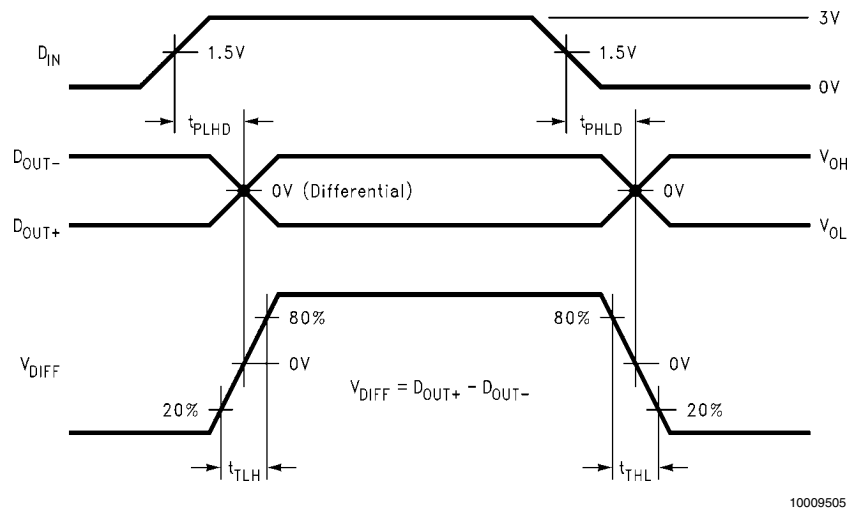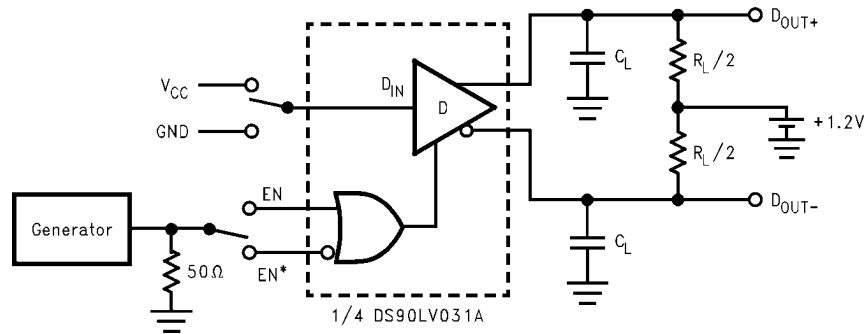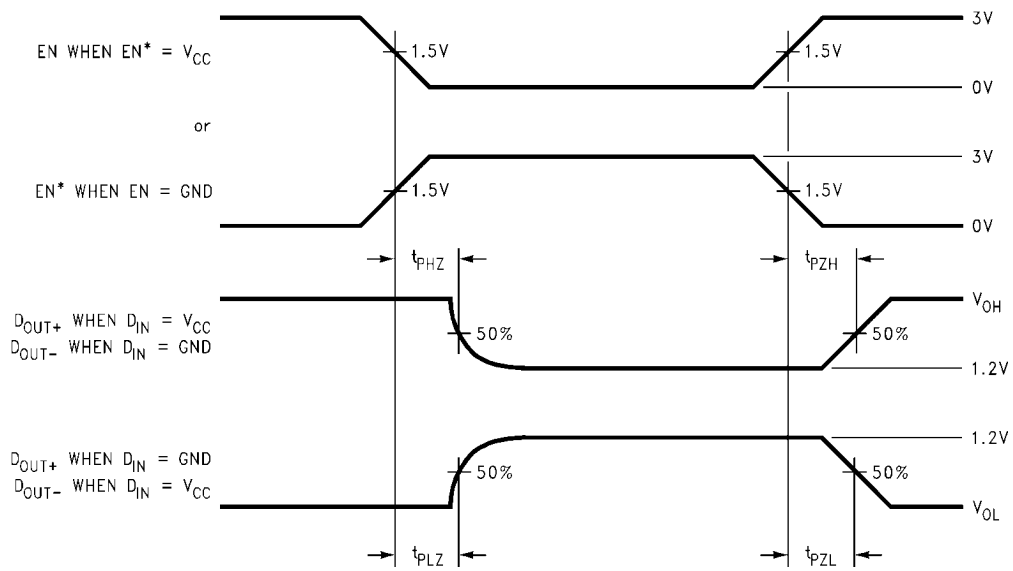**FIGURE 3. Driver Propagation Delay and Transition Time Waveforms**

FIGURE 4. Driver TRI-STATE Delay Test Circuit

FIGURE 5. Driver TRI-STATE Delay Waveform

Applications Information

General application guidelines and hints for LVDS drivers and receivers may be found in the following application notes: LVDS Owner's Manual (lit #550062-001), AN808, AN1035, AN977, AN971, AN916, AN805, AN903.

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 7*. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic differential impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90LV031A differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The output current is typically 3.5 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in *Figure 7*. AC or unterminated configurations are not allowed. The 3.5 mA loop current will develop a differential voltage of 350 mV across the 100Ω termination resistor which the receiver detects with a 250 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (350 mV − 100 mV = 250 mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in *Figure 6*. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 700 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

The footprint of the DS90LV031A is the same as the industry standard 26LS31 Quad Differential (RS-422) Driver and is a step down replacement for the 5V DS90C031 Quad Driver.

Power Decoupling Recommendations:

Bypass capacitors must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1µF in parallel with 0.01µF, in parallel with 0.001µF at the power supply pin as well as scattered capacitors over the printed circuit board. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board.

PC Board considerations:

Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

Differential Traces:

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. Lab experiments show that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is greater with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

Termination:

Use a resistor which best matches the differential impedance of your transmission line. The resistor should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination. Typically, connect a single resistor across the pair at the receiver end.

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm MAX).

Probing LVDS Transmission Lines:

Always use high impedance (> 100kΩ), low capacitance (< 2pF) scope probes with a wide bandwidth (1GHz) scope. Improper probing will give deceiving results.

Cables and Connectors, General Comments:

When choosing cable and connectors for LVDS it is important to remember:

Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax.) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differen-

tial mode) noise which is rejected by the receiver. For cable distances < 0.5M, most cables can be made to work effectively. For distances 0.5M ≤ d ≤ 10M, CAT 3 (category 3) twisted pair cable works well, is readily available and relatively inexpensive.

Fail-safe of an LVDS Interface

If the LVDS link as shown in *Figure 7* needs to support the case where the Line Driver is disabled, powered off, or removed (un-plugged) and the Receiver device is powered on and enabled, the state of the LVDS bus is unknown and therefore the output state of the Receiver is also unknown. If this is of concern, please consult the respective LVDS Receiver data sheet for guidance on Failafe Biasing options for the LVDS interface to set a known state on the inputs for these conditions.
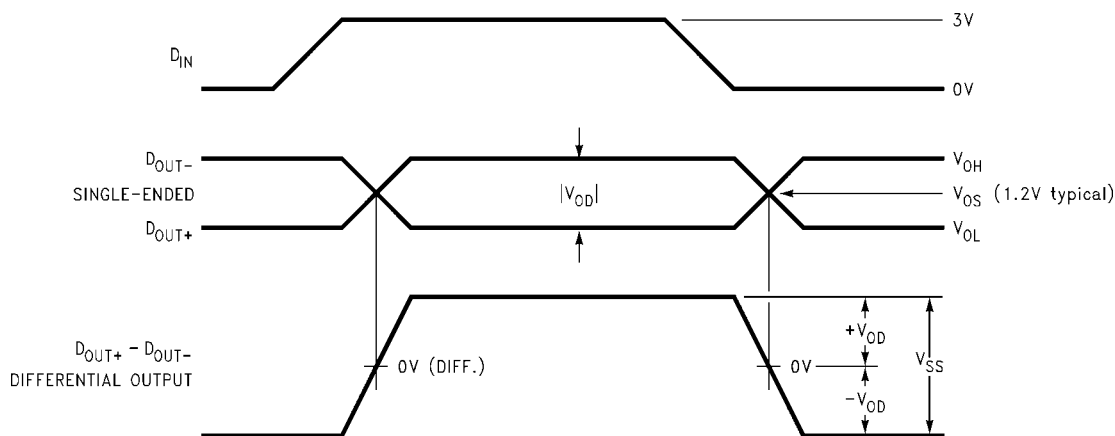
10009509

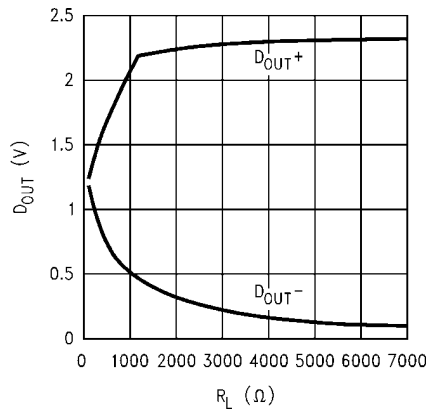**FIGURE 6. Driver Output Levels**

Typical Application
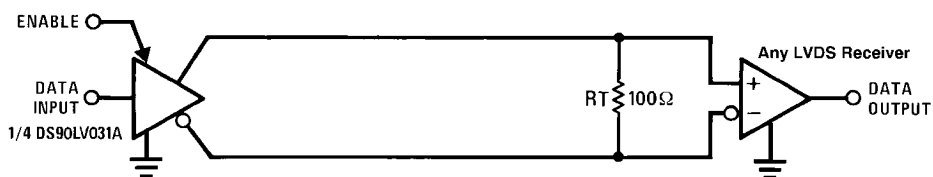
10009508

FIGURE 7. Point-to-Point Application

Typical Performance Curves
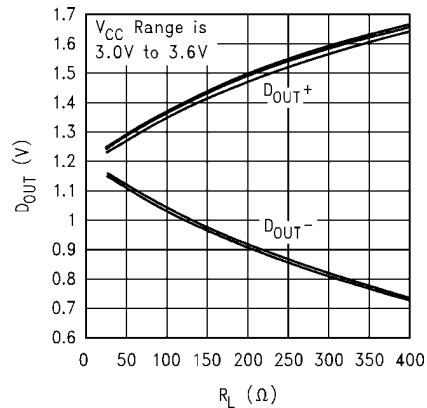
10009510

FIGURE 8. Typical DS90LV031A, D_{OUT} (single ended) vs R_L, $T_A = 25°C$

10009511

**FIGURE 9. Typical DS90LV031A, D_{OUT} vs R_L,
$V_{CC} = 3.3V$, $T_A = 25°C$**

Pin Descriptions

Pin No.	Name	Description
1, 7, 9, 15	D_{IN}	Driver input pin, TTL/CMOS compatible
2, 6, 10, 14	D_{OUT+}	Non-inverting driver output pin, LVDS levels
3, 5, 11, 13	D_{OUT-}	Inverting driver output pin, LVDS levels
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +3.3V ± 0.3V
8	GND	Ground pin

Ordering Information

Package Type	Package Number	Order Number
SOP	M16A	DS90LV031ATM
TSSOP	MTC16	DS90LV031ATMTC

Physical Dimensions inches (millimeters) unless otherwise noted

0.386 − 0.394
(9.804 − 10.00)

16 15 14 13 12 11 10 9

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO.1
IDENT

1 2 3 4 5 6 7 8

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020
(0.356 − 0.508) TYP

M16A (REV H)

16-Lead (0.150 Wide) Molded Small Outline Package, JEDEC
Order Number DS90LV031ATM
NS Package Number M16A

A

5 ± 0.1

16   9

B

6.4

3.2

4.4 ± 0.1

1   8

PIN #1 ID

⌓ 0.2 C B A
ALL LEAD TIPS

SYMM
℄

SYMM
℄

(5.94)

(16X 1.78)

(16X 0.42)

(14X 0.65)
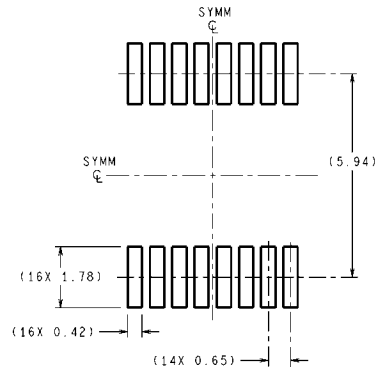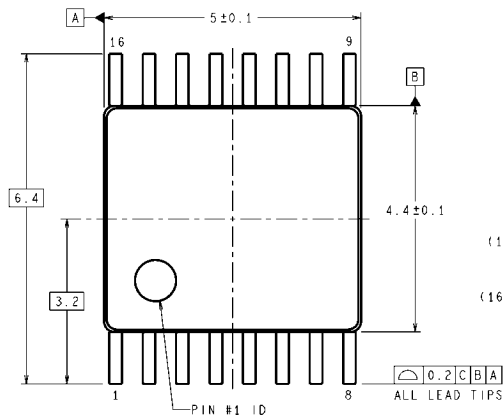
RECOMMENDED LAND PATTERN

GAGE PLANE

0.25

0° - 8°

0.6 ± 0.1

SEATING PLANE

DETAIL A
TYPICAL

1.1 MAX
TYP

(0.9)

C

⌓ 0.1 C
ALL LEAD TIPS

16X 0.19-0.30

14X 0.65

⊕ 0.13 Ⓜ A BⓈ CⓈ

0.1 ± 0.05 TYP

SEE DETAIL A

16X
0.09-0.20
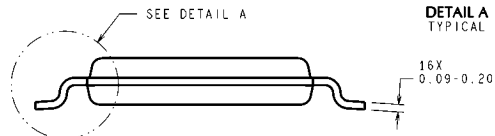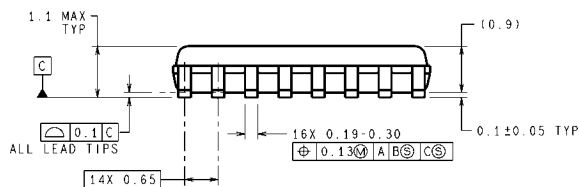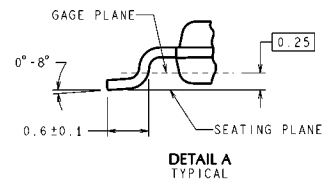
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MTC16 (Rev D)

16-Lead (0.100 Wide) Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90LV031ATMTC
NS Package Number MTC16

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:
www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

National Semiconductor Americas Technical Support Center Email: support@nsc.com Tel: 1-800-272-9959	**National Semiconductor Europe Technical Support Center** Email: europe.support@nsc.com	**National Semiconductor Asia Pacific Technical Support Center** Email: ap.support@nsc.com	**National Semiconductor Japan Technical Support Center** Email: jpn.feedback@nsc.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		

TI E2E Community Home Page   e2e.ti.com