

SONY CXK581100TM/YM -10LX/12LX/15LX -10LLX/12LLX/15LLX

131072-word × 8-bit High Speed CMOS Static RAM

Description

CXK581100TM/YM is a 1M bits, 131,072 words by 8 bits, CMOS static RAM. It is suitable for portable and battery back-up systems by adopting TSOP packages correspond to extending operating temperature range and low power consumption.

Features

- Extended operating temperature range (-25 to +85 °C)
- Thin small-outline packages of EIAJ standard:
CXK581100TM:
8mm × 20mm 32 pin TSOP
CXK581100YM:
8mm × 20mm 32 pin TSOP (Mirror image pinout)
- Low stand-by current:
LX-Version:
200 µA (Max.) @Vcc=5.5V, Ta=-25 to +85 °C
LLX-Version:
40 µA (Max.) @Vcc=5.5V, Ta=-25 to +85 °C
- Low voltage data retention: 2.2V (Min.)
- Fast access time: (Access time)
CXK581100TM/YM-10LX, -10LLX 100ns (Max.)
CXK581100TM/YM-12LX, -12LLX 120ns (Max.)
CXK581100TM/YM-15LX, -15LLX 150ns (Max.)
- Single +5V Supply: +5V ± 10%

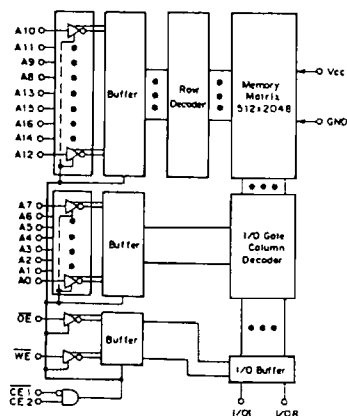
Function

131072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram



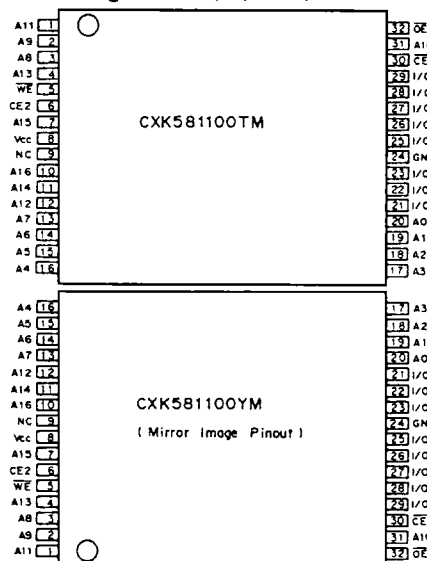
CXK581100TM 32 pin TSOP (Plastic) CXK581100YM 32 pin TSOP (Plastic)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Pin Configuration (Top View)



Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	-25 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	235 • 10	°C • sec

* V_{IN}, V_{I/O}=-3.0V Min. for pulse width less than 50ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta=-25 to +85°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.4	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.6	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=-25 to +85 °C)

Item	Symbol	Test conditions		-10LX/12LX/15LX			-10LLX/12LLX/15LLX			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}		-1	—	1	-1	—	1	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} , V _{I/O} =GND to V _{CC}		-1	—	1	-1	—	1	μA
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} , V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA		—	7	15	—	7	15	mA
Average operating current	I _{CC2}	Cycle=Min. Duty=100%, I _{OUT} =0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty=100%, I _{OUT} =0mA CE1 ≤ 0.2V, CE2 ≥ V _{CC} -0.2V V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} -0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} -0.2V CE2 ≥ V _{CC} -0.2V	-25 to +85 °C	—	—	200	—	—	40	μA
			-25 to +70 °C	—	—	100	—	—	20	
			-25 to +40 °C	—	—	20	—	—	4	
			+25 °C	—	2	8	—	0.7	2	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	0.6	3	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} =-1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O Capacitance

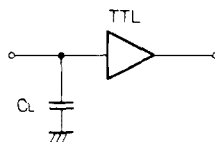
(T_a=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics**● AC test conditions**(V_{CC}=5V ± 10%, T_a=-25 to +85 °C)

Item	Conditions
Input pulse high level	V _{IH} =2.4V
Input pulse low level	V _{IL} =0.6V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load conditions	C _L * ≈100pF, 1TTL

* C_L includes scope and jig capacitances

• Read cycle ($\overline{WE}$ ="H")

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	trc	100	—	120	—	150	—	ns
Address access time	tAA	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	tco1	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE2}$)	tco2	—	100	—	120	—	150	ns
Output enable to output valid	toE	—	50	—	60	—	70	ns
Output hold from address change	toH	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, $\overline{CE2}$)	tlZ1, tlZ2	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	tolZ	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, $\overline{CE2}$)	thZ1*, thZ2*	—	35	—	40	—	50	ns
Chip disable to output in high Z ($\overline{OE}$)	toH* *	—	35	—	40	—	50	ns

* thZ1, thZ2 and toH are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

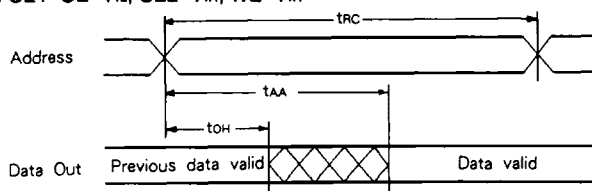
• Write cycle

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	twc	100	—	120	—	150	—	ns
Address valid to end of write	taw	70	—	85	—	100	—	ns
Chip enable to end of write	tcw	70	—	85	—	100	—	ns
Data to write time overlap	tdw	40	—	50	—	60	—	ns
Data hold from write time	tdH	0	—	0	—	0	—	ns
Write pulse width	tWP	70	—	80	—	90	—	ns
Address setup time	tAs	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	tWR	5	—	5	—	5	—	ns
Write recovery time ($\overline{CE1}$, $\overline{CE2}$)	tWR1	0	—	0	—	0	—	ns
Output active from end of write	tow	10	—	10	—	10	—	ns
Write to output in high Z	twhZ *	—	30	—	30	—	30	ns

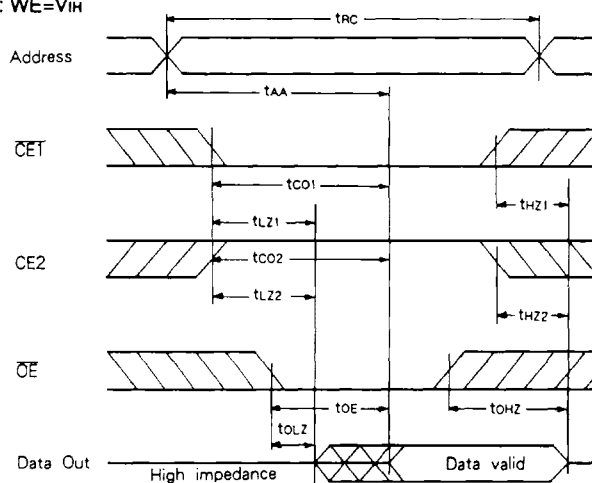
* twhZ is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$

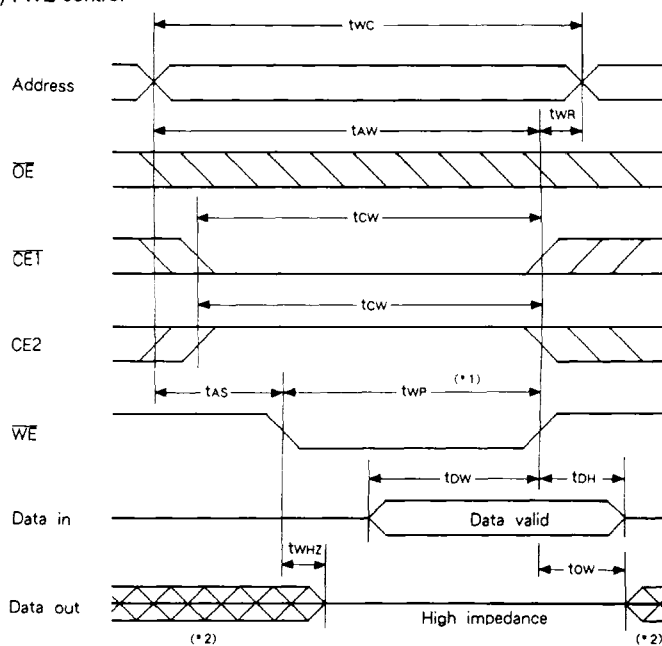
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



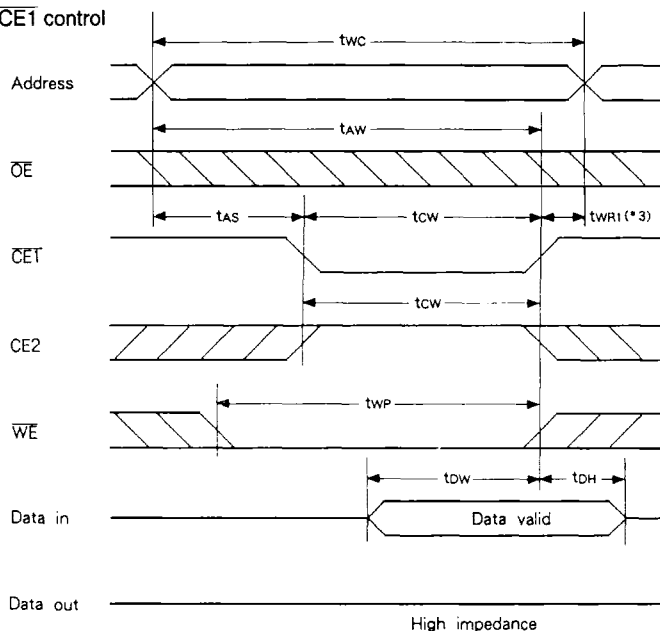
- Read cycle (2) : $\overline{WE}=V_{IH}$



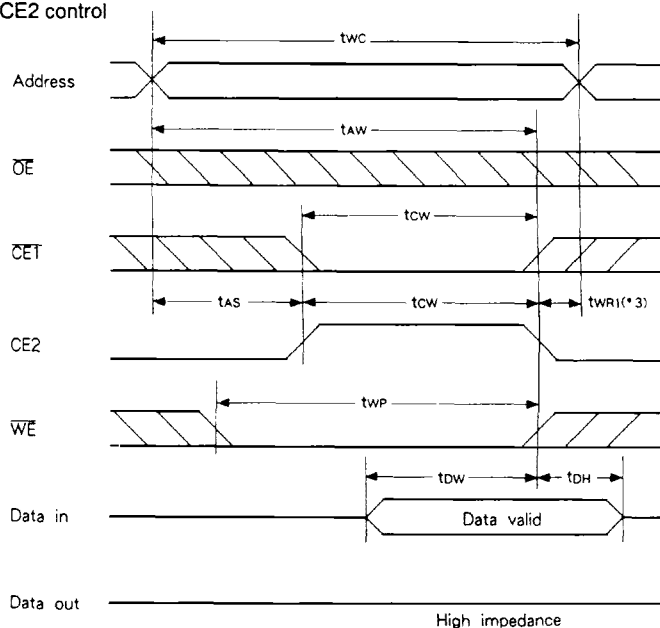
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control



- * 1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and CE2 is at high simultaneously.
- * 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- * 3. t_{WR1} is tested from either the rising edge of $\overline{\text{CE1}}$ or the falling edge of CE2 , whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

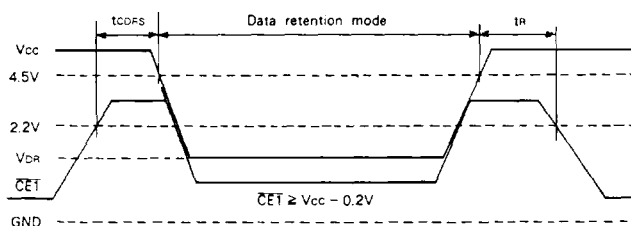
(Ta = -25 to +85 °C)

Item	Symbol	Test conditions	-10LX/12LX/15LX			-10LLX/12LLX/15LLX			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	* 1	2.2	—	5.5	2.2	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V * 1	-25 to +85 °C	—	100	—	—	24	μA
			-25 to +70 °C	—	50	—	—	12	
			-25 to +40 °C	—	10	—	—	2.4	
			+25 °C	—	1	—	0.4	1.2	
	I _{CCDR2}	V _{CC} =2.2 to 5.5V * 1	—	2 * 3	200	—	0.7 * 3	40	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _R		t _{RC} * 2	—	—	t _{RC} * 2	—	—	ns

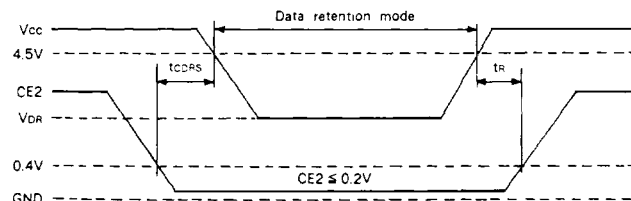
* 1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)* 2. t_{RC}: Read cycle time* 3. V_{CC}=5V, Ta=25 °C

Data Retention Waveform

- Low supply voltage data retention waveform (1) : $\overline{CE1}$ control



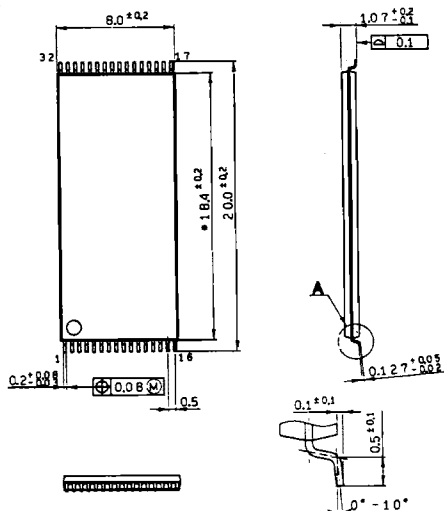
- Low supply voltage data retention waveform (2) : $CE2$ control



Package Outline Unit: mm

CXK581100TM

32pin TSOP (Plastic)

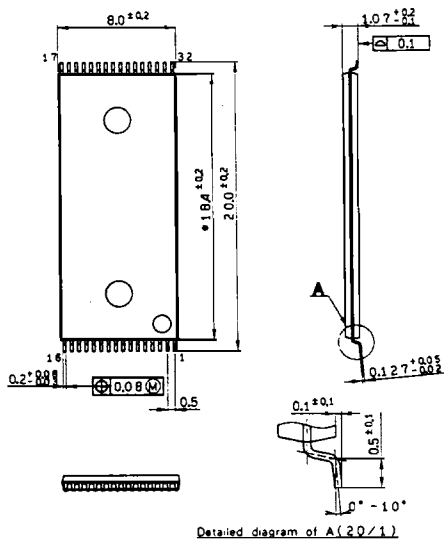


Note) Dimensions marked with *
does not include resin residue.

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP032-P-0820-A
JEDEC CODE	

CXK581100YM

32pin TSOP (Plastic)



Note) Dimensions marked with *
does not include resin residue.

SONY NAME	TSOP-32P-L01R
EIAJ NAME	TSOP032-P-0820-B
JEDEC CODE	