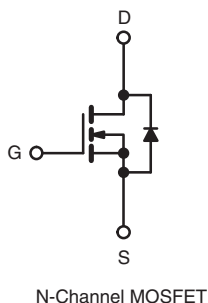
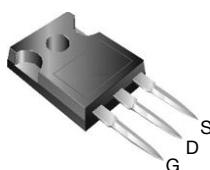


## E Series Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	650	
$R_{DS(on)}$ max. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V	0.039
$Q_g$ max. (nC)	362	
$Q_{gs}$ (nC)	48	
$Q_{gd}$ (nC)	98	
Configuration	Single	

**TO-247AC**


### FEATURES

- Low Figure-of-Merit (FOM)  $R_{on} \times Q_g$
- Low Input Capacitance ( $C_{iss}$ )
- Reduced Switching and Conduction Losses
- Ultra Low Gate Charge ( $Q_g$ )
- Avalanche Energy Rated (UIS)
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### APPLICATIONS

- Switch Mode Power Supplies (SMPS)
- Power Factor Correction Power Supplies (PFC)
- Lighting
  - High-Intensity Discharge (HID)
  - Fluorescent Ballast Lighting
- Industrial
  - Welding
  - Induction Heating
  - Motor Drives
  - Battery Chargers
  - Renewable Energy
  - Solar (PV Inverters)

### ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	SiHG73N60E-E3
Lead (Pb)-free and Halogen-free	SiHG73N60E-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Gate-Source Voltage AC ( $f > 1$ Hz)		30	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	236	
Linear Derating Factor		4.2	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	2030	mJ
Maximum Power Dissipation	$P_D$	520	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Drain-Source Voltage Slope	$dV/dt$	$T_J = 125$ °C	V/ns
Reverse Diode $dV/dt$ <sup>d</sup>			
Soldering Recommendations (Peak Temperature)	for 10 s	300°	°C


#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DS} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 12$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 30$  A/ $\mu$ s, starting  $T_J = 25$  °C.

**THERMAL RESISTANCE RATINGS**

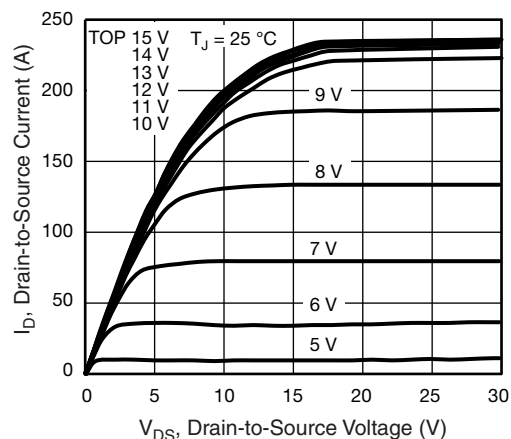
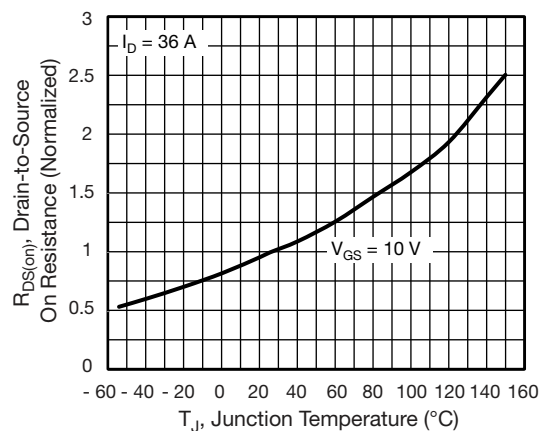
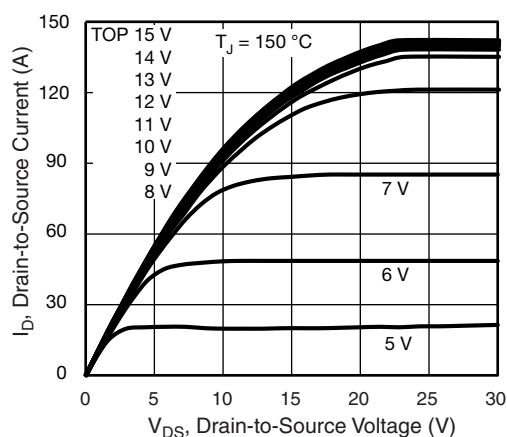
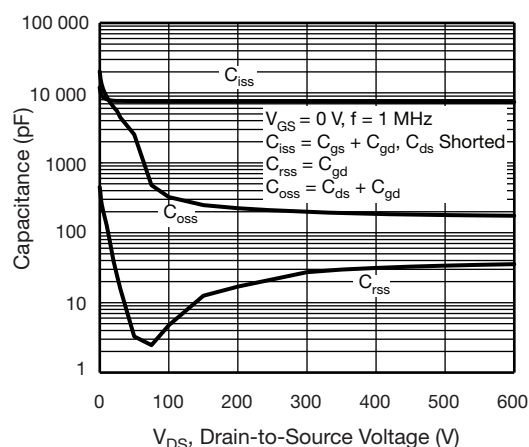
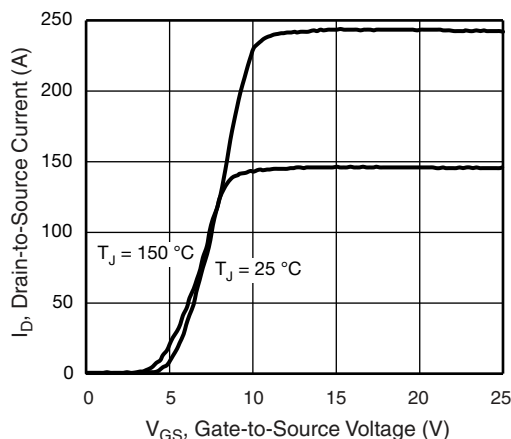
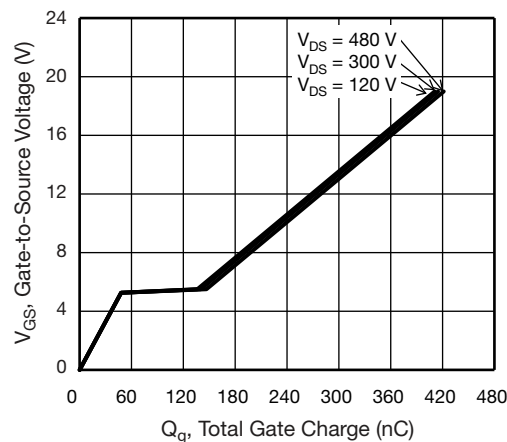
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.24	

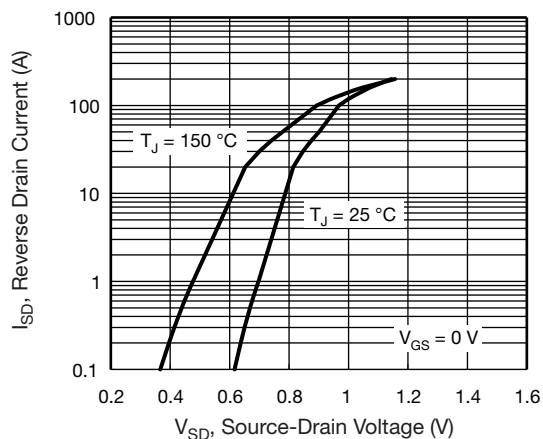
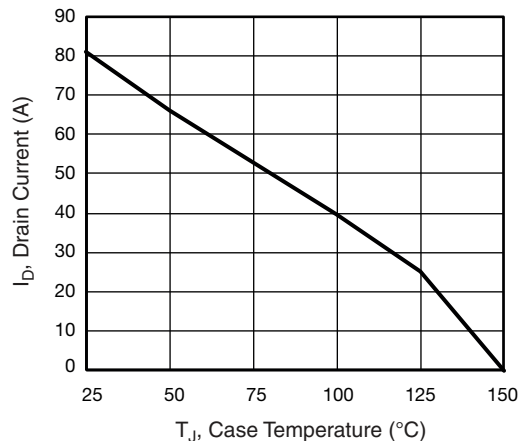
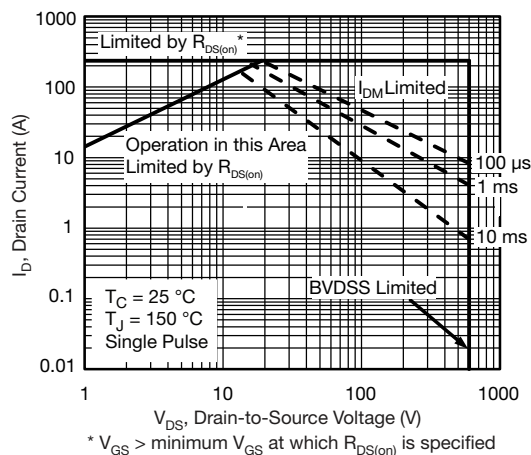
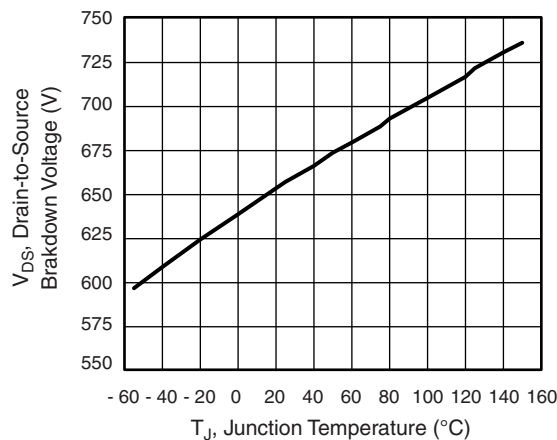
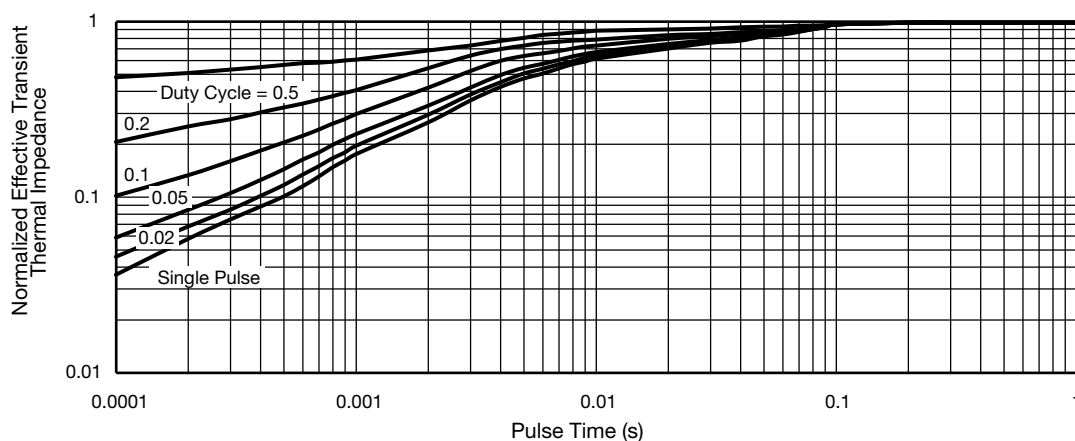
**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

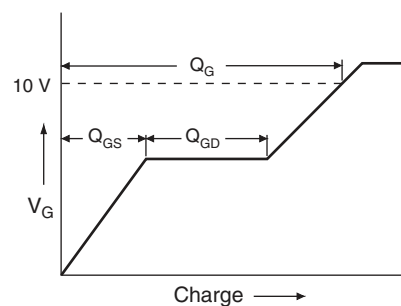
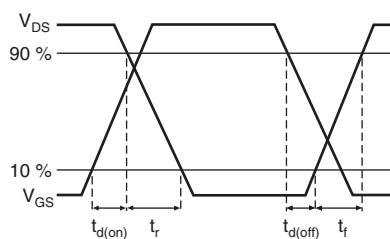
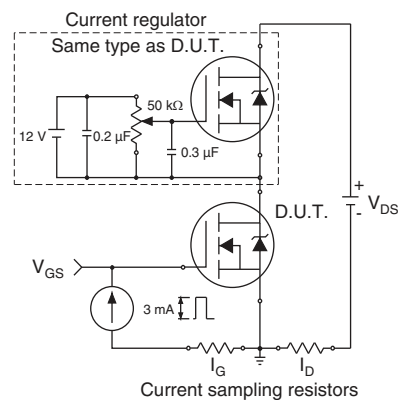
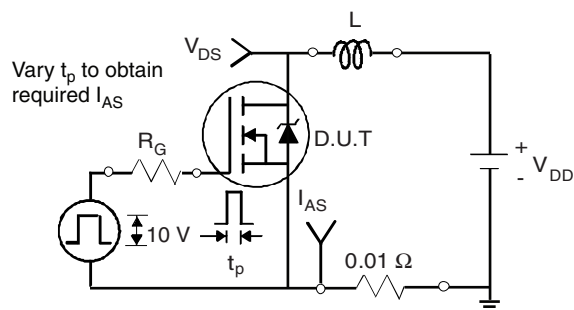
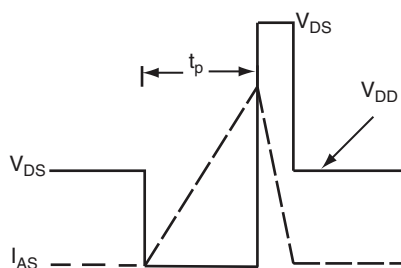
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$ , $I_D = 250\text{ }\mu\text{A}$	-	0.65	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^{\circ}\text{C}$	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 36\text{ A}$	-	0.032	0.039	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 40\text{ V}$ , $I_D = 10\text{ A}$	-	12	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$	-	7700	-	pF
Output Capacitance	$C_{oss}$		-	320	-	
Reverse Transfer Capacitance	$C_{rss}$		-	5	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	259	-	
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$		-	907	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$ , $I_D = 24\text{ A}$ , $V_{DS} = 480\text{ V}$	-	241	362	nC
Gate-Source Charge	$Q_{gs}$		-	48	-	
Gate-Drain Charge	$Q_{gd}$		-	98	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480\text{ V}$ , $I_D = 24\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_g = 10\text{ }\Omega$	-	63	95	ns
Rise Time	$t_r$		-	105	158	
Turn-Off Delay Time	$t_{d(off)}$		-	290	435	
Fall Time	$t_f$		-	120	180	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}$ , open drain	-	1.52	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	73	A
Pulsed Diode Forward Current	$I_{SM}$		-	-	200	
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_S = 36\text{ A}$ , $V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_F = I_S = 10\text{ A}$ , $dI/dt = 30\text{ A}/\mu\text{s}$ , $V_R = 50\text{ V}$	-	688	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	6.7	-	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$		-	19	-	A

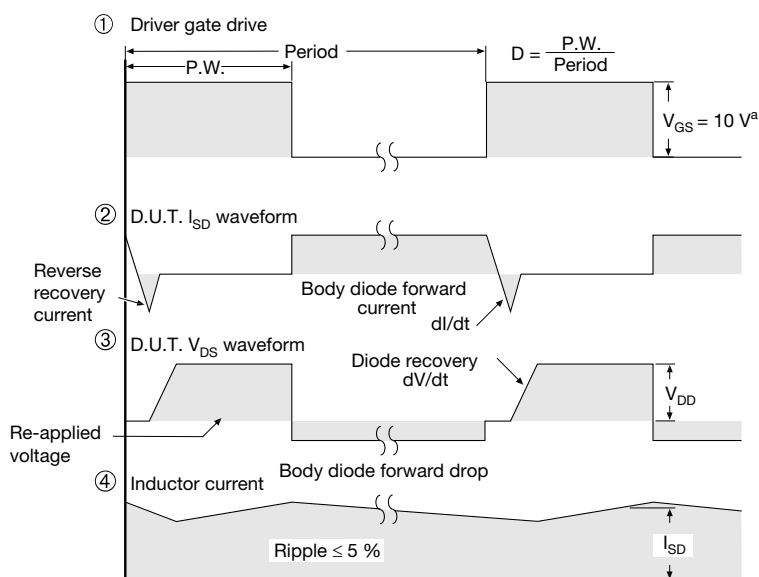
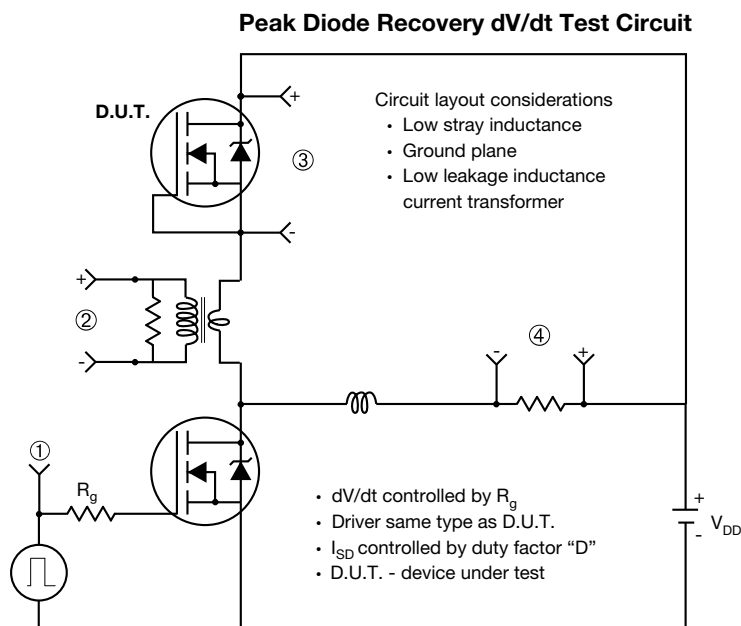
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .  
b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

**Fig. 9 - Maximum Drain Current vs. Case Temperature**

**Fig. 8 - Maximum Safe Operating Area**

**Fig. 10 - Temperature vs. Drain-to-Source Voltage**

**Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case**

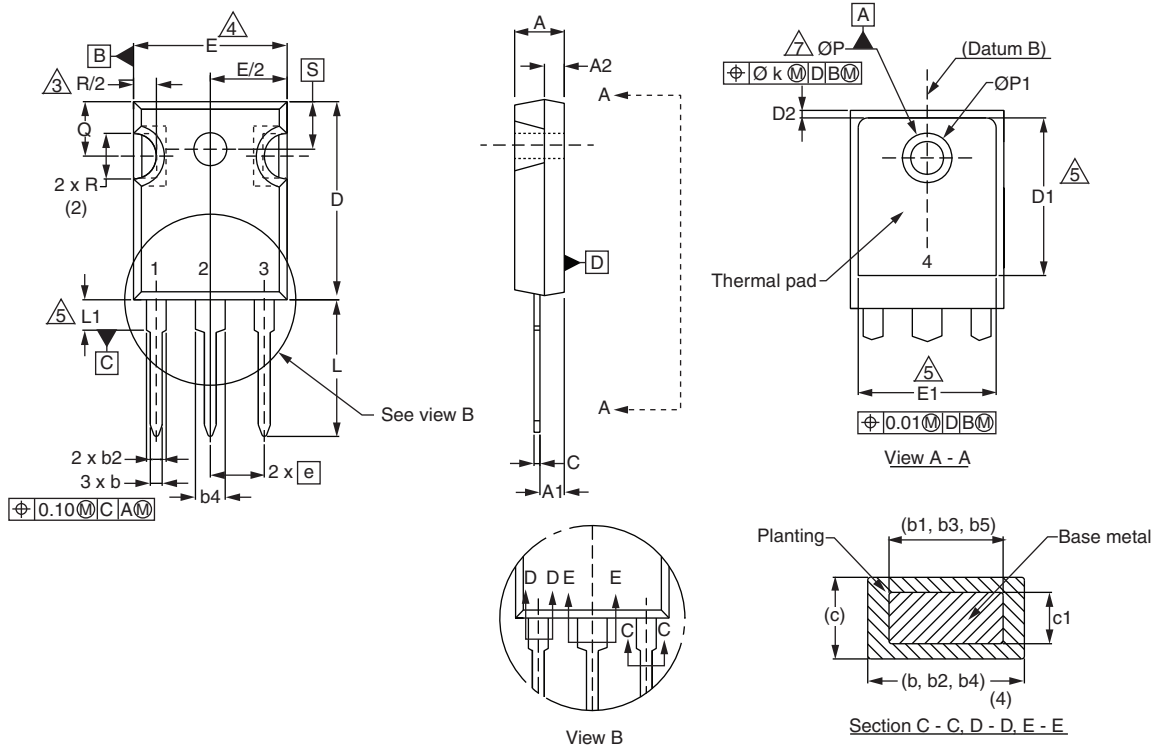

**Fig. 12 - Switching Time Test Circuit**

**Fig. 16 - Basic Gate Charge Waveform**

**Fig. 13 - Switching Time Waveforms**

**Fig. 17 - Gate Charge Test Circuit**

**Fig. 14 - Unclamped Inductive Test Circuit**

**Fig. 15 - Unclamped Inductive Waveforms**



**Fig. 18 - For N-Channel**

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## TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: X13-0045-Rev. C, 18-Mar-13  
DWG: 5971

### Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Contour of slot optional.
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
- Thermal pad contour optional with dimensions D1 and E1.
- Lead finish uncontrolled in L1.
- Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
- Outline conforms to JEDEC outline TO-247 with exception of dimension c.
- Xian and Mingxin actually photo.





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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

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