VISHAY®

New Product

P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY

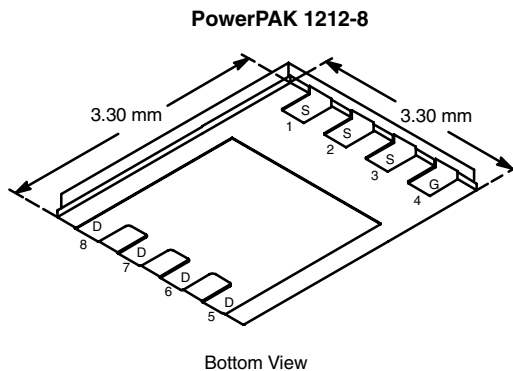| V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
− 12	0.012 at V_{GS} = − 4.5 V	− 15.6
	0.016 at V_{GS} = − 2.5 V	− 13.5
	0.024 at V_{GS} = − 1.8 V	− 11

FEATURES

- TrenchFET® Power MOSFETS: 1.8-V Rated
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
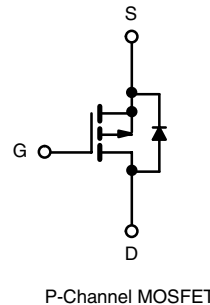- Ultra-Low $r_{DS(on)}$

Pb Available

RoHS* COMPLIANT

APPLICATIONS

- Load Switch
- PA Switch
- Battery Switch

PowerPAK 1212-8

3.30 mm   3.30 mm

Bottom View

Ordering Information: Si7407DN-T1
Si7407DN-T1–E3 (Lead (Pb)–free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	− 12		V
Gate-Source Voltage		V_{GS}	± 8		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	− 15.6	− 9.9	A
	T_A = 85 °C		− 11.2	− 7.2	
Pulsed Drain Current		I_{DM}	− 30		
Continuous Source Current (Diode Conduction)[a]		I_S	− 3.2	− 1.3	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	3.8	1.5	W
	T_A = 85 °C		2.0	0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	− 55 to 150		°C
Soldering Recommendations[b,c]			260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	26	33	°C/W
	Steady State		65	81	
Maximum Junction-to-Case	Steady State	R_{thJC}	1.9	2.4	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. See Solder Profile (*http://www.vishay.com/ppg?73257*). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

* Pb containing terminations are not RoHS compliant, exemptions may apply

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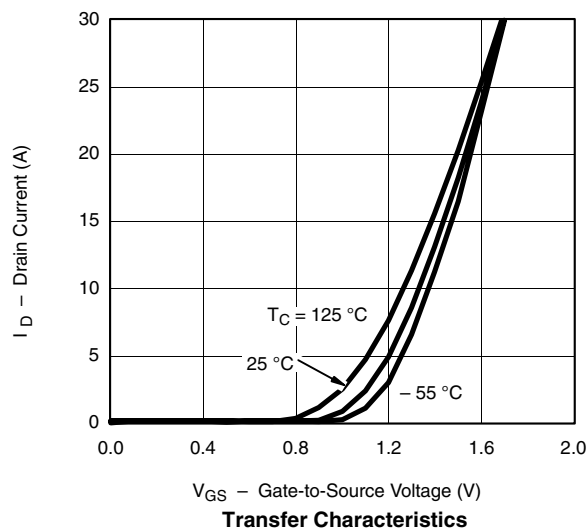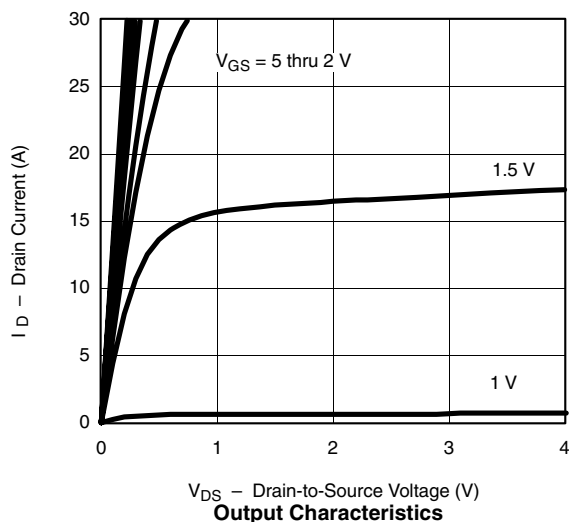## SPECIFICATIONS $T_J = 25\ °C$, unless otherwise noted

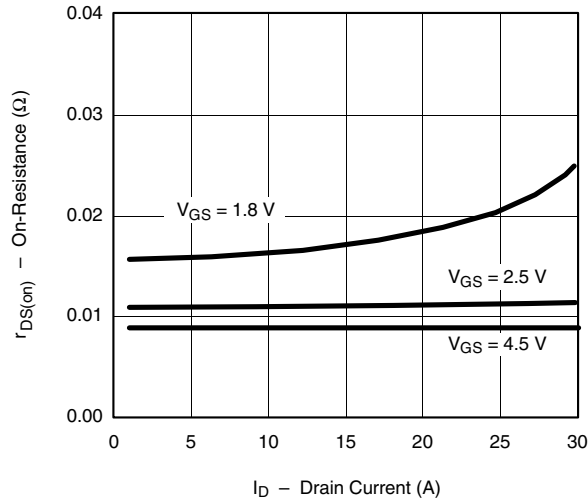| Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -400\ \mu A$	-0.40		-1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ V$, $V_{GS} = \pm 8\ V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\ V$, $V_{GS} = 0\ V$			-1	μA
		$V_{DS} = -12\ V$, $V_{GS} = 0\ V$, $T_J = 85\ °C$			-5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq -5\ V$, $V_{GS} = -4.5\ V$	-30			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = -4.5\ V$, $I_D = -15.6\ A$		0.009	0.012	Ω
		$V_{GS} = -2.5\ V$, $I_D = -13.5\ A$		0.013	0.016	
		$V_{GS} = -1.8\ V$, $I_D = -5\ A$		0.019	0.024	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -6\ V$, $I_D = -15.6\ A$		52		S
Diode Forward Voltage[a]	V_{SD}	$I_S = -3.2\ A$, $V_{GS} = 0\ V$		-0.7	-1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	$V_{DS} = -6\ V$, $V_{GS} = -4.5\ V$, $I_D = -15.6\ A$		39	59	nC
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			11		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\ V$, $R_L = 6\ \Omega$ $I_D \cong -1\ A$, $V_{GEN} = -4.5\ V$, $R_g = 6\ \Omega$		30	45	ns
Rise Time	t_r			50	75	
Turn-Off DelayTime	$t_{d(off)}$			200	300	
Fall Time	t_f			165	250	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -3.2\ A$, $di/dt = 100\ A/\mu s$		60	90	

Notes
a. Pulse test; pulse width $\leq 300\ \mu s$, duty cycle $\leq 2\ \%$.
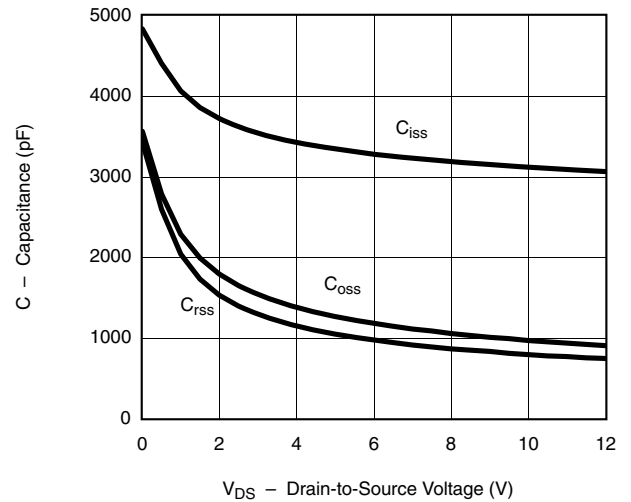b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $T_A = 25\ °C$, unless otherwise noted

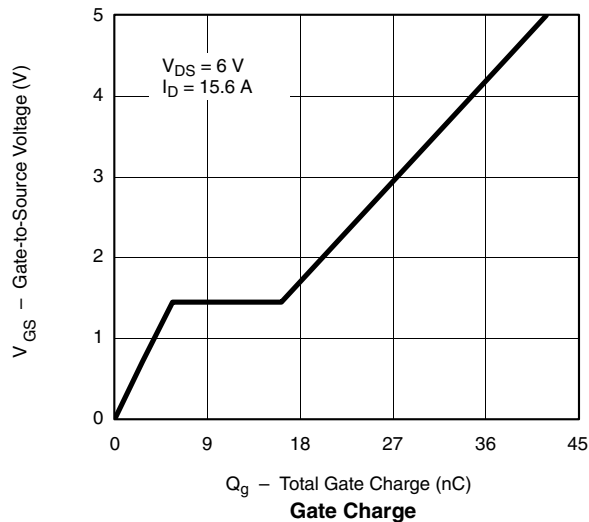**Output Characteristics**

Transfer Characteristics

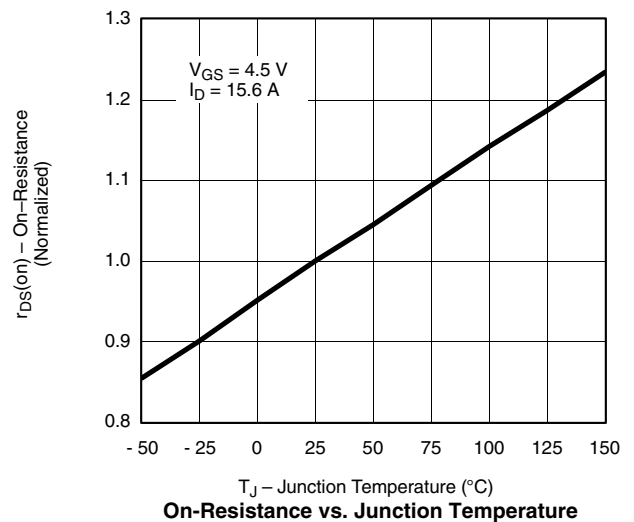**TYPICAL CHARACTERISTICS** T_A = 25 °C, unless otherwise noted

On-Resistance vs. Drain Current

Capacitance

Gate Charge

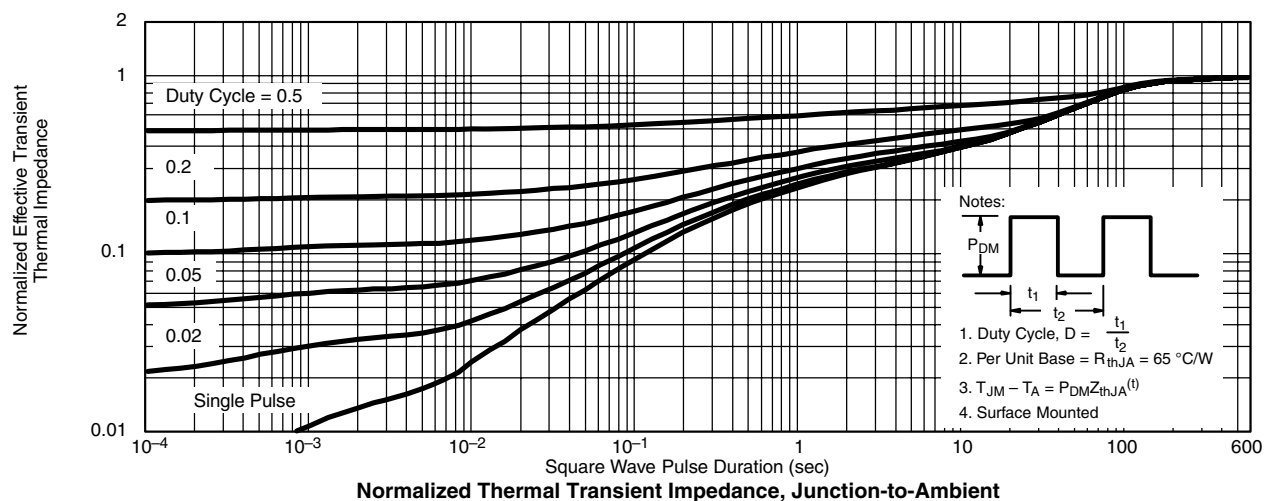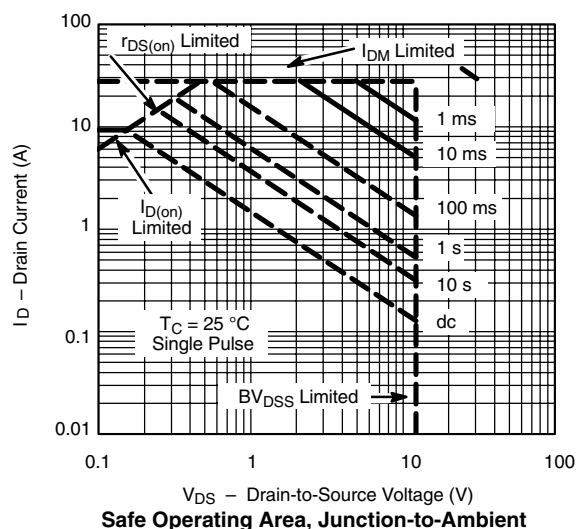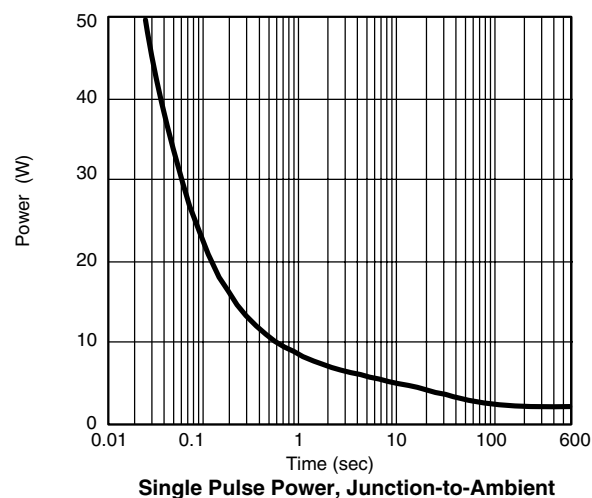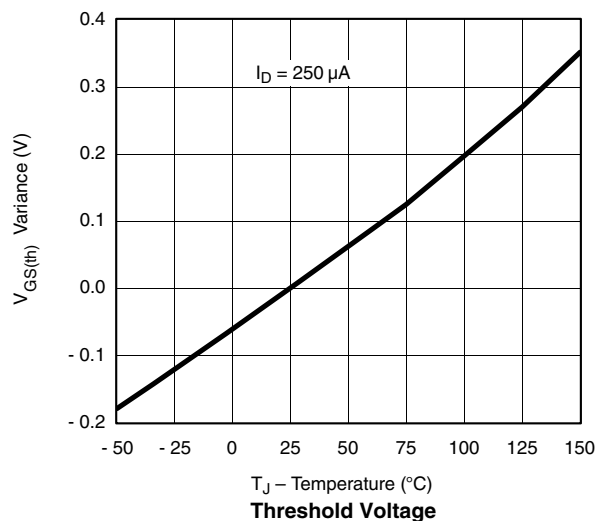**On-Resistance vs. Junction Temperature**

Source-Drain Diode Forward Voltage

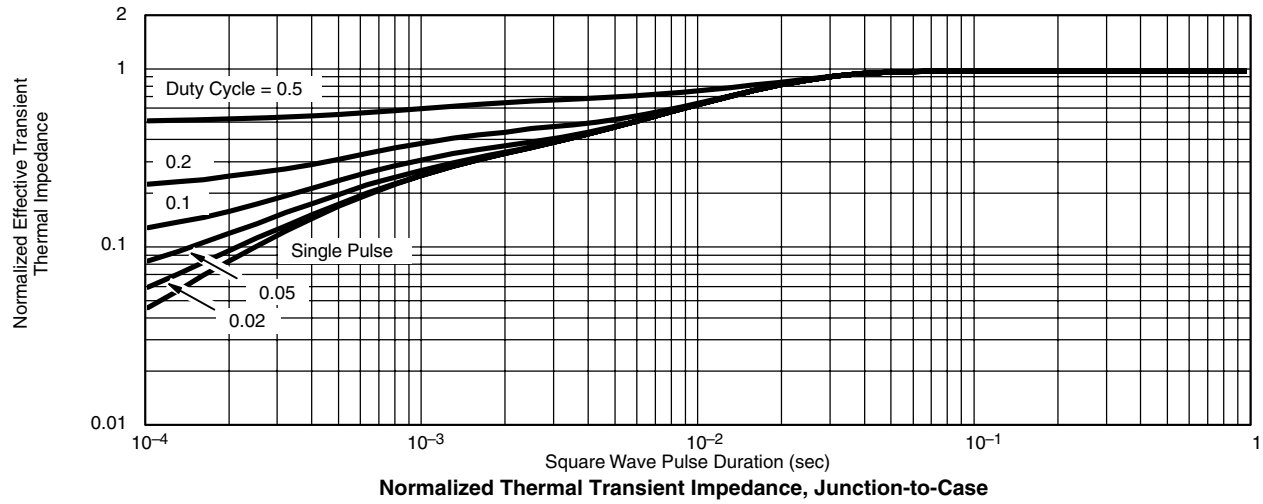**On-Resistance vs. Gate-to-Source Voltage**

TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted

I_D = 250 µA

$V_{GS(th)}$ Variance (V)

T_J – Temperature (°C)

Threshold Voltage

Power (W)

Time (sec)

Single Pulse Power, Junction-to-Ambient

$r_{DS(on)}$ Limited

I_{DM} Limited

1 ms
10 ms
100 ms
1 s
10 s
dc

$I_{D(on)}$ Limited

I_D – Drain Current (A)

T_C = 25 °C
Single Pulse

BV_{DSS} Limited

V_{DS} – Drain-to-Source Voltage (V)

Safe Operating Area, Junction-to-Ambient

Normalized Effective Transient Thermal Impedance

Duty Cycle = 0.5

0.2

0.1

0.05

0.02

Single Pulse

Square Wave Pulse Duration (sec)

Notes:

P_{DM}

t_1
t_2

1. Duty Cycle, D = $\dfrac{t_1}{t_2}$
2. Per Unit Base = R_{thJA} = 65 °C/W
3. $T_{JM} - T_A = P_{DM} Z_{thJA}^{(t)}$
4. Surface Mounted

Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted

Normalized Thermal Transient Impedance, Junction-to-Case

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