M320x Series

9x14 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML, VCXO

Product Features

- Featuring *QiK Chip™* Technology
- Superior Jitter Performance (comparable to SAW based)
- APR of ±50 or ±100ppm over industrial temperature range
- Frequencies from 150 MHz to 1.4 GHz
- Designed for a short 2 week cycle time

QiK Chip™

Product Description

The M320x series of VCXO's is designed with a hermetically sealed high precision AT cut quartz crystal, combined with our QiK Chip™ technology. This combination provides an industry setting 0.35 ps RMS jitter performance and excellent Phase Noise for your demanding circuit. The M310x is available in LVPECL, LVDS, or CML output and can be built to a variety of power requirements, 3.3, 2.5, and 1.8V. Tight thermal stability performance, broad frequency range, an industry standard 9x14mm package, and the ability to build and provide product in approximately 2 weeks, gives the designer a quick, solid foundation to build a solution with.

Product Applications

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- xDSL, Network Communications
- Avionic Flight Controls
- Military Communications
- Clock and Data Recovery
- Low Jitter Clock Generation

Product Ordering Information

Ordering Information

M320	0	6	A	G	P	J	00.0000 MHz

Product Series

Supply Voltage
0: 3.3 V **1:** 2.5 V
2: 1.8 V

Temperature Range
2: -40°C to +85°C
6: -20°C to +70°C

Absolute Pull Range (APR)
A: ±50 ppm **B:** ±100 ppm **D:** ±200 ppm

Enable/Disable
G: Complementary Enable High (Pad 2)
M: Complementary Enable Low (Pad 2)
U: Complementary Output

Logic Type
P: PECL **L:** LVDS
M: CML

Package/Lead Configuration
J: 9x14 mm J-lead

Frequency (customer specified)

M3200Sxxx, M3201Sxxx & M3202Sxxx - Contact factory for datasheets.

Revision: 11-5-10

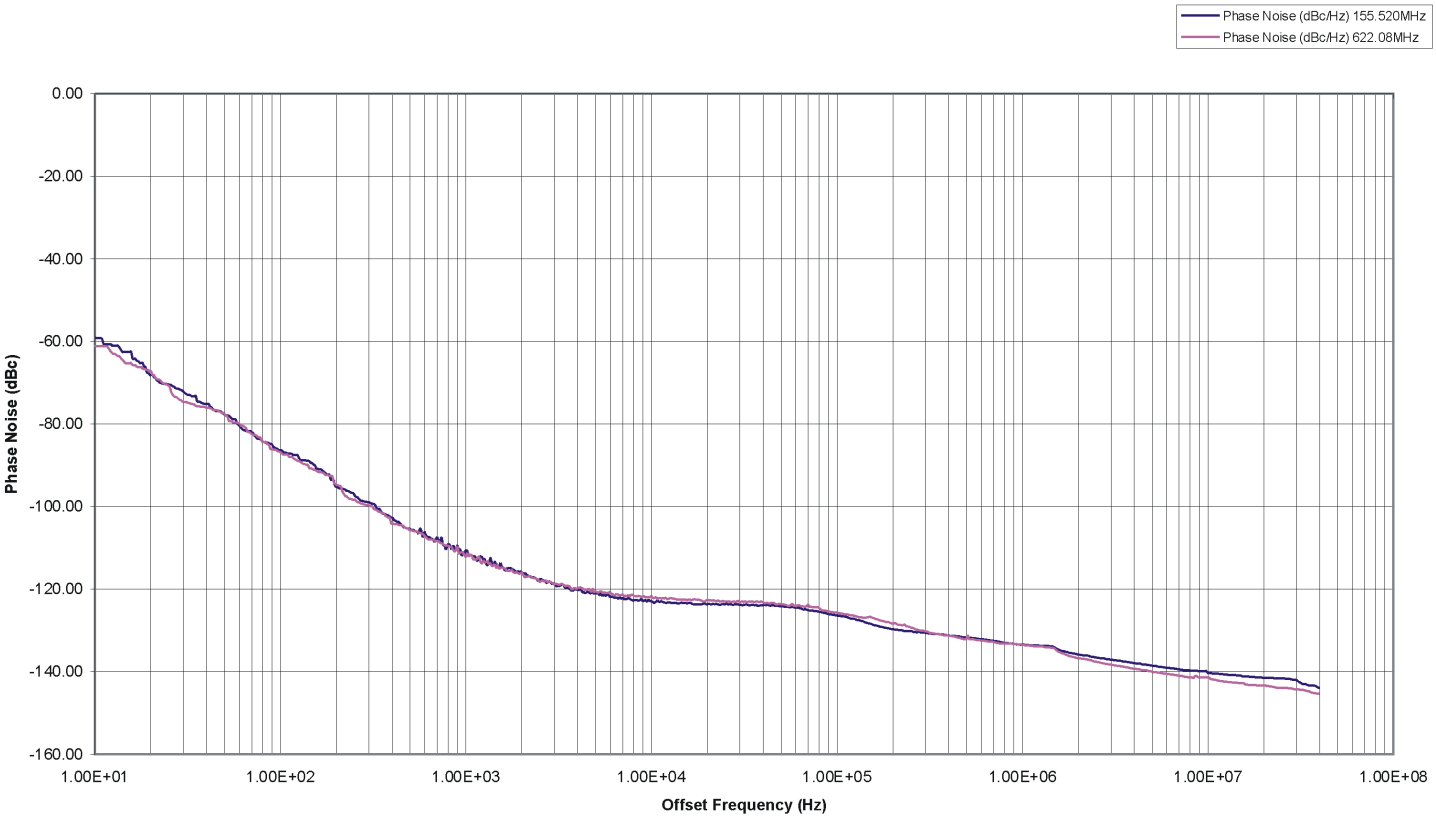
Performance Characteristics

	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Electrical Specifications	**Frequency Range**	F	50		1400	MHz	See Note 1
	Operating Temperature	TA	(See ordering information)				
	Storage Temperature	Ts	-55		+125	°C	
	Frequency Stability	ΔF/F		±25		ppm	
	Aging **1st Year** **Thereafter (per year)**		 -3 -1		 +3 +1	 ppm ppm	
	Pullability/APR		(See ordering information)				See Note 2
	Gain Transfer Function			90 135 180		ppm/V ppm/V ppm/V	For ±50 ppm APR For ±100 ppm APR For ±200 ppm APR
	Control Voltage	Vc	0.18 0.25 0.30	0.90 1.25 1.65	1.62 2.25 3.0	V V V	@ 1.8V Vcc @ 2.5V Vcc @ 3.3V Vcc
	Linearity			1	5	%	Positive Monotonic
	Modulation Bandwidth	fm	10			KHz	-3 dB bandwidth
	Input Impedance	Zin	500k	1M		Ohms	@ DC
	Supply Voltage	Vcc	1.71 2.375 3.135	1.8 2.5 3.3	1.89 2.625 3.465	V V V	LVDS/CML
	Input Current	Icc			125	mA	LVPECL/LVDS/CML
	Load		50 Ohms to (Vcc –2) Vdc 100 Ohm differential load				See Note 3 LVPECL Waveform LVDS/CML Waveform
	Symmetry (Duty Cycle)		45		55	%	LVPECL: Vdd-1.3 V LVDS: 1.25 V
	Output Skew			20 15 20		ps ps ps	LVPECL CML LVDS
	Differential Voltage	Vod	250	350	450	mV	LVDS
		Vod	0.7	0.95	1.20	Vpp	CML
	Common Mode Output Voltage	Vcm		1.2		V	LVDS
	Logic "1" Level	Voh	Vcc - 1.02			V	LVPECL
	Logic "0" Level	Vol			Vcc -1.63	V	LVPECL
	Rise/Fall Time	Tr/Tf		0.23	0.35	ns	@ 20/80% LVPECL, LVDS, CML
	Enable Function		80% Vcc min or N/C: Output active 0.5V max: Output disables to high-Z				Output Option G
			0.5V max or N/C: Output active 80% Vcc min: Output disables to high-Z				Output Option M
	Start up Time				10	ms	
	Phase Jitter @ 622.08 MHz	ϕJ		0.25		ps RMS	Integrated 12 kHz – 20 MHz

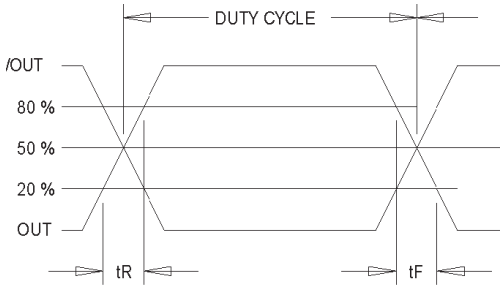
Environmental		
	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C
	Vibration	Per MIL-STD-202, Method 201 & 204
	Max Soldering Conditions	See solder profile, Figure 1
	Hermeticity	Per MIL-STD-202, Method 112 (1 x 10^{-8} atm cc/s of helium)
	Solderability	Per MIL-STD-883, Method 203

Note 1: Contact factory for standard frequency availability over 945 MHz.
Note 2: APR specification is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.
Note 3: See Load Circuit Diagram in this Datasheet. Consult factory with nonstandard output load requirements.

Phase Noise Plot



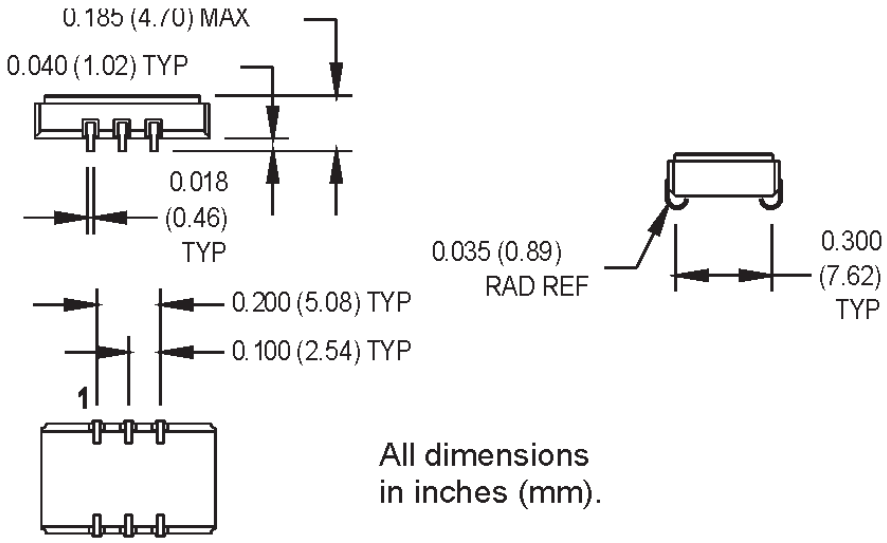
Output Waveform

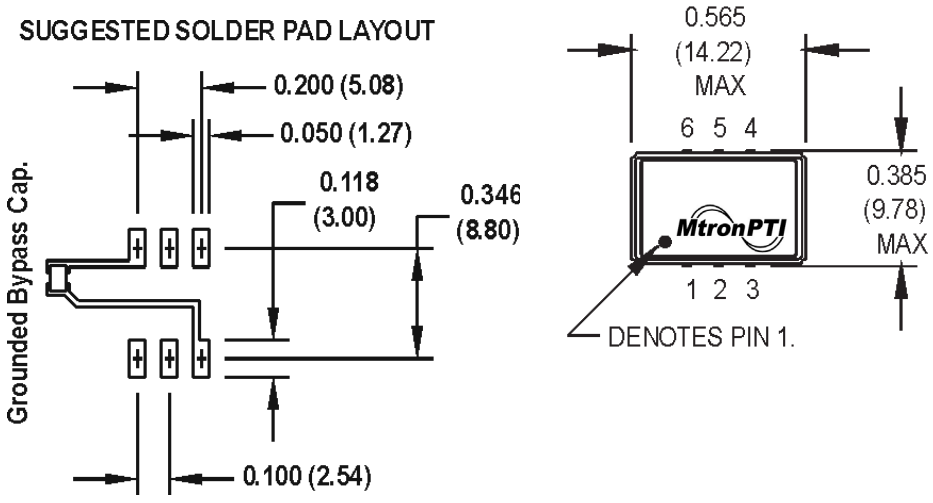


Output Waveform: LVDS/CML/PECL

Product Dimension & Pinout Information

Pin1: Voltage Control
Pin2: Enable/Disable (or N/C)
Pin3: Ground
Pin4: Output Q (PECL,LVDS,CML)
Pin5: Output $\overline{Q}$ (PECL,LVDS,CML)
Pin6: Vcc





Handling Information

Although protection circuitry has been designed into the M320x oscillator, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. MtronPTI utilizes a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained using these circuit parameters.

Model	ESD Threshold, Minimum	Unit
Human Body	1500*	V
Charged Device	1500*	V

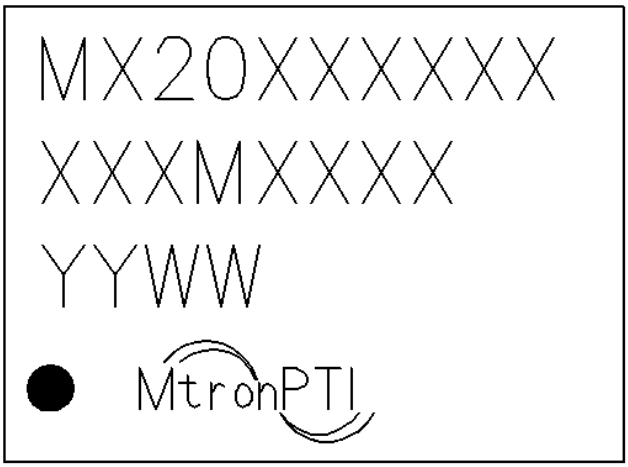
* MIL-STD-833D, Method 3015, Class 1

Quality Parameters

Environmental Specifications/Qualification Testing Performed on the M320 VCXO		
Test	**Test Method**	**Test Condition**
Electrical Characteristics	Internal Specification	Per Specification
Frequency vs. Temperature	Internal Specification	Per Specification
Mechanical Shock	MIL-STD-202, Method 213, C	100 g's
Vibration	MIL-STD-202, Method 201-204	10 g's from 10-2000 Hz
Thermal Cycle	MIL-STD-883, Method 1010, B	-55 Deg. C to +125 Deg. C, 15 minute Dwell, 10 cycles
Aging	Internal Specification	168 Hours at 105 Degrees C
Gross Leak	MIL-STD-202, Method 112	30 Second Immersion
Fine Leak	MIL-STD-202, Method 112	Must meet $1x10^{-8}$
Solderability	MIL-STD-883, Method 2003	8 Hour Steam Age – Must Exhibit 95% coverage
Resistance to Solvents	MIL-STD-883, Method 2015	Three 1 minute soaks
Terminal Pull	MIL-STD-883, Method 2004, A	2 Pounds
Lead Bend	MIL-STD-883, Method 2004, B1	1 Bending Cycle
Physical Dimensions	MIL-STD-883, Method 2016	Per Specification
Internal Visual	Internal Specification	Per Internal Specification

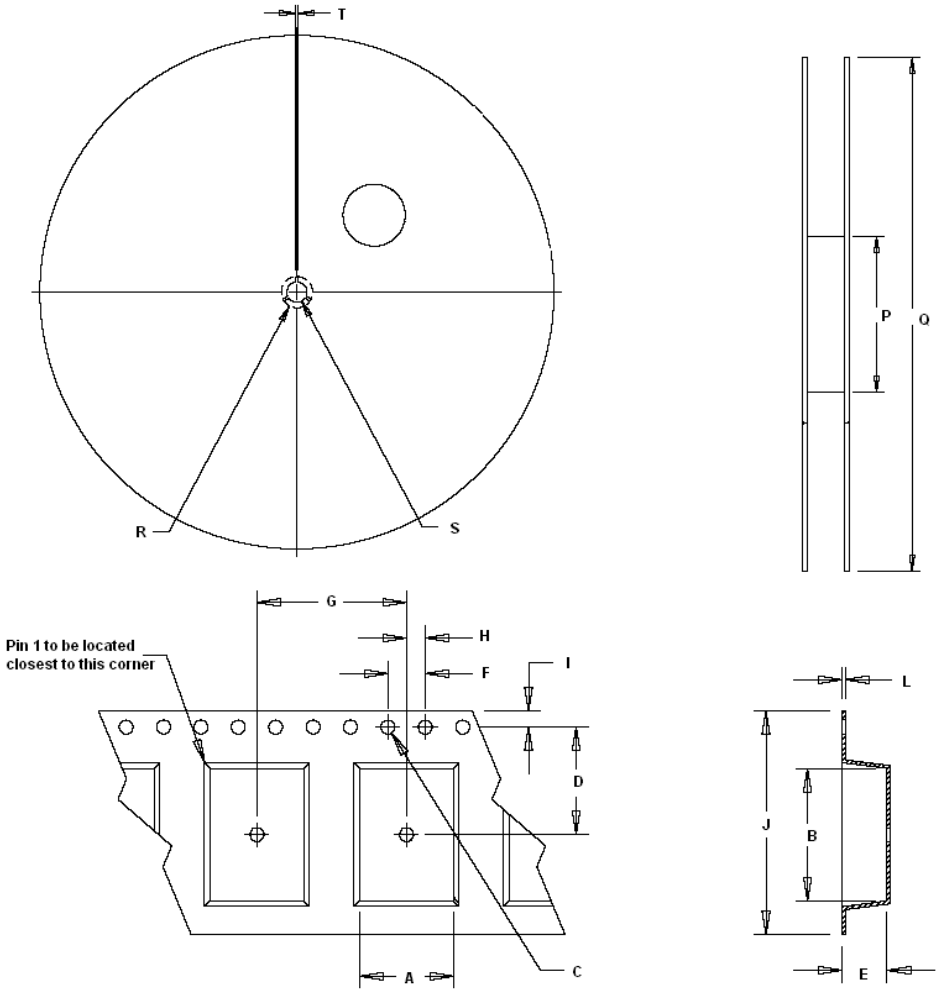
Part Marking Guide

Line 1: Model Number
Line 2: Frequency
Line 3: Date Code
Line 4: Pin 1 Indicator / MtronPTI



Tape & Reel Specifications

(all measurements are in mm)	A	B	C	D	E	F	G	H	I	J	L	P	Q	R	S	T
M320x	10.00	14.20	1.50	11.50	4.85	4.00	16.00	2.00	1.75	24.00	0.35	100.00	330.00	20.20	13.00	2.00

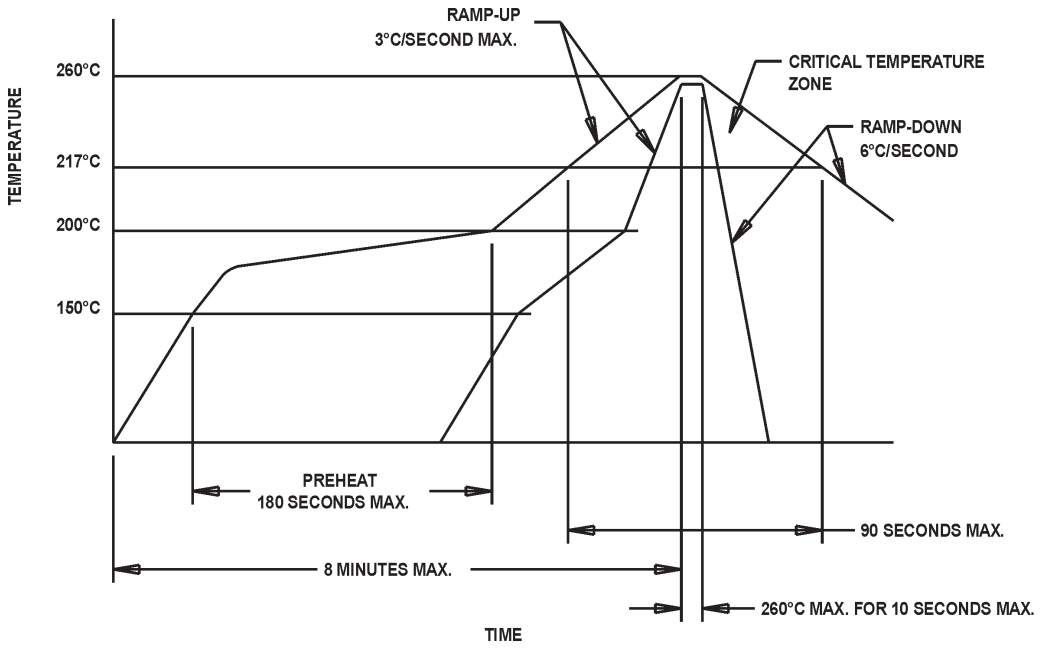


Standard Tape and Reel: 500 parts per reel

Product Revision Table

Date	Revision	PCN Number	Details of Revision
7/20/07	A	10118	IC Revision to improve phase noise and electrical performance

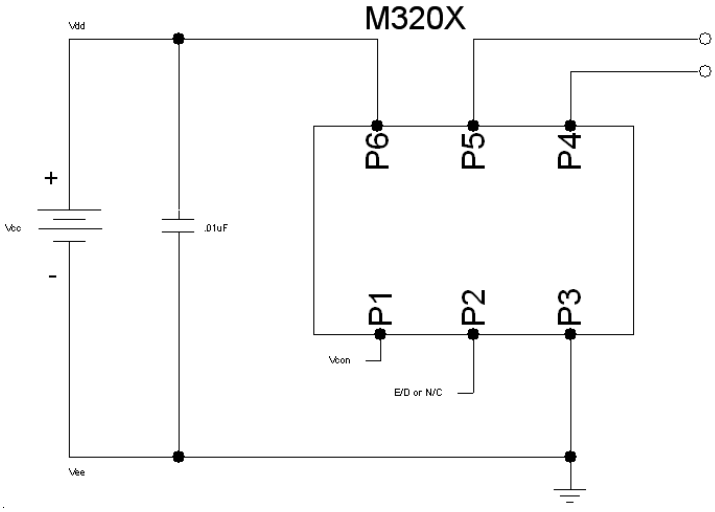
Maximum Soldering Conditions

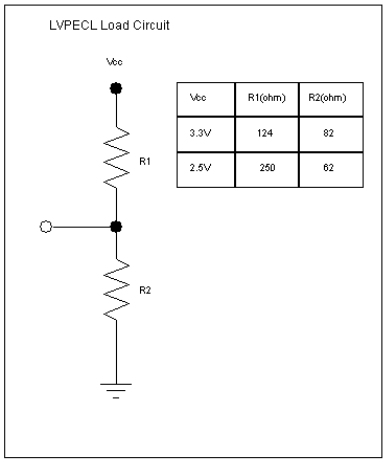


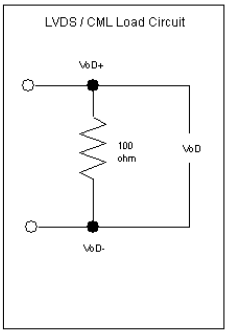
Solder Conditions

Note: Exceeding these limits may damage the device.

Typical Test Circuit & Load Circuit Diagrams







For custom products or additional specifications contact our sales team at
800.762.8800 (toll free) or 605.665.9321

For more information on this product visit the MtronPTI website at
www.mtronpti.com