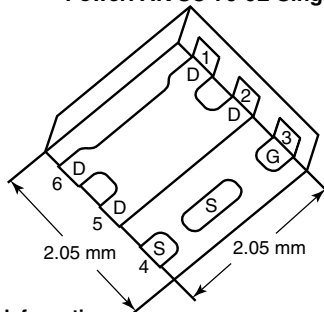




P-Channel 8 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) (Max.)	I _D (A)	Q _g (Typ.)
- 8	0.016 at V _{GS} = - 4.5 V	- 12 ^a	30 nC
	0.0215 at V _{GS} = - 2.5 V	- 12 ^a	
	0.026 at V _{GS} = - 1.8 V	- 12 ^a	
	0.032 at V _{GS} = - 1.5 V	- 12 ^a	
	0.095 at V _{GS} = - 1.2 V	- 3	

PowerPAK SC-70-6L-Single



Ordering Information:

SiA427ADJ-T4-GE3 (Lead (Pb)-free and Halogen-free)

SiA427ADJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

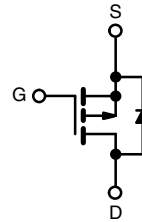
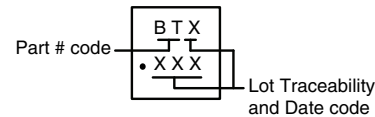
- TrenchFET[®] Power MOSFET
- Thermally Enhanced PowerPAK[®] SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_g Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Load Switch, for 1.2 V Power Line for Portable and Handheld Devices

Marking Code



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 8	V
Gate-Source Voltage	V _{GS}	± 5	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C - 12 ^a	A
		T _C = 70 °C - 12 ^a	
		T _A = 25 °C - 12 ^{a, b, c}	
		T _A = 70 °C - 9.9 ^{b, c}	
Pulsed Drain Current (t = 300 μs)	I _{DM}	- 50	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C - 12 ^a	
		T _A = 25 °C - 2.9 ^{b, c}	
Maximum Power Dissipation	P _D	T _C = 25 °C 19	W
		T _C = 70 °C 12	
		T _A = 25 °C 3.5 ^{b, c}	
		T _A = 70 °C 2.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	28	36	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	5.3	6.5	

Notes:

- Package limited
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80 °C/W.

SiA427ADJ

Vishay Siliconix



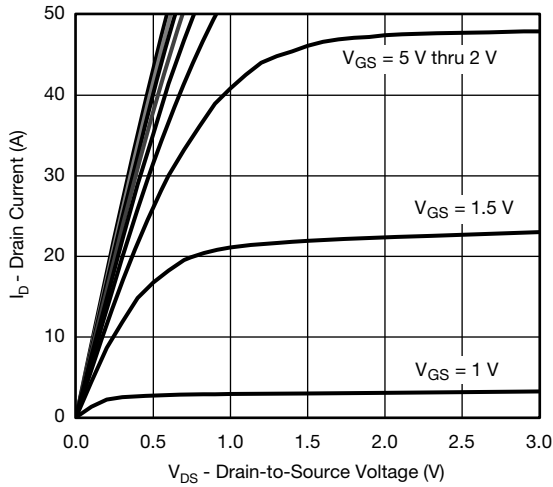
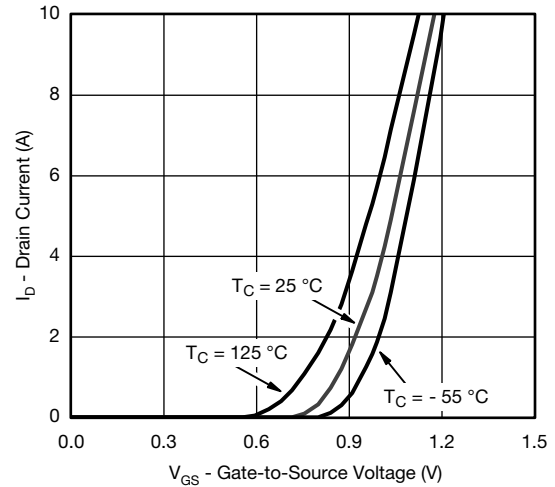
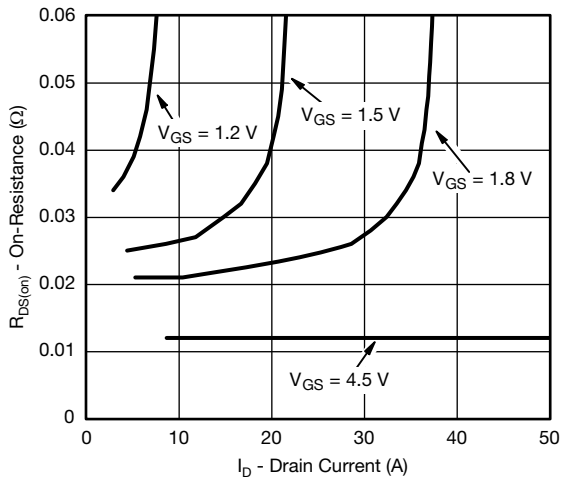
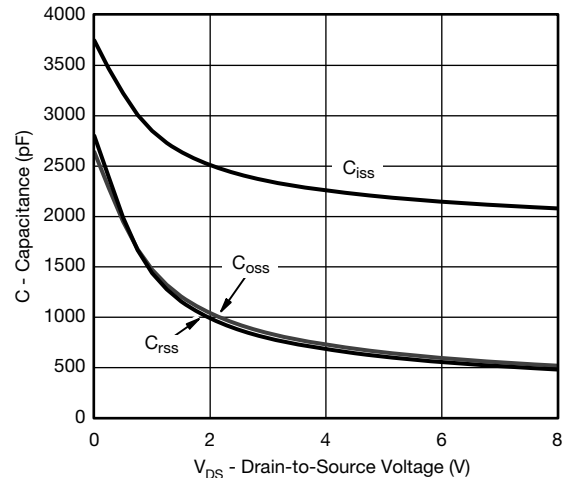
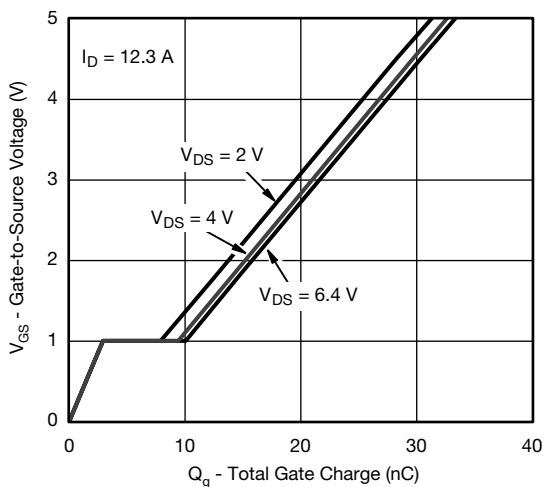
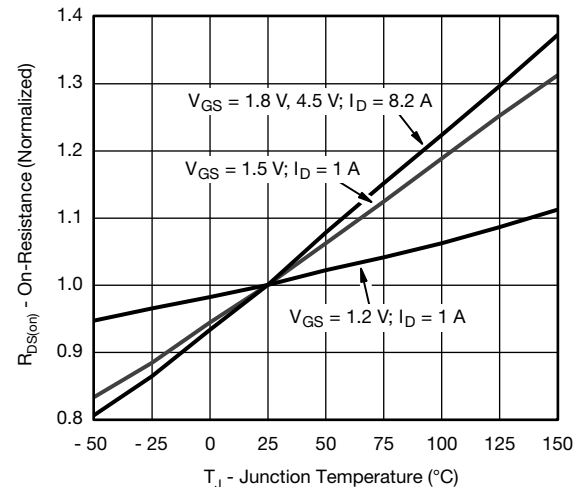
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0, I_D = -250\text{ }\mu\text{A}$	- 8			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 5.8		mV/ $^{\circ}\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 0.35		- 0.8	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -8\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -8\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^{\circ}\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	- 10			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -8.2\text{ A}$		0.013	0.016	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -7.2\text{ A}$		0.018	0.0215	
		$V_{GS} = -1.8\text{ V}, I_D = -6.6\text{ A}$		0.021	0.026	
		$V_{GS} = -1.5\text{ V}, I_D = -1\text{ A}$		0.025	0.032	
		$V_{GS} = -1.2\text{ V}, I_D = -1\text{ A}$		0.037	0.095	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -4\text{ V}, I_D = -8.2\text{ A}$		37		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -4\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2300		pF
Output Capacitance	C_{oss}			735		
Reverse Transfer Capacitance	C_{rss}			690		
Total Gate Charge	Q_g	$V_{DS} = -4\text{ V}, V_{GS} = -5\text{ V}, I_D = -10\text{ A}$		33	50	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = -4\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		30	45	
Gate-Drain Charge	Q_{gd}			3		
Gate Resistance	R_g			6.6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -4\text{ V}, R_L = 0.4\text{ }\Omega$ $I_D \cong -9.8\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$	2	9	18	Ω
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			70	105	
				40	60	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			- 12	A
Pulse Diode Forward Current	I_{SM}				- 50	
Body Diode Voltage	V_{SD}	$I_S = -9.8\text{ A}, V_{GS} = 0$		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -9.8\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^{\circ}\text{C}$		40	80	ns
Body Diode Reverse Recovery Charge	Q_{rr}			12	25	nC
Reverse Recovery Fall Time	t_a			14		ns
Reverse Recovery Rise Time	t_b			26		

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

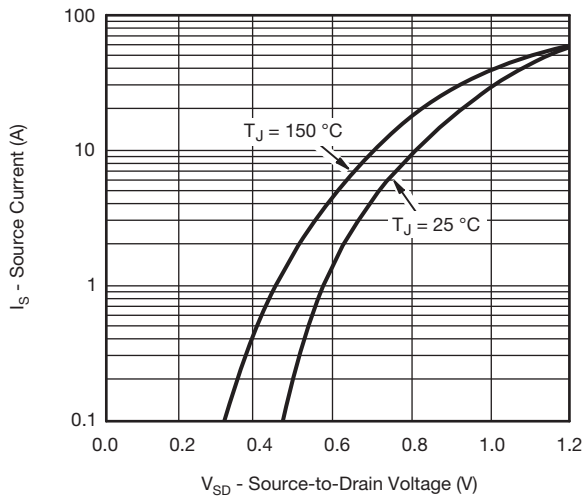
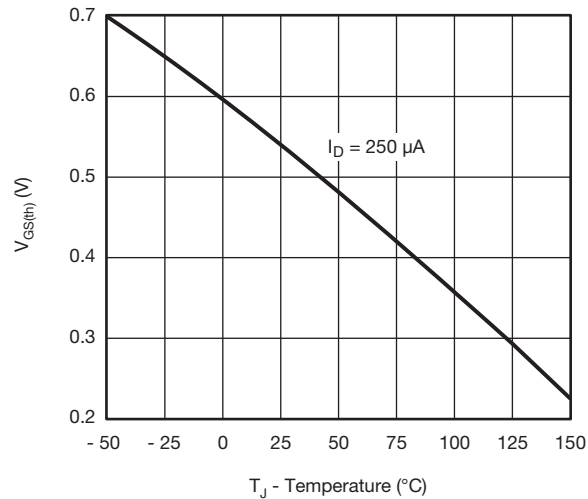
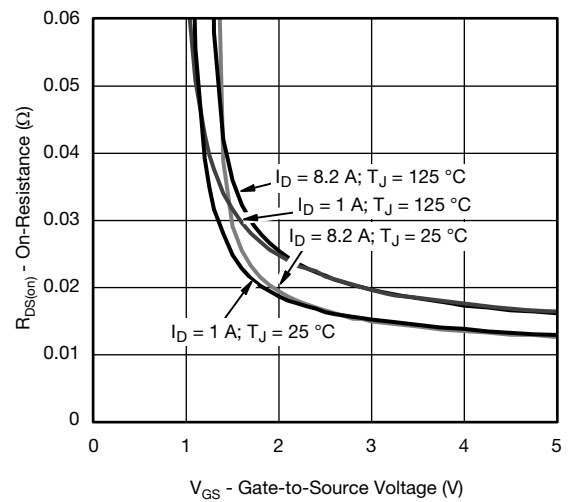
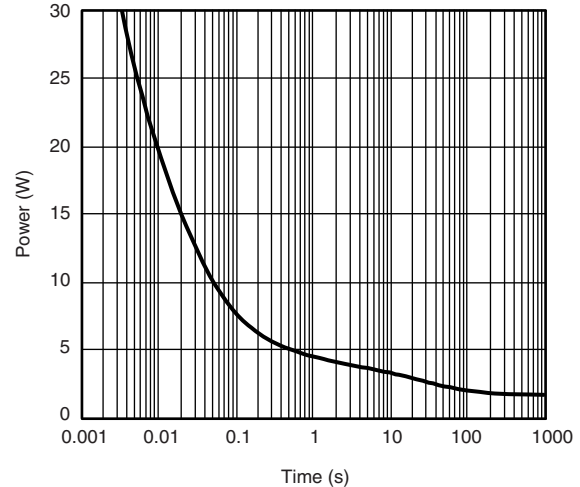
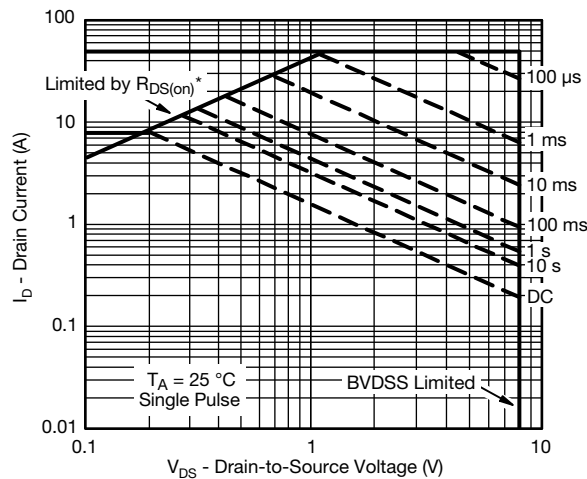
b. Guaranteed by design, not subject to production testing.

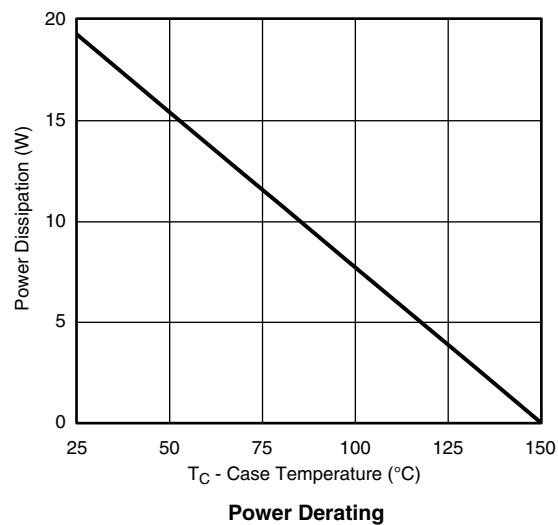
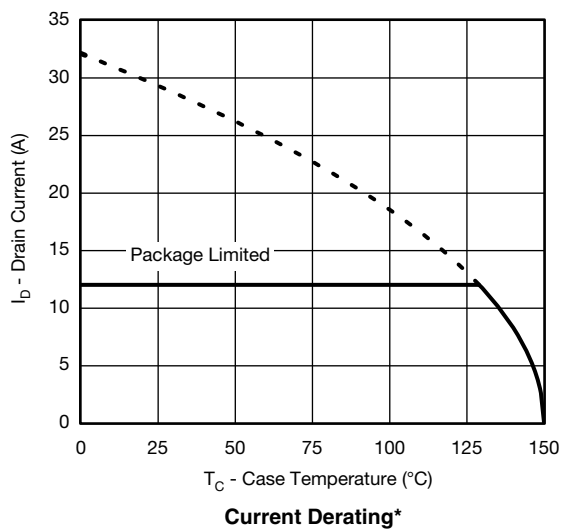
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

SiA427ADJ

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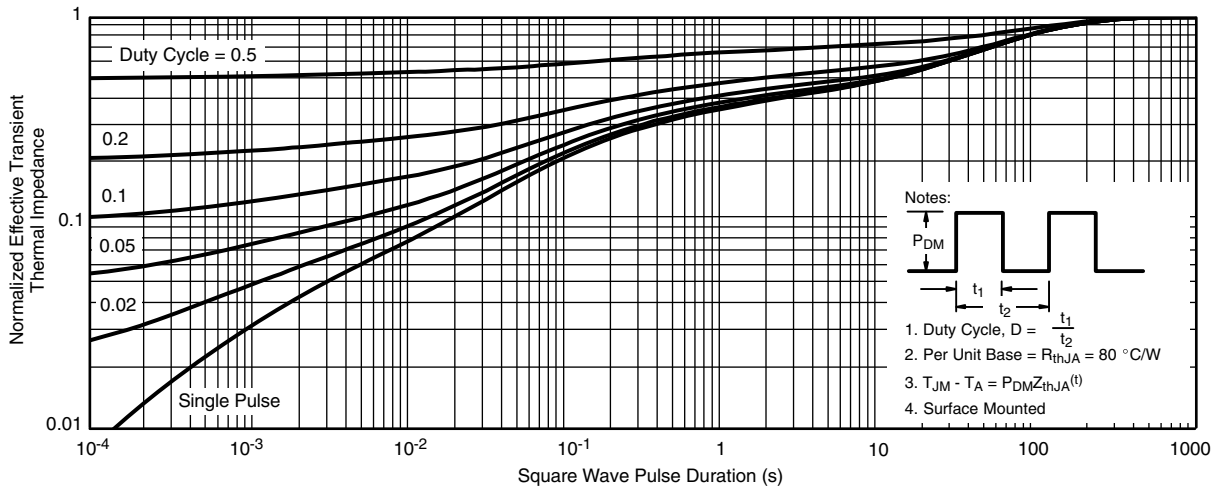
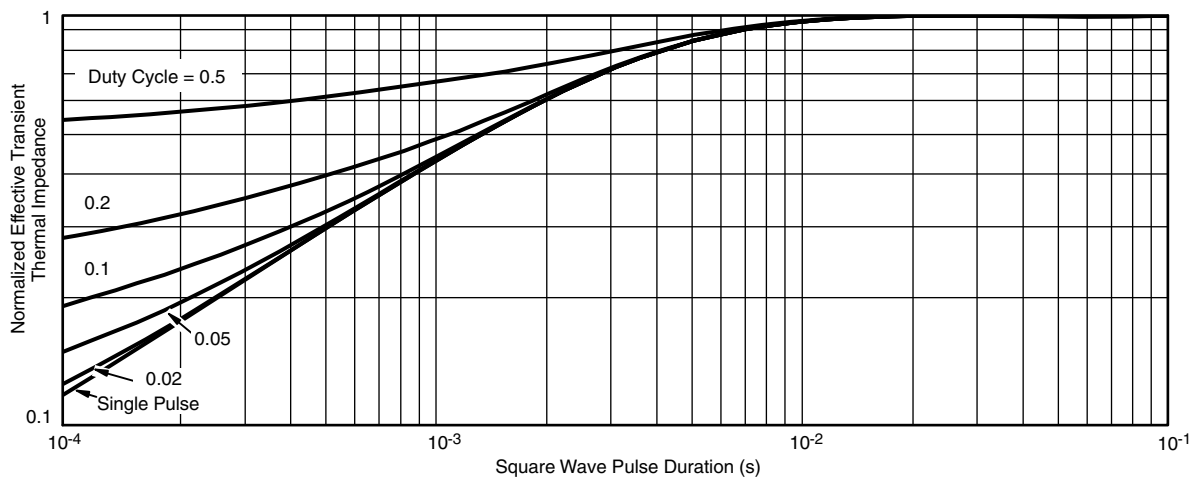
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Source-Drain Diode Forward Voltage****Threshold Voltage****On-Resistance vs. Gate-to-Source Voltage****Single Pulse Power, Junction-to-Ambient*** V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SiA427ADJ

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**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63651.



PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL



Notes:

1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 – Rev. C, 06-Aug-07
DWG: 5934

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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