FAIRCHILD SEMICONDUCTOR®

October 2013

FDMC8032L

Dual N-Channel PowerTrench® MOSFET

40 V, 7 A, 20 mΩ

Features

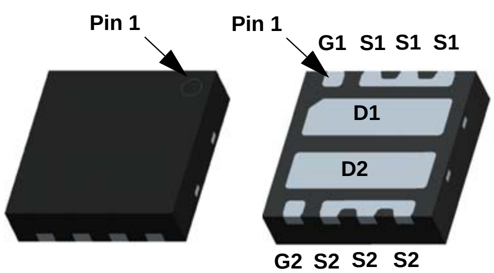
- Max $r_{DS(on)}$ = 20 mΩ at V_{GS} = 10 V, I_D = 7 A
- Max $r_{DS(on)}$ = 27 mΩ at V_{GS} = 4.5 V, I_D = 6 A
- Low Inductance Packaging Shortens Rise/Fall Times
- Lower Switching Losses
- 100% Rg Tested
- Termination is Lead-free and RoHS Compliant

General Description

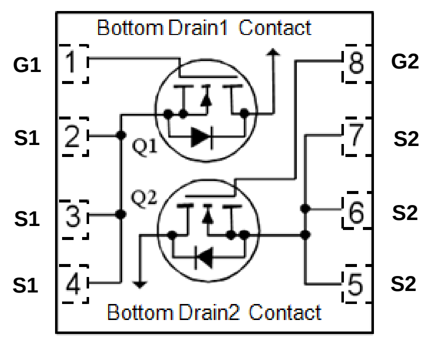
This device includes two 40V N-Channel MOSFETs in a dual Power 33 (3 mm X 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

Applications

- Battery Protection
- Load Switching
- Point of Load



Power 33



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			40	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C		20	A
	-Continuous	T_A = 25 °C	(Note 1a)	7	
	-Pulsed		(Note 4)	50	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	13	mJ
P_D	Power Dissipation	T_C = 25 °C		12	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	1.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		9.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	65	

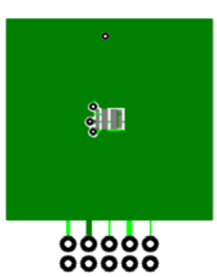
Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8032L	FDMC8032L	Power 33	13 ”	12 mm	3000 units

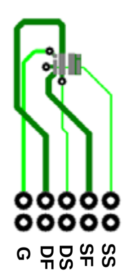
Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		23		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = ±20 V, V_{DS} = 0 V			100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250 μA	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 7 A		16	20	mΩ
		V_{GS} = 4.5 V, I_D = 6 A		21	27	
		V_{GS} = 10 V, I_D = 7 A, T_J = 125 °C		23	29	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 7 A		27		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V, f = 1MHz		513	720	pF
C_{oss}	Output Capacitance			137	195	pF
C_{rss}	Reverse Transfer Capacitance			9.3	15	pF
R_g	Gate Resistance		0.1	2.6	3.6	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20 V, I_D = 7 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		5.5	11	ns
t_r	Rise Time			1.2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			13	24	ns
t_f	Fall Time			1.3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 20 V, I_D = 7 A		7.6	11	nC
	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 20 V, I_D = 7 A		3.6	5.1	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 20 V, I_D = 7 A		1.5		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.0		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 7 A (Note 2)		0.85	1.3	V
		V_{GS} = 0 V, I_S = 1.4 A (Note 2)		0.75	1.2	
t_{rr}	Reverse Recovery Time	I_F = 7 A, di/dt = 100 A/μs		16	29	ns
Q_{rr}	Reverse Recovery Charge			3.9	10	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 65 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 155 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. E_{AS} of 13 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 3 A, V_{DD} = 40 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 11 A.
4. Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

Typical Characteristics T_J = 25 °C unless otherwise noted

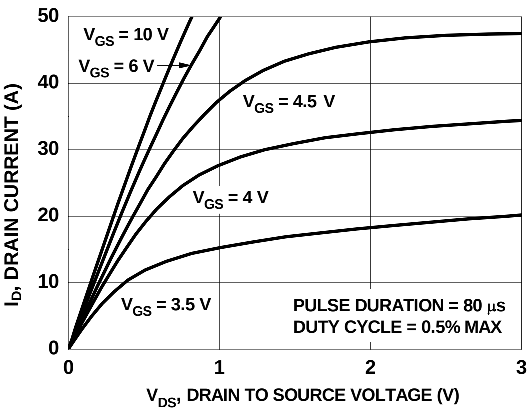


Figure 1. On-Region Characteristics

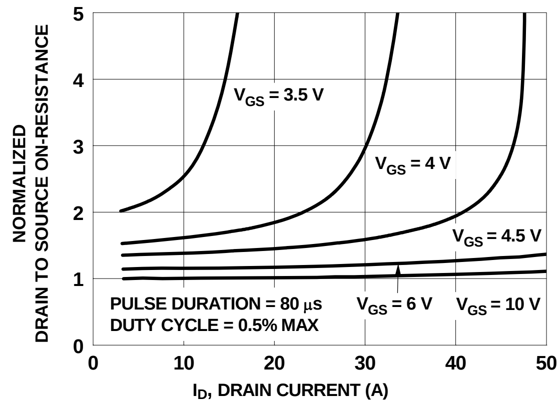


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

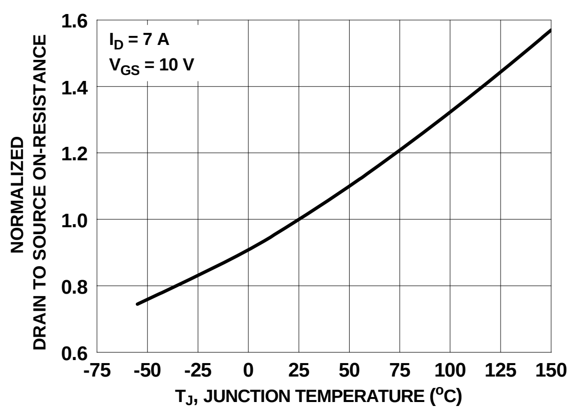


Figure 3. Normalized On-Resistance vs Junction Temperature

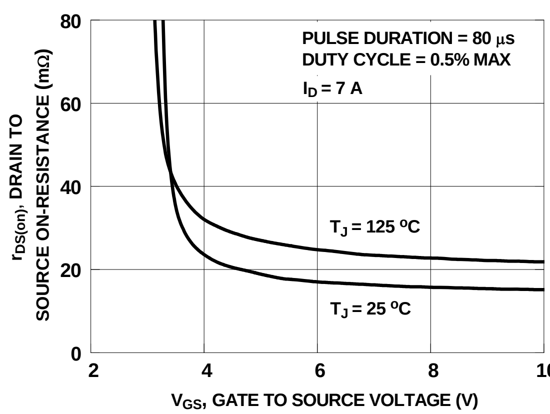


Figure 4. On-Resistance vs Gate to Source Voltage

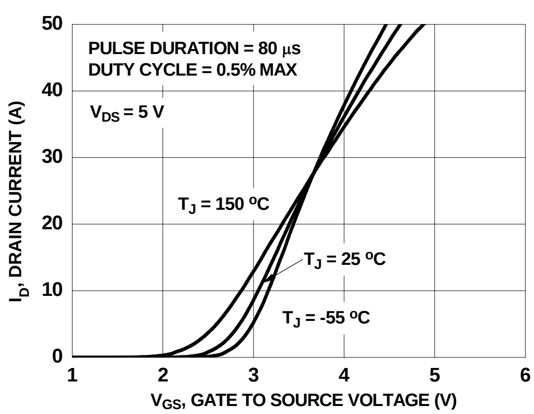


Figure 5. Transfer Characteristics

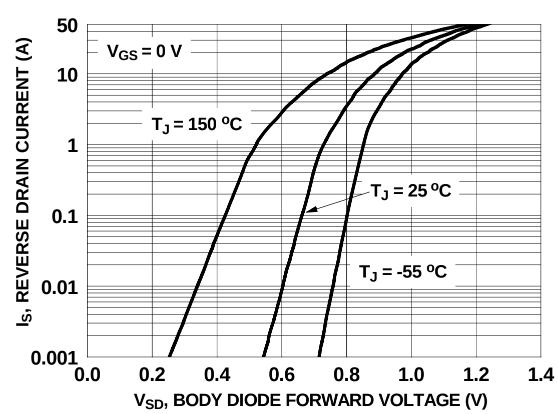


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

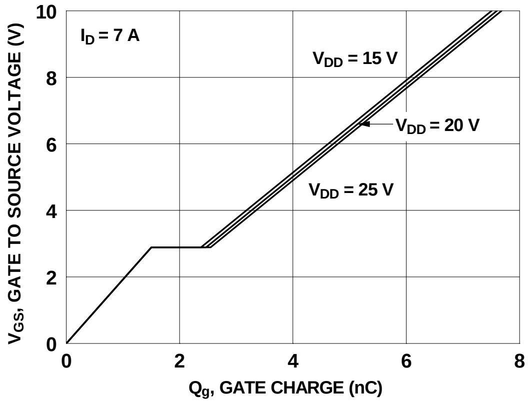


Figure 7. Gate Charge Characteristics

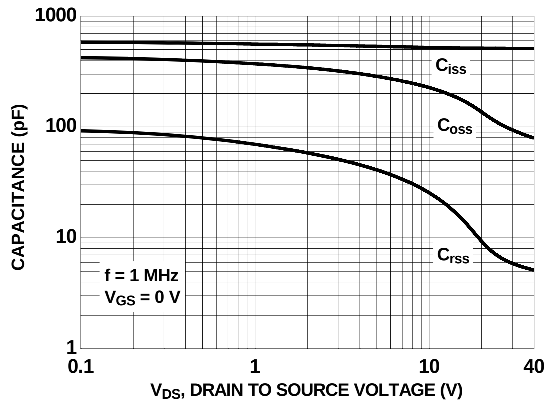


Figure 8. Capacitance vs Drain to Source Voltage

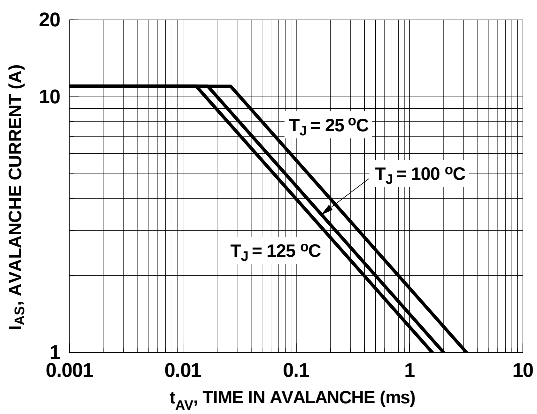


Figure 9. Unclamped Inductive Switching Capability

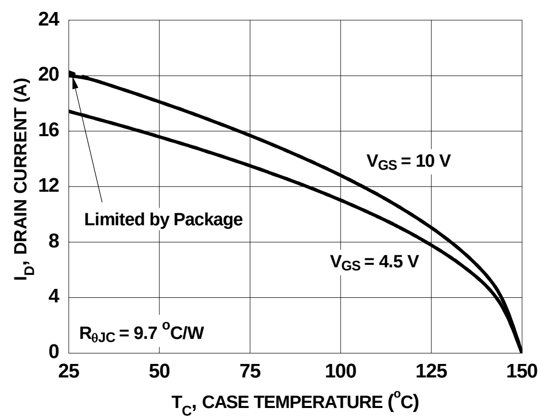


Figure 10. Maximum Continuous Drain Current vs Case Temperature

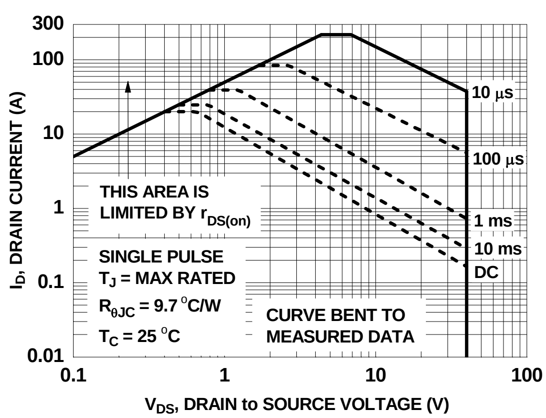


Figure 11. Forward Bias Safe Operating Area

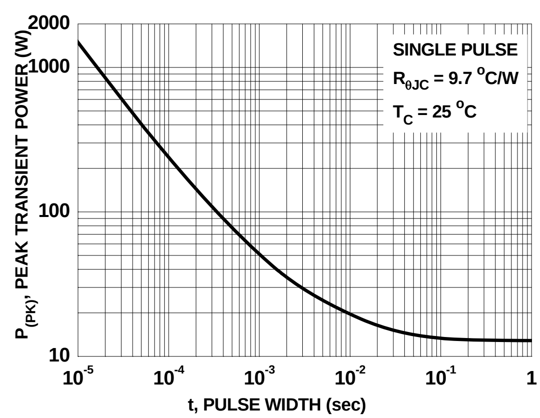


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

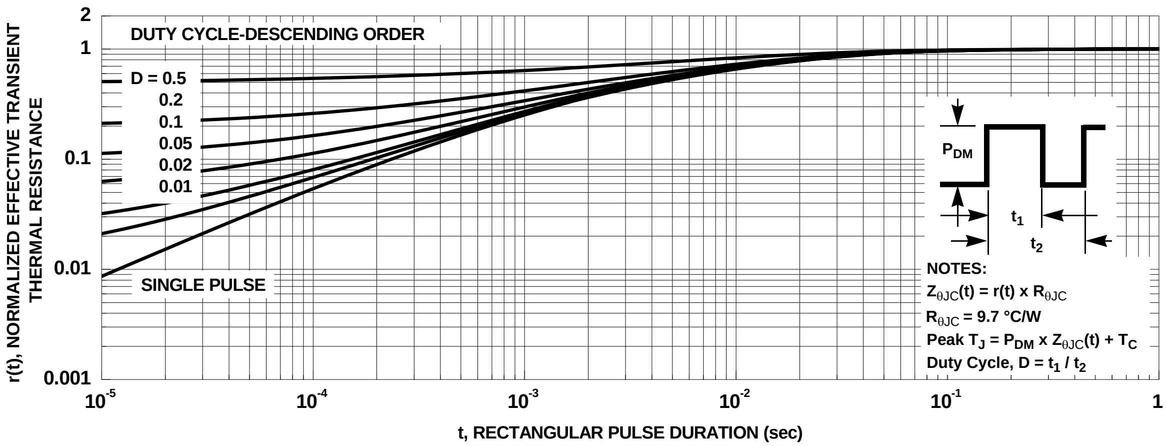
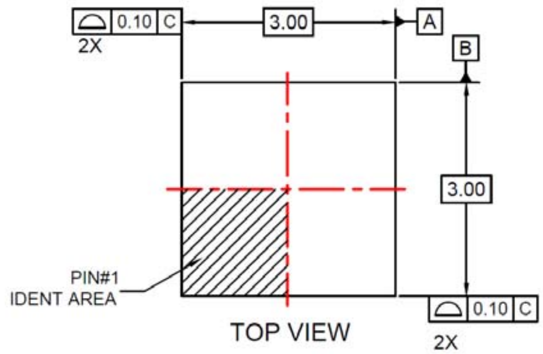
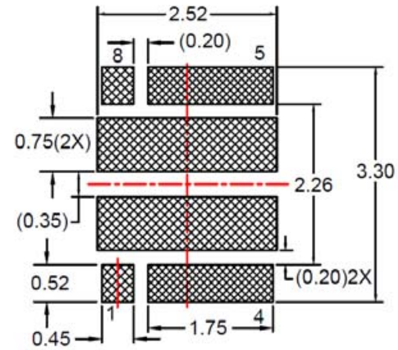


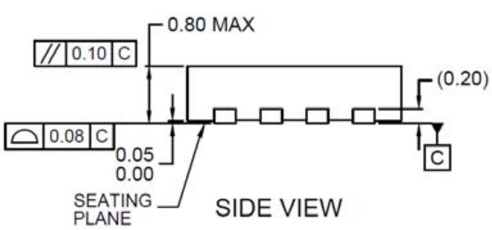
Figure 13. Transient Thermal Response Curve

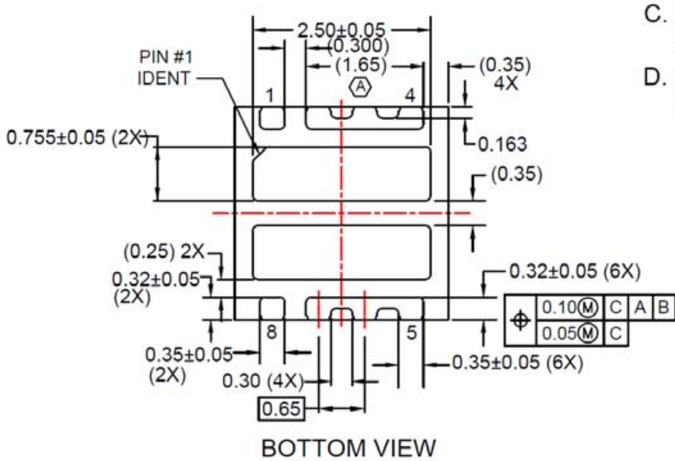
Dimensional Outline and Pad Layout





RECOMMENDED LAND PATTERN





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