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# FAN6920MR
# mWSaver™ Technology Integrated Critical-Mode PFC and Quasi-Resonant Current-Mode PWM Controller

## Features

- mWSaver™ Technology Provides Industry's Best-in-Class Standby Power
  - Internal High-Voltage JFET Startup
  - Adaptive Off-Time Modulation of $t_{OFF-MIN}$ for QR PWM Stage, Improved Light-Load Efficiency
  - PFC Burst or Shutdown at Light-Load Condition
  - Optimized for Dual Switch Flyback Design to Achieve > 90% Efficiency While Meeting 2013 ErP lot 6 Standby Power Requirement
- Integrated PFC and Flyback Controller
- Critical-Mode PFC Controller
- Zero-Current Detection for PFC Stage
- Quasi-Resonant Operation for PWM Stage
- Internal 5 ms Soft-Start for PWM
- Brownout Protection
- High / Low Line Over-Power Compensation
- Auto-Recovery Over-Current Protection
- Auto-Recovery Open-Loop Protection
- Externally Auto-Recovery Triggering (RT Pin)
- Adjustable Over-Temperature Protection
- VDD Pin and Output Voltage OVP (Auto-Recovery)
- Internal Over-Temperature Shutdown (140°C)

## Applications

- AC/DC NB Adapters
- Open-Frame SMPS
- Battery Charger

## Description

The highly integrated FAN6920MR combines Power Factor Correction (PFC) controller and quasi-resonant PWM controller. Integration provides cost-effective design and reduces external components.

For PFC, FAN6920MR uses a controlled on-time technique to provide a regulated DC output voltage and to perform natural power-factor correction. With an innovative THD optimizer, FAN6920MR can reduce input current distortion at zero-crossing duration to improve THD performance.

For PWM, FAN6920MR provides several functions to enhance the power system performance: valley detection, green-mode operation, and high / low line over-power compensation. Protection functions include secondary-side open-loop and over-current with auto-recovery protection; external auto-recovery triggering; adjustable over-temperature protection by the RT pin; and external NTC resistor, internal over-temperature shutdown, $V_{DD}$ pin OVP, and the DET pin over-voltage for output OVP, and brown-in / out for AC input voltage UVP.

The FAN6920MR controller is available in a 16-pin small-outline package (SOP).

## Related Resources

- Evaluation Board: FEBFAN6920MR_T02U120A

## Ordering Information

| Part Number | OLP Mode | Operating Temperature Range | Package | Packing Method |
|---|---|---|---|---|
| FAN6920MRMY | Recovery | -40°C to +105°C | 16-Pin Small Outline Package (SOP) | Tape & Reel |

## Application Diagram

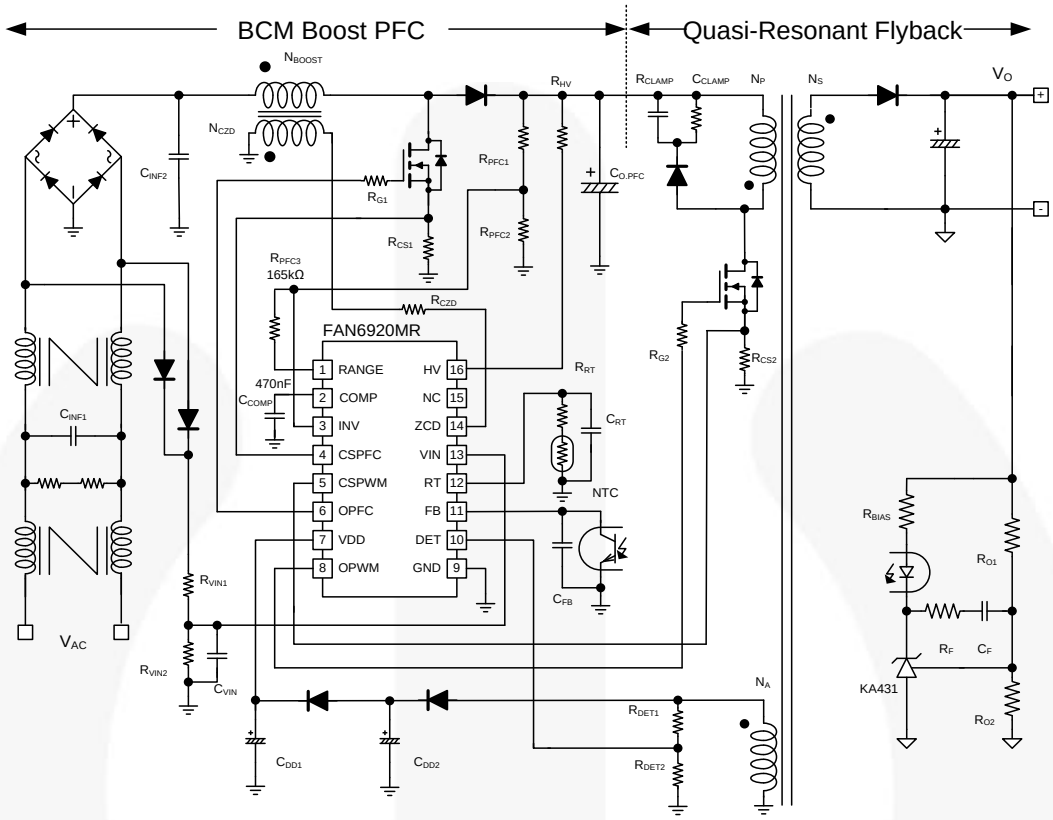



**Figure 1. Typical Application Circuit**

## Internal Block Diagram

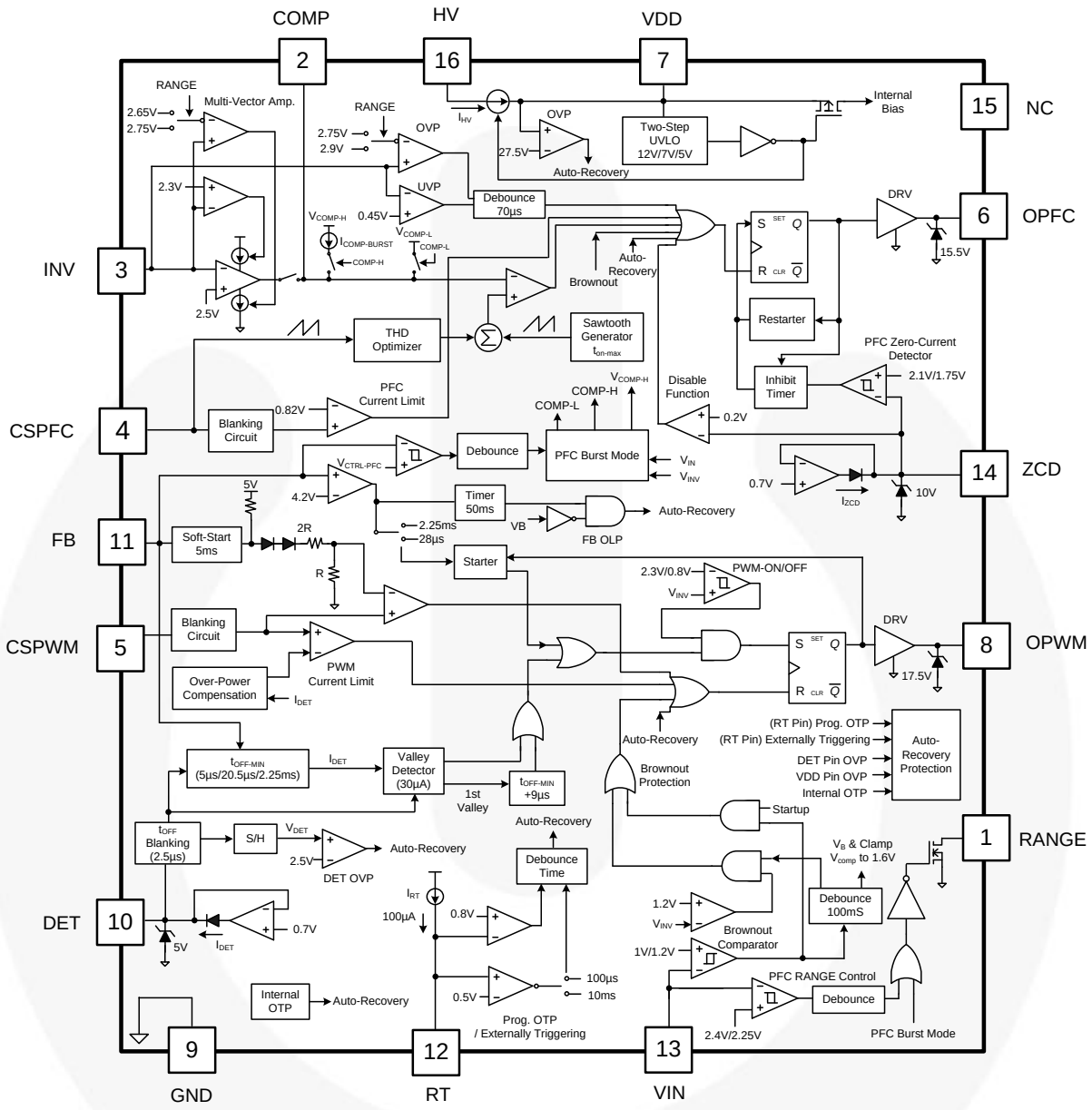
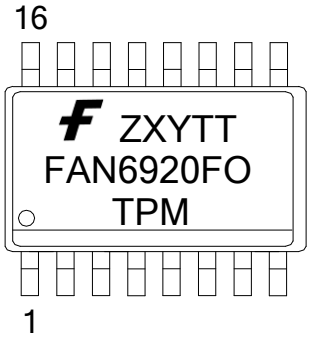



**Figure 2. Functional Block Diagram**

## Marking Information




- Fairchild Logo
Z - Plant Code
X - Year Code
Y - Week Code
TT - Die Run Code
F - Frequency (M = Low, H = High Level)
O - OLP Mode (L = Latch, R = Recovery)
T - Package Type (M = SOP)
P - Y = Green Compound
M - Manufacturing Flow Code

**Figure 3. Marking Diagram**

## Pin Configuration

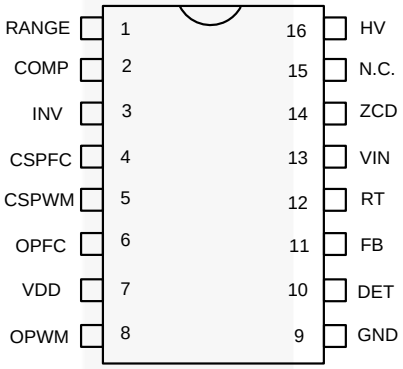



**Figure 4. Pin Configuration**

## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| 1 | RANGE | The RANGE pin's impedance changes according to VIN pin voltage level. When the input voltage detected by the VIN pin is higher than a threshold voltage, it sets to low impedance; whereas it sets to high impedance if input voltage is at a high level. |
| 2 | COMP | Output pin of the error amplifier. It is a transconductance-type error amplifier for PFC output voltage feedback. Proprietary multi-vector current is built-in to this amplifier; therefore, the compensation for PFC voltage feedback loop allows a simple compensation circuit between this pin and GND. |
| 3 | INV | Inverting input of the error amplifier. This pin is used to receive PFC voltage level by a voltage divider and provides PFC output over- and under-voltage protections. This pin also controls the PWM startup. Once the FAN6920MR is turned on and $V_{INV}$ exceeds in 2.3 V, PWM starts. |
| 4 | CSPFC | Input to the PFC over-current protection comparator that provides cycle-by-cycle current limiting protection. When the sensed voltage across the PFC current-sensing resistor reaches the internal threshold (0.82 V typical), the PFC switch is turned off to activate cycle-by-cycle current limiting. |
| 5 | CSPWM | Input to the comparator of the PWM over-current protection and performs PWM current-mode control with FB pin voltage. A resistor is used to sense the switching current of the PWM switch and the sensing voltage is applied to the CSPWM pin for the cycle-by-cycle current limit, current-mode control, and high / low line over-power compensation according to DET pin source current during PWM $t_{ON}$ time. |

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## Pin Definitions (Continued)

| Pin # | Name | Description |
|---|---|---|
| 6 | OPFC | Totem-pole driver output to drive the external power MOSFET. The clamped gate output voltage is 15.5 V. |
| 7 | VDD | Power supply. The threshold voltages for startup and turn-off are 12 V and 7 V, respectively. The startup current is less than 30 μA and the operating current is lower than 10 mA. |
| 8 | OPWM | Totem-pole output generates the PWM signal to drive the external power MOSFET. The clamped gate output voltage is 17.5 V. |
| 9 | GND | The power ground and signal ground. |
| 10 | DET | This pin is connected to an auxiliary winding of the PWM transformer through a resistor divider for the following purposes:<br>▪ Producing an offset voltage to compensate the threshold voltage of PWM current limit for over-power compensation. The offset is generated in accordance with the input voltage when the PWM switch is on.<br>▪ Detecting the valley voltage signal of drain voltage of the PWM switch to achieve the valley voltage switching and minimize the switching loss on the PWM switch.<br>▪ Providing output over-voltage protection. A voltage comparator is built in to the DET pin. The DET pin detects the flat voltage through a voltage divider paralleled with auxiliary winding. This flat voltage is reflected to the secondary winding during PWM inductor discharge time. If output over voltage and this flat voltage are higher than 2.5 V, the controller stops all PFC and PWM switching operation. The protection mode is auto-recovery. |
| 11 | FB | Feedback voltage pin used to receive the output voltage level signal to determine PWM gate duty for regulating output voltage. The FB pin voltage can also activate open-loop, overload protection and output-short circuit protection if the FB pin voltage is higher than a threshold of around 4.2 V for more than 50 ms. The input impedance of this pin is a 5 kΩ equivalent resistance. A 1/3 attenuator is connected between the FB pin and the input of the CSPWM/FB comparator. |
| 12 | RT | Adjustable over-temperature protection and external protection triggering. A constant current flows out from the RT pin. When RT pin voltage is lower than 0.8 V (typical), protection is activated and stops PFC and PWM switching operation. This protection is auto-recovery. |
| 13 | VIN | Line-voltage detection for brownin / out protections. This pin can receive the AC input voltage level through a voltage divider. The voltage level of the VIN pin is not only used to control RANGE pin's status, but it can also perform brownin / out protection for AC input voltage UVP. |
| 14 | ZCD | Zero-current detection for the PFC stage. This pin is connected to an auxiliary winding coupled to PFC inductor winding to detect the ZCD voltage signal once the PFC inductor current discharges to zero. When the ZCD voltage signal is detected, the controller starts a new PFC switching cycle. When the ZCD pin voltage is pulled to under 0.2 V (typical), it disables the PFC stage and the controller stops PFC switching. This can be realized with an external circuit if disabling the PFC stage is desired. |
| 15 | NC | No connection |
| 16 | HV | High-voltage startup pin is connected to the AC line voltage through a resistor (100 kΩ typical) for providing a high charging current to $V_{DD}$ capacitor. |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | | 30 | V |
| $V_{HV}$ | HV | | 500 | V |
| $V_H$ | OPFC, OPWM | -0.3 | 25.0 | V |
| $V_L$ | INV, COMP, CSPFC, DET, FB, CSPWM, RT, VIN, RANGE | -0.3 | 7.0 | V |
| $V_{ZCD}$ | Input Voltage to ZCD Pin | -0.3 | 12.0 | V |
| $P_D$ | Power Dissipation | | 800 | mW |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Air) | | 104 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | | 41 | °C/W |
| $T_J$ | Operating Junction Temperature | -40 | +150 | °C |
| $T_{STG}$ | Storage Temperature Range | -55 | +150 | °C |
| $T_L$ | Lead Temperature (Soldering, 10 Seconds) | | +260 | °C |
| ESD | Human Body Model, JESD22-A114 (All Pins Except HV Pin)[3] | | 4500 | V |
| | Charged Device Model, JESD22-C101 (All Pins Except HV Pin)[3] | | 1250 | |

**Notes:**
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to the GND pin.
3. All pins including HV pin: CDM=750 V, HBM 1000 V.

## Electrical Characteristics

$V_{DD}$=15 V and $T_A$=25°C unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **$V_{DD}$ Section** | | | | | | |
| $V_{OP}$ | Continuously Operating Voltage | | | | 25 | V |
| $V_{DD-ON}$ | Turn-On Threshold Voltage | | 10.5 | 12.0 | 13.5 | V |
| $V_{DD-PWM-OFF}$ | PWM Off Threshold Voltage | | 6 | 7 | 8 | V |
| $V_{DD-OFF}$ | Turn-Off Threshold Voltage | | 4 | 5 | 6 | V |
| $I_{DD-ST}$ | Startup Current | $V_{DD}$=$V_{DD-ON}$ - 0.16 V, Gate Open | | 20 | 30 | µA |
| $I_{DD-OP}$ | Operating Current | $V_{DD}$=15 V, OPFC, OPWM=100 kHz, $C_{L-PFC}$, $C_{L-PWM}$=2 nF | | | 10 | mA |
| $I_{DD-GREEN}$ | Green-Mode Operating Supply Current (Average) | $V_{DD}$=15 V, OPWM=450 Hz, $C_{L-PWM}$=2 nF | | 5.5 | | mA |
| $I_{DD-PWM-OFF}$ | Operating Current at PWM-Off Phase | $V_{DD}$=$V_{DD-PWM-OFF}$ - 0.5 V | 70 | 120 | 170 | µA |
| $V_{DD-OVP}$ | $V_{DD}$ Over-Voltage Protection (Auto-Recovery) | | 26.5 | 27.5 | 28.5 | V |
| $t_{VDD-OVP}$ | $V_{DD}$ OVP Debounce Time | | 100 | 150 | 200 | µs |
| **HV Startup Current Source Section** | | | | | | |
| $I_{HV}$ | Supply Current Drawn from HV Pin | $V_{AC}$=90 V, ($V_{DC}$=120 V), $V_{DD}$=0 V | 1.3 | | | mA |
| | | HV=500 V, $V_{DD}$=$V_{DD-OFF}$ +1 V | | 1.0 | | µA |
| **VIN and RANGE Section** | | | | | | |
| $V_{VIN-UVP}$ | Threshold Voltage for AC Input Under-Voltage Protection | | 0.95 | 1.00 | 1.05 | V |
| $V_{VIN-RE-UVP}$ | Under-Voltage Protection Reset Voltage | | $V_{VIN-UVP}$ +0.15 V | $V_{VIN-UVP}$ +0.20 V | $V_{VIN-UVP}$ +0.25 V | V |
| $t_{VIN-UVP}$ | Under-Voltage Protection Debounce Time | | 70 | 100 | 130 | ms |
| $V_{VIN-RANGE-H}$ | High $V_{VIN}$ Threshold for RANGE Comparator | | 2.40 | 2.45 | 2.50 | V |
| $V_{VIN-RANGE-L}$ | Low $V_{VIN}$ Threshold for RANGE Comparator | | 2.20 | 2.25 | 2.30 | V |
| $t_{RANGE}$ | Range-Enable / Disable Debounce Time | | 60 | 90 | 120 | ms |
| $V_{RANGE-OL}$ | Output Low Voltage of RANGE Pin | $I_O$=1 mA | | | 0.5 | V |
| $I_{RANGE-OH}$ | Output High Leakage Current of RANGE Pin | RANGE=5 V | | | 50 | nA |
| $t_{ON-MAX-PFC}$ | PFC Maximum On Time | $R_{MOT}$=24 kΩ | 22 | 25 | 28 | µs |

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## Electrical Characteristics (Continued)

$V_{DD}$=15V and $T_A$=25°C unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **PFC STAGE** | | | | | | |
| **Voltage Error Amplifier Section** | | | | | | |
| Gm | Transconductance[4] | | 100 | 125 | 150 | µmho |
| $V_{REF}$ | Feedback Comparator Reference Voltage | | 2.465 | 2.500 | 2.535 | V |
| $V_{INV-H}$ | Clamp High Feedback Voltage | RANGE=Open | 2.70 | 2.75 | 2.80 | V |
| | | RANGE=Ground | 2.60 | 2.65 | 2.70 | |
| $V_{RATIO}$ | Clamp High Output Voltage Ratio[4] | $V_{INV-H}$ / $V_{REF}$, RANGE=Open | 1.06 | | 1.14 | V/V |
| | | $V_{INV-H}$ / $V_{REF}$, RANGE=Ground | 1.04 | | 1.08 | |
| $V_{INV-L}$ | Clamp Low Feedback Voltage | | 2.25 | 2.35 | 2.45 | V |
| $V_{INV-OVP}$ | Over-Voltage Protection for INV Input | RANGE=Open | | 2.90 | 2.95 | V |
| | | RANGE=Ground | | 2.75 | 2.80 | |
| $t_{INV-OVP}$ | Over-Voltage Protection Debounce Time | | 50 | 70 | 90 | µs |
| $V_{INV-UVP}$ | Under-Voltage Protection for INV Input | | 0.35 | 0.45 | 0.55 | V |
| $V_{INV-PWMON}$ | PWM ON Threshold Voltage on INV Pin | | 2.2 | 2.3 | 2.4 | V |
| $V_{HYST-PWMON}$ | Hysteresis for PWM ON Threshold Voltage on INV Pin | | $V_{INV-PWMON}$ -1.6 | $V_{INV-PWMON}$ -1.5 | $V_{INV-PWMON}$ -1.4 | V |
| $t_{INV-UVP}$ | Under-Voltage Protection Debounce Time | | 50 | 70 | 90 | µs |
| $V_{INV-BO}$ | PWM and PFC Off Threshold for Brownout Protection | | 1.15 | 1.20 | 1.25 | V |
| $V_{COMP-BO}$ | Limited Voltage on COMP Pin for Brownout Protection | | 1.55 | 1.60 | 1.65 | V |
| $I_{COMP-BURST}$ | Internal Bias Current for PFC Burst Mode | | 120 | 150 | 180 | µA |
| $V_{COMP-H}$ | Comparator Output High Voltage | | 4.80 | | 5.20 | V |
| | Comparator Output High Voltage at PFC Burst Mode | $V_{FB}$=1.3 V, $V_{VIN}$=1.2 V | 2.20 | 2.30 | 2.40 | |
| | | $V_{FB}$=1.3 V, $V_{VIN}$=1.6 V | 2.00 | 2.10 | 2.20 | |
| | | $V_{FB}$=1.3 V, $V_{VIN}$=2 V | 1.80 | 1.90 | 2.00 | |
| $V_{COMP-L}$ | Comparator Output Low Voltage at PFC Burst Mode | RANGE=Open, $V_{FB}$=1.3 V | 0.9 | 1.0 | 1.1 | V |
| $V_{OZ}$ | Zero Duty Cycle Voltage on COMP Pin | | 1.10 | 1.25 | 1.40 | V |
| $I_{COMP}$ | Comparator Output Source Current | $V_{INV}$=2.3 V, $V_{COMP}$=1.5 V | 15 | 30 | 45 | µA |
| | | $V_{INV}$=1.5 V | 0.50 | 0.75 | 1.00 | mA |
| | Comparator Output Sink Current | RANGE=Open, $V_{INV}$=2.75 V, $V_{COMP}$=5 V | 20 | 30 | 40 | µA |
| | | RANGE=Ground, $V_{INV}$=2.65 V, $V_{COMP}$=5 V | 20 | 30 | 40 | |

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## Electrical Characteristics (Continued)

$V_{DD}$=15 V and $T_A$=25°C unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **PFC Current-Sense Section** | | | | | | |
| $V_{CSPFC}$ | Threshold Voltage for Peak Current Cycle-by-Cycle Limit | $V_{COMP}$=5 V | 0.77 | 0.82 | 0.87 | V |
| $t_{PD}$ | Propagation Delay | | | 110 | 200 | ns |
| $t_{BNK}$ | Leading-Edge Blanking Time | | 110 | 180 | 250 | ns |
| $A_V$ | CSPFC Compensation Ratio for THD | | 0.90 | 0.95 | 1.00 | V/V |
| **PFC Output Section** | | | | | | |
| $V_Z$ | PFC Gate Output Clamping Voltage | $V_{DD}$=25 V | 14.0 | 15.5 | 17.0 | V |
| $V_{OL}$ | PFC Gate Output Voltage Low | $V_{DD}$=15 V, $I_O$=100 mA | | | 1.5 | V |
| $V_{OH}$ | PFC Gate Output Voltage High | $V_{DD}$=15 V, $I_O$=100 mA | 8 | | | V |
| $t_R$ | PFC Gate Output Rising Time | $V_{DD}$=12 V, $C_L$=3 nF, 20~80% | 30 | 65 | 100 | ns |
| $t_F$ | PFC Gate Output Falling Time | $V_{DD}$=12 V, $C_L$=3 nF, 80~20% | 30 | 50 | 70 | ns |
| **PFC Zero-Current Detection Section** | | | | | | |
| $V_{ZCD}$ | Input Threshold Voltage Rising Edge | $V_{ZCD}$ Increasing | 1.9 | 2.1 | 2.3 | V |
| $V_{ZCD-HYST}$ | Threshold Voltage Hysteresis | $V_{ZCD}$ Decreasing | 0.25 | 0.35 | 0.45 | V |
| $V_{ZCD-HIGH}$ | Upper Clamp Voltage | $I_{ZCD}$=3 mA | 8 | 10 | | V |
| $V_{ZCD-LOW}$ | Lower Clamp Voltage | | 0.35 | 0.45 | 0.55 | V |
| $V_{ZCD-SSC}$ | Starting Source Current Threshold Voltage | | 0.70 | 0.90 | 1.10 | V |
| $t_{DELAY}$ | Maximum Delay from ZCD to Output Turn-On | $V_{COMP}$=5 V, $f_S$=60 kHz | 100 | | 200 | ns |
| $t_{RESTART-PFC}$ | Restart Time | | 300 | 500 | 700 | µs |
| $t_{INHIB}$ | Inhibit Time (Maximum Switching Frequency Limit) | $V_{COMP}$=5 V | 1.5 | 2.5 | 3.5 | µs |
| $V_{ZCD-DIS}$ | PFC Enable / Disable Function Threshold Voltage | | 0.15 | 0.20 | 0.25 | V |
| $t_{ZCD-DIS}$ | PFC Enable / Disable Function Debounce Time | $V_{ZCD}$=100 mV | 100 | 150 | 200 | µs |

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## Electrical Characteristics (Continued)

$V_{DD}$=15 V and $T_A$=25°C unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **PWM STAGE** | | | | | | |
| **Feedback Input Section** | | | | | | |
| $A_V$ | Input-Voltage to Current Sense Attenuation[4] | $A_V=\Delta V_{CS}/\Delta V_{FB}$, $0 < V_{CS} < 0.9$ | 1/2.75 | 1/3.00 | 1/3.25 | V/V |
| $Z_{FB}$ | Input Impedance[4] | $V_{FB} > V_G$ | 3 | 5 | 7 | kΩ |
| $I_{OZ}$ | Bias Current | $V_{FB}=V_{OZ}$ | | 1.2 | 2.0 | mA |
| $V_{OZ}$ | Zero Duty Cycle Input Voltage | | 0.7 | 0.9 | 1.1 | V |
| $V_{FB-OLP}$ | Open-Loop Protection Threshold Voltage | | 3.9 | 4.2 | 4.5 | V |
| $t_{FB-OLP}$ | The Debounce Time for Open-Loop Protection | | 40 | 50 | 60 | ms |
| $t_{FB-SS}$ | Internal Soft-Start Time[4] | $V_{FB}$=0 V~3.6 V | 4 | 5 | 6 | ms |
| **DET Pin OVP and Valley Detection Section** | | | | | | |
| $V_{DET-OVP}$ | Comparator Reference Voltage | | 2.45 | 2.50 | 2.55 | V |
| Av | Open-Loop Gain[4] | | | 60 | | dB |
| BW | Gain Bandwidth[4] | | | 1 | | MHz |
| $t_{DET-OVP}$ | Output OVP (Auto-Recovery) Debounce Time | | 100 | 150 | 200 | µs |
| $I_{DET-SOURCE}$ | Maximum Source Current | $V_{DET}$=0 V | | | 1 | mA |
| $V_{DET-LOW}$ | Lower Clamp Voltage | $I_{DET}$=1 mA | 0.15 | 0.25 | 0.35 | V |
| $t_{VALLEY-DELAY}$ | Delay Time from Valley Signal Detected to Output Turn-On[4] | | 150 | 200 | 250 | ns |
| $t_{OFF-BNK}$ | Leading-Edge Blanking Time for DET-OVP (2.5 V) and Valley Signal when PWM MOS Turns Off[4] | | | 2.5 | | µs |
| $t_{TIME-OUT}$ | Time-Out After $t_{OFF-MIN}$[4] | | 8 | 9 | 10 | µs |
| **PWM Oscillator Section** | | | | | | |
| $t_{ON-MAX-PWM}$ | Maximum On-Time | | 38 | 45 | 52 | µs |
| $t_{OFF-MIN}$ | Minimum Off-Time | $V_{FB} \geqq V_N$, $T_A$=25°C | | 5 | | µs |
| | | $V_{FB}=V_G$ | | 20.5 | | |
| $V_N$ | Beginning of Green-On Mode at FB Voltage Level | | 1.95 | 2.10 | 2.25 | V |
| $V_G$ | Beginning of Green-Off Mode at FB Voltage Level | | 1.00 | 1.15 | 1.30 | V |
| $\Delta V_G$ | Hysteresis for Beginning of Green-Off Mode at FB Voltage Level[4] | | | 0.1 | | V |

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## Electrical Characteristics (Continued)

$V_{DD}$=15 V and $T_A$=25°C unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CTRL-PFC-BM}$ | Threshold Voltage on FB Pin for PFC Burst Mode | RANGE Pin Internally Open | 1.65 | 1.70 | 1.75 | V |
| | | RANGE Pin Internally Ground | 1.60 | 1.65 | 1.70 | |
| $V_{CTRL-PFC-ON}$ | Threshold Voltage on FB Pin for PFC Normal operating | | 1.75 | 1.80 | 1.85 | V |
| $t_{PFC-BM}$ | Debounce Time for PFC Burst Mode | PFC Normal Operating → Burst Mode | | 100 | | ms |
| $t_{PFC-ON}$ | Debounce Time for PFC Recovery to Normal Operating | PFC Burst Mode→ Normal Operating | | 200 | | µs |
| $t_{STARTER-PWM}$ | Start Timer (Time-Out Timer) | $V_{FB} < V_G$, $T_A$=25°C | 1.85 | 2.25 | 2.65 | ms |
| | | $V_{FB} > V_{FB-OLP}$, $T_A$=25°C | 22 | 28 | 34 | µs |
| **PWM Output Section** | | | | | | |
| $V_{CLAMP}$ | PWM Gate Output Clamping Voltage | $V_{DD}$=25 V | 16.0 | 17.5 | 19.0 | V |
| $V_{OL}$ | PWM Gate Output Voltage Low | $V_{DD}$=15 V, $I_O$=100 mA | | | 1.5 | V |
| $V_{OH}$ | PWM Gate Output Voltage High | $V_{DD}$=15 V, $I_O$=100 mA | 8 | | | V |
| $t_R$ | PWM Gate Output Rising Time | $C_L$ =3 nF, $V_{DD}$=12 V, 20~80% | | 80 | 110 | ns |
| $t_F$ | PWM Gate Output Falling Time | $C_L$=3 nF, $V_{DD}$=12 V, 20~80% | | 40 | 70 | ns |
| **Current Sense Section** | | | | | | |
| $t_{PD}$ | Delay to Output | | | 150 | 200 | ns |
| $V_{LIMIT}$ | Limit Voltage on CSPWM Pin for Over-Power Compensation | $I_{DET} < 75$ µA, $T_A$=25°C | 0.81 | 0.84 | 0.87 | V |
| | | $I_{DET}$=185 µA, $T_A$=25°C | 0.69 | 0.72 | 0.75 | |
| | | $I_{DET}$=350 µA, $T_A$=25°C | 0.55 | 0.58 | 0.61 | |
| | | $I_{DET}$=550 µA, $T_A$=25°C | 0.37 | 0.40 | 0.43 | |
| $V_{SLOPE}$ | Slope Compensation[4] | $t_{ON}$ =45 µs, RANGE=Open | 0.25 | 0.30 | 0.35 | V |
| | | $t_{ON}$=0 µs | 0.05 | 0.10 | 0.15 | |
| $t_{ON-BNK}$ | Leading-Edge Blanking Time | | | 300 | | ns |
| $V_{CS-FLOATING}$ | CSPWM Pin Floating $V_{CSPWM}$ Clamped High Voltage | CSPWM Pin Floating | 4.5 | | 5.0 | V |
| $t_{CS-H}$ | Delay Time, CS Pin Floating | CSPWM Pin Floating | | 150 | | µs |

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## Electrical Characteristics (Continued)

$V_{DD}$=15 V and $T_A$=25°C unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **RT Pin Over-Temperature Protection Section** | | | | | | |
| $T_{OTP}$ | Internal Threshold Temperature for OTP(4) | | 125 | 140 | 155 | °C |
| $T_{OTP-HYST}$ | Hysteresis Temperature for Internal OTP(4) | | | 30 | | °C |
| $I_{RT}$ | Internal Source Current of RT Pin | | 90 | 100 | 110 | µA |
| $V_{RT-AR}$ | Protection Triggering Voltage | | 0.75 | 0.80 | 0.85 | V |
| $V_{RT-OTP-LEVEL}$ | Threshold Voltage for Two-Level Debounce Time | | 0.45 | 0.50 | 0.55 | V |
| $t_{RT-OTP-H}$ | Debounce Time for OTP | | | 10 | | ms |
| $t_{RT-OTP-L}$ | Debounce Time for Externally Triggering | $V_{RT} < V_{RT-OTP-LEVEL}$ | 70 | 110 | 150 | µs |

**Note:**

4. Guaranteed by design.

## Typical Performance Characteristics

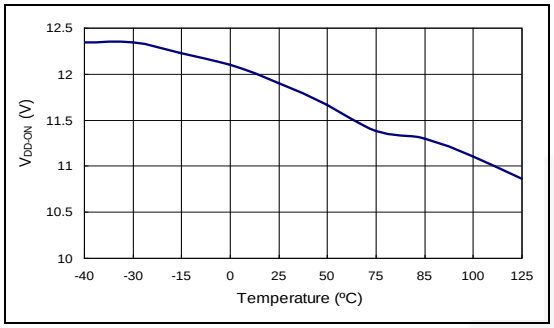



**Figure 5. Turn-On Threshold Voltage**

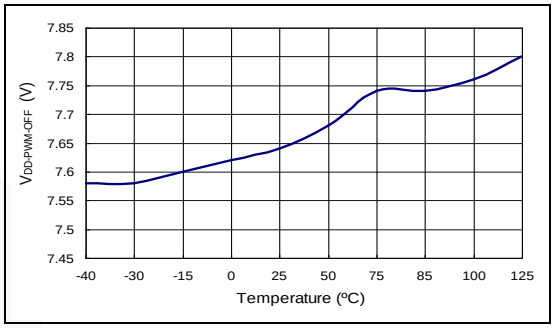



**Figure 6. PWM-Off Threshold Voltage**

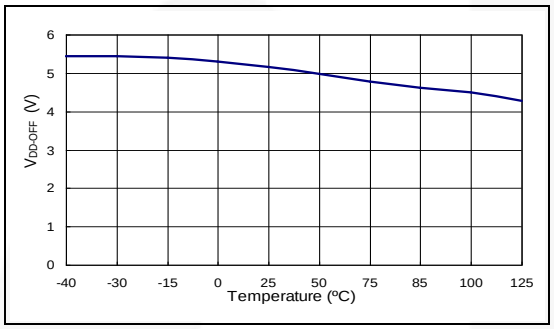



**Figure 7. Turn-Off Threshold Voltage**

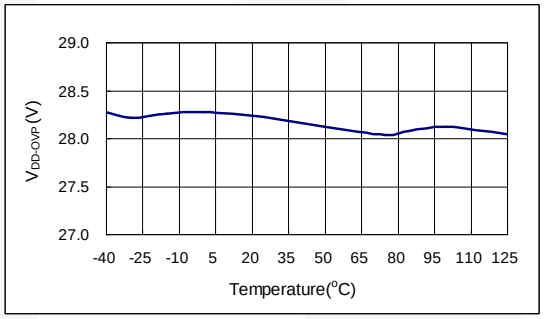



**Figure 8. $V_{DD}$ Over-Voltage Protection Threshold**

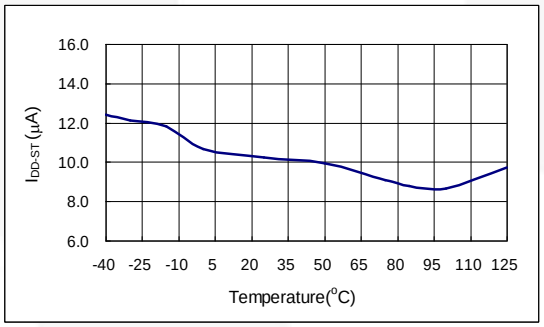



**Figure 9. Startup Current**

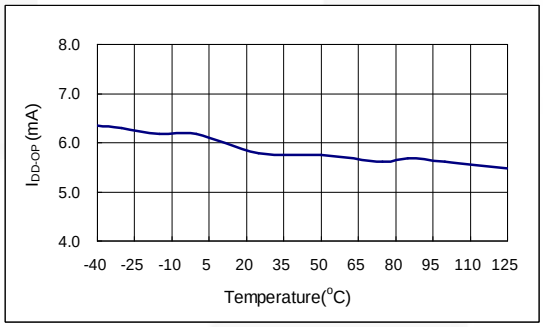



**Figure 10. Operating Current**

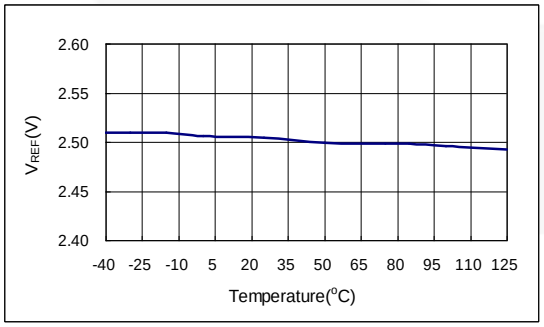



**Figure 11. PFC Output Feedback Reference Voltage**

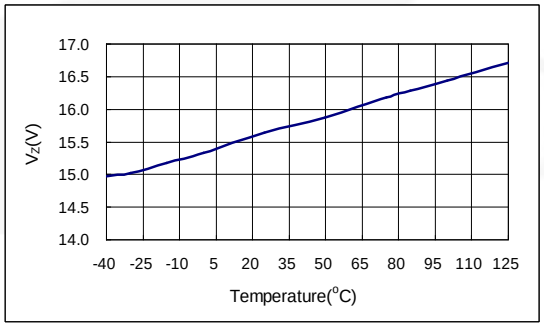



**Figure 12. PFC Gate Output Clamping Voltage**

## Typical Performance Characteristics (Continued)

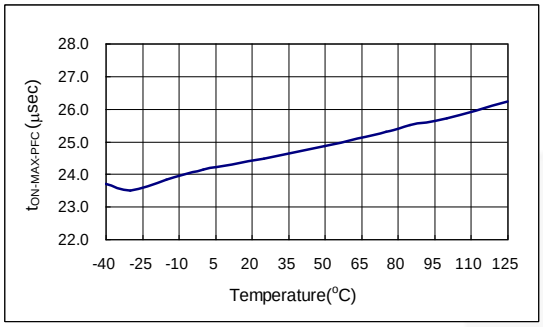



**Figure 13. PFC Maximum On-Time**

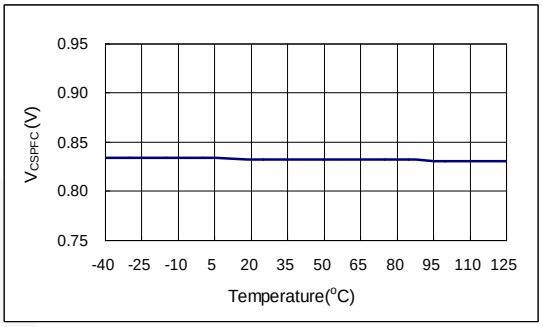



**Figure 14. PFC Peak Current Limit Voltage**

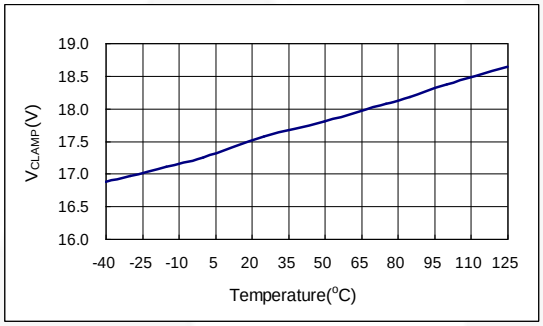



**Figure 15. PWM Gate Output Clamping Voltage**

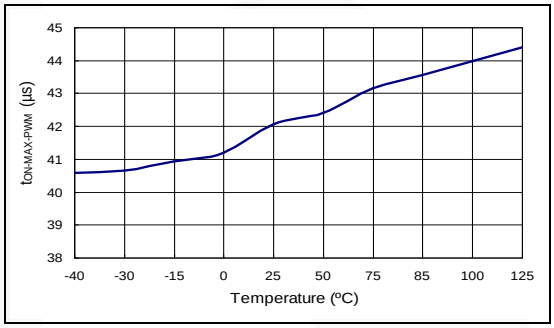



**Figure 16. PWM Maximum On-Time**

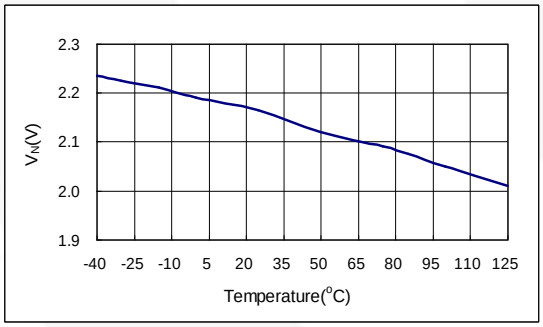



**Figure 17. Beginning of Green-On Mode at $V_{FB}$**

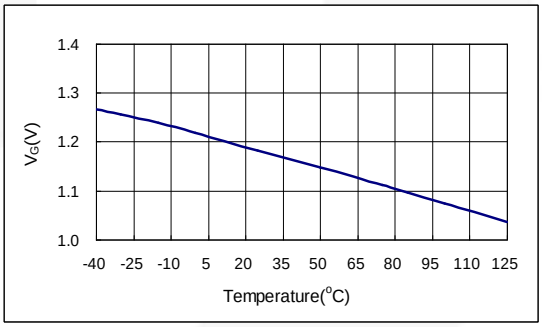



**Figure 18. Beginning of Green-Off Mode at $V_{FB}$**

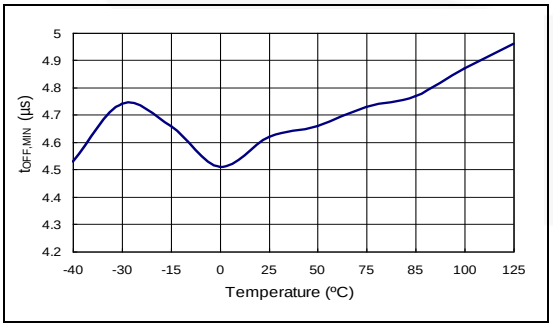



**Figure 19. PWM Minimum Off-Time for $V_{FB} > V_N$**

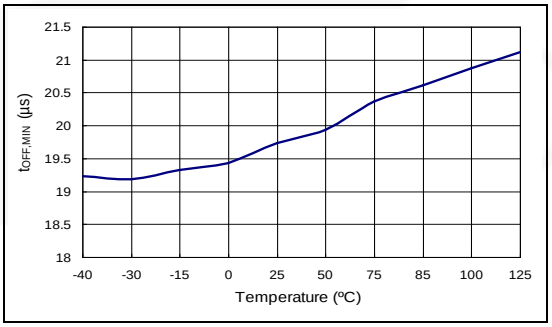



**Figure 20. PWM Minimum Off-Time for $V_{FB}=V_G$**

## Typical Performance Characteristics (Continued)

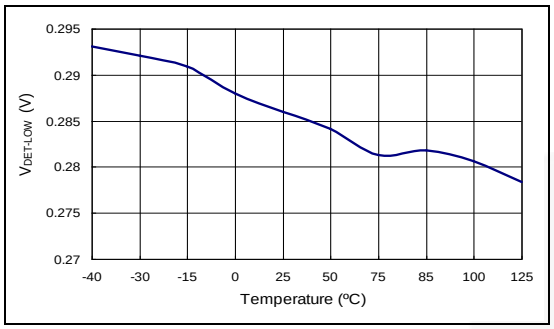



**Figure 21. Lower Clamp Voltage of DET Pin**

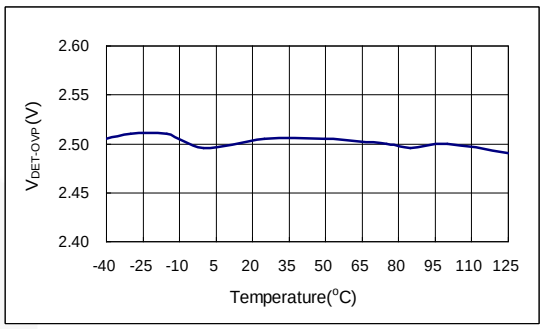



**Figure 22. Reference Voltage for Output Over-Voltage Protection of DET Pin**

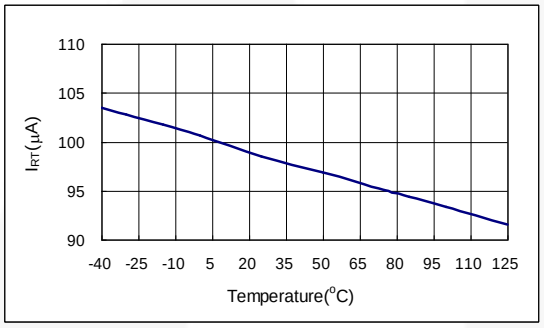



**Figure 23. Internal Source Current of RT Pin**

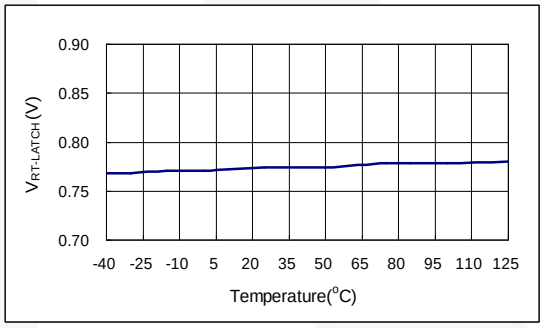



**Figure 24. Over-Temperature Protection Threshold Voltage of RT Pin**

# Functional Description

## PFC Stage

### Multi-Vector Error Amplifier and THD Optimizer

For better dynamic performance, faster transient response, and precise clamping on the PFC output, FAN6920MR uses a transconductance type amplifier with proprietary innovative multi-vector error amplifier. The schematic diagram of this amplifier is shown in Figure 25. The PFC output voltage is detected from the INV pin by an external resistor divider circuit that consists of $R_1$ and $R_2$. When PFC output variation voltage reaches 6% over or under the reference voltage of 2.5 V, the multi-vector error amplifier adjusts its output sink or source current to increase the loop response to simplify the compensated circuit.

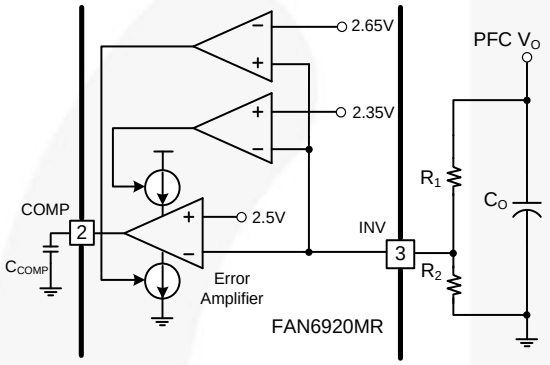



**Figure 25. Multi-Vector Error Amplifier**

The feedback voltage signal on the INV pin is compared with reference voltage 2.5 V, which makes the error amplifier source or sink current to charge or discharge its output capacitor $C_{COMP}$. The COMP voltage is compared with the internally generated sawtooth waveform to determine the on-time of PFC gate. Normally, with lower feedback loop bandwidth, the variation of the PFC gate on-time should be very small and almost constant within one input AC cycle. However, the power factor correction circuit operating at light-load condition has a defect, zero crossing distortion; which distorts input current and makes the system's Total Harmonic Distortion (THD) worse. To improve the result of THD at light-load condition, especially at high input voltage, an innovative THD optimizer is inserted by sampling the voltage across the current-sense resistor. This sampling voltage on current-sense resistor is added into the sawtooth waveform to modulate the on-time of PFC gate, so it is not constant on-time within a half AC cycle. The method of operation block between THD optimizer and PWM is shown in Figure 26. After THD optimizer processes, around the valley of AC input voltage, the compensated on-time becomes wider than the original. The PFC on-time, which is around the peak voltage, is narrowed by the THD optimizer. The timing sequences of the PFC MOS and the shape of the inductor current are shown in Figure 27. Figure 28 shows the difference between calculated fixed on-time mechanism and fixed on-time with THD optimizer during a half AC cycle.

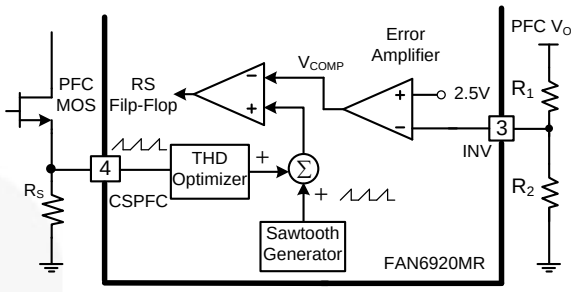



**Figure 26. Multi-Vector Error Amplifier with THD Optimizer**

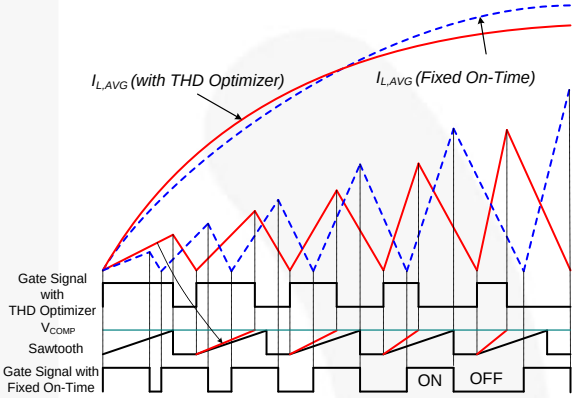



**Figure 27. Operation Waveforms of Fixed On-Time with and without THD Optimizer**

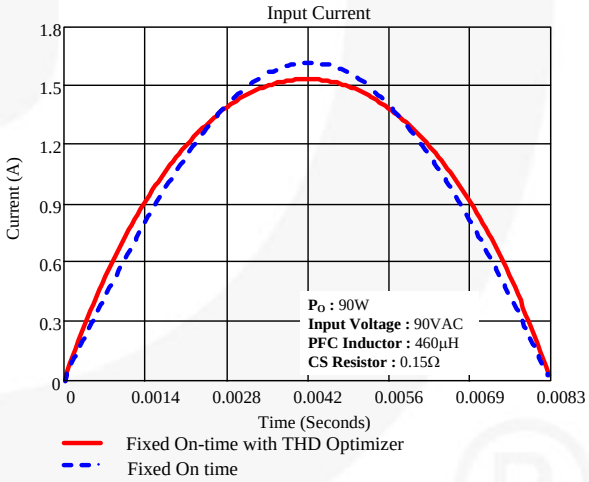



**Figure 28. Calculated Waveforms of Fixed On-Time with and without THD Optimizer During a Half AC Cycle**

### RANGE Pin

A built-in low-voltage MOSFET can be turned on or off according to $V_{VIN}$ voltage level and PFC status. The drain pin of this internal MOSFET is connected to the RANGE pin. Figure 29 shows the status curve of $V_{VIN}$ voltage level and RANGE impedance (open or ground).

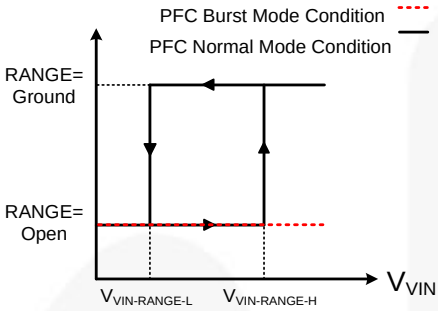



**Figure 29. Hysteresis Behavior between RANGE Pin and VIN Pin Voltage**

### Zero-Current Detection (ZCD Pin)

Figure 30 shows the internal block of zero-current detection. The detection function is performed by sensing the information on an auxiliary winding of the PFC inductor. Referring to Figure 31, when PFC MOS is off, the stored energy of the PFC inductor starts to release to the output load. Then the drain voltage of PFC MOS starts to decrease since the PFC inductor resonates with parasitic capacitance. Once the ZCD pin voltage is lower than the triggering voltage (1.75 V typical), the PFC gate signal is sent again to start a new switching cycle.

If PFC operation needs to be shut down due to abnormal condition, pull the ZCD pin LOW, voltage under 0.2 V (typical), to activate the PFC disable function to stop PFC switching operation.

For preventing excessive high switching frequency at light load, a built-in inhibit timer is used to limit the minimum $t_{OFF}$ time. Even if the ZCD signal has been detected, the PFC gate signal is not sent during the inhibit time (2.5 µs typical).

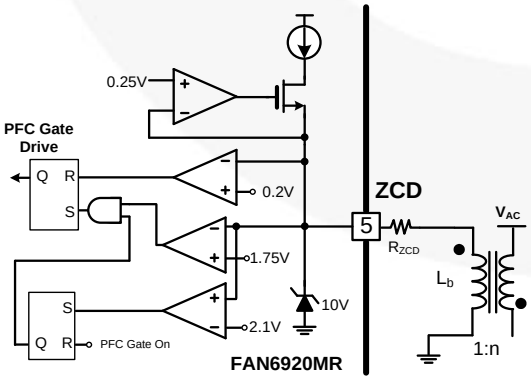



**Figure 30. Internal Block of the Zero-Current Detection**

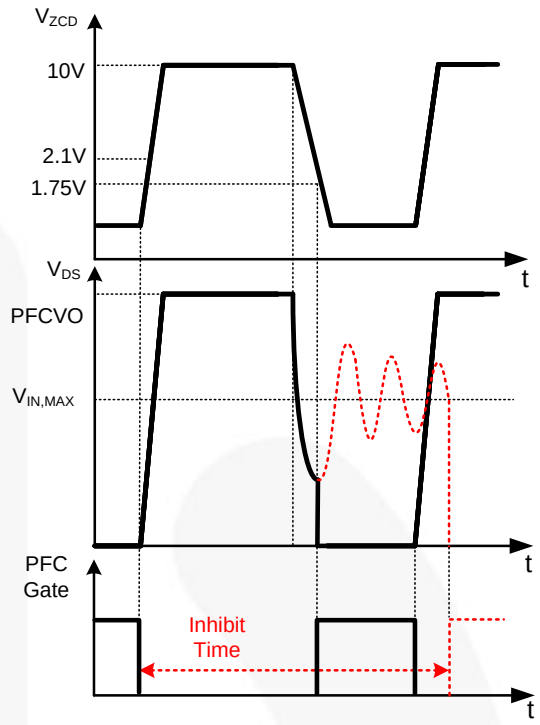



**Figure 31. Operation Waveforms of PFC Zero-Current Detection**

## Protection for PFC Stage

### PFC Output Voltage UVP and OVP (INV Pin)

FAN6920MR provides several kinds of protection for PFC stage. PFC output over- and under-voltage are essential for PFC stage. Both are detected and determined by INV pin voltage, as shown in Figure 32. When INV pin voltage is over 2.75 V or under 0.45 V, due to overshoot or abnormal conditions, and lasts for a de-bounce time around 70 µs; the OVP or UVP circuit is activated to stop PFC switching operation immediately.

The INV pin is not only used to receive and regulate PFC output voltage; it can also perform PFC output OVP/ UVP protection. For failure-mode test, this pin can shut down PFC switching if pin floating occurs.

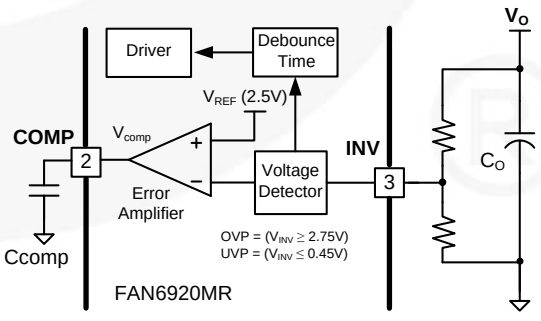



**Figure 32. Internal Block of PFC Over- and Under-Voltage Protection**

### PFC Peak Current Limiting (CSPFC Pin)

During PFC stage switching operation, the PFC switch current is detected by the current-sense resistor on the CSPFC pin and the detected voltage on this resistor is delivered to the input terminal of a comparator and compared with a threshold voltage 0.82 V (typical). Once the CSPFC pin voltage is higher than the threshold voltage, the PFC gate is turned off immediately.

The PFC peak switching current is adjustable by the current-sense resistor. Figure 33 shows the measured waveform of PFC gate and CSPFC pin voltage.

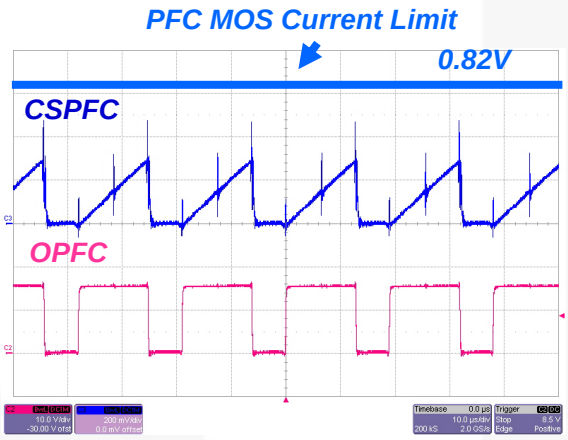



**Figure 33. Cycle-by-Cycle Current Limiting**

### Brownout Protection (VIN Pin)

With AC voltage detection, FAN6920MR can perform brownout / in protection (AC voltage UVP). Figure 34 shows the key operation waveforms of brownout / in protection. Both use the VIN pin to detect AC input voltage level and the VIN pin is connected to AC input by a resistor divider *(refer to Figure 1)*; therefore, the $V_{VIN}$ voltage is proportional to the AC input voltage. When the AC voltage drops and $V_{VIN}$ voltage is lower than 1 V for 100 ms, the UVP protection is activated and the COMP pin voltage is clamped to around 1.6 V. Because PFC gate duty is determined by comparing the sawtooth waveform and COMP pin voltage, lower COMP voltage results in narrow PFC on-time, so that the energy converged is limited and the PFC output voltage decreases. When INV pin voltage is lower than 1.2 V, FAN6920MR stops all PFC and PWM switching operation immediately until $V_{DD}$ voltage drops to turn-off voltage then rises to turn-on voltage again (UVLO).

When the brownout protection is activated, all switching operation is turned off and $V_{DD}$ voltage enters Hiccup Mode up and down continuously. Once $V_{VIN}$ voltage is higher than 1.3 V (typical) and $V_{DD}$ reaches turn-on voltage again, the PWM and PFC gate is sent.

The measured waveforms of brownout / in protection are shown in Figure 35.

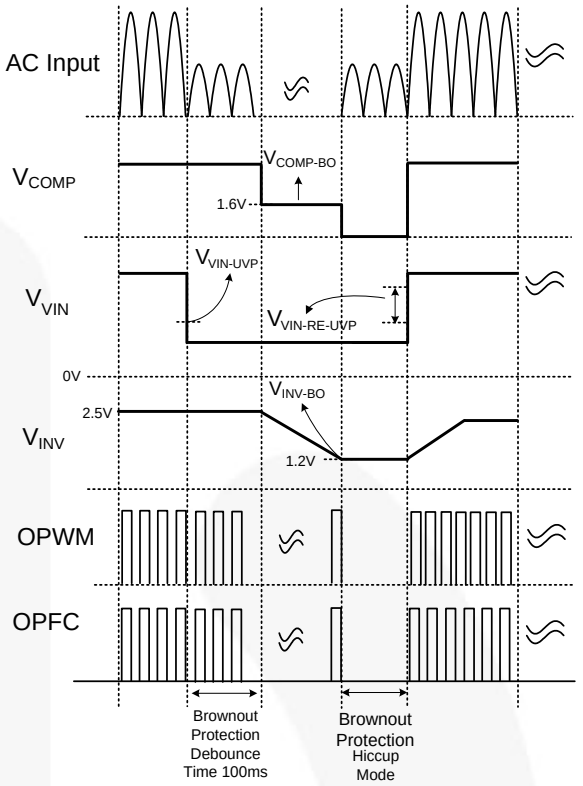



**Figure 34. Operation Waveforms of Brownout / In Protection**

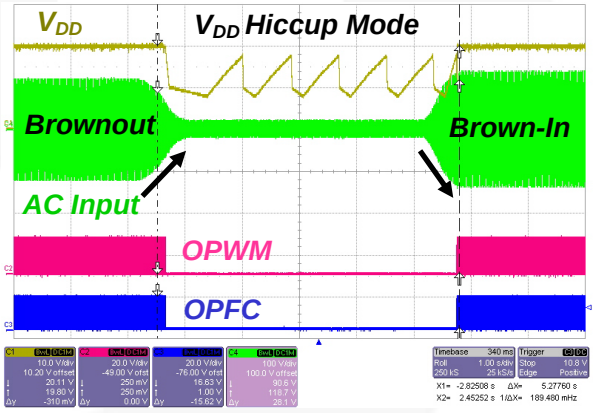



**Figure 35. Measured Waveform of Brownout / In Protection (Adapter Application)**

### PFC Burst Mode

To minimize the power dissipation at light-load condition, the FAN6920MR PFC control enters burst-mode operation. As the load decreases, the PWM feedback voltage ($V_{FB}$) decreases. When $V_{FB} < V_{CTRL-PFC-BM}$ for 100 ms, the device enters PFC burst mode, the $V_{COMP}$ pulls high to $V_{COMP-H}$, and PFC output voltage increases. When the PFC feedback voltage on INV pin ($V_{INV}$) triggers the OVP threshold voltage ($V_{INV-OVP}$), $V_{COMP}$ pulls low to $V_{COMP-L}$, the OPFC pin switching stops and the PFC output voltages start to drop. Once the $V_{INV}$ drops below the feedback comparator reference voltage ($V_{REF}$), $V_{COMP}$ pulls high to $V_{COMP-H}$ and OPFC starts switching again. Burst-mode operation alternately enables and disables switching of the power MOSFET to reduce the switching loss at light-load condition.

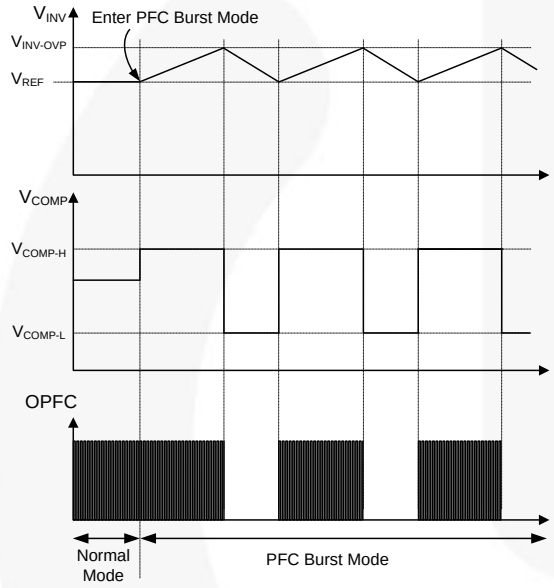



**Figure 36. PFC Burst Mode Behavior**

The $V_{COMP-H}$ is adjusted by the VIN pin voltage, as shown in Figure 37. Since the VIN pin is connected to rectified AC input line voltage through the resistive divider, a higher line voltage generates a higher VIN pin voltage. The $V_{COMP-H}$ decreases as VIN pin voltage increases, limiting the PFC choke current at a higher input voltage to reduce acoustic noise. If the $V_{COMP-H}$ is below the PFC $V_{OZ}$, the PFC automatically shuts down at light load with high line voltage input condition.

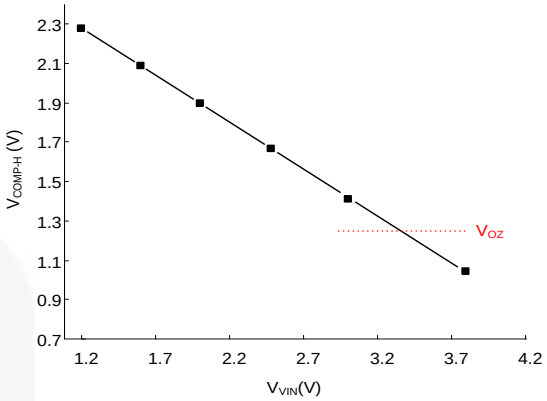



**Figure 37. $V_{COMP-H}$ Voltage vs. $V_{VIN}$ Voltage Characteristic Curve**

## PWM Stage

### HV Startup and Operating Current (HV Pin)

The HV pin is connected to the AC line through a resistor *(refer to Figure 1)*. With a built-in high-voltage startup circuit, when AC voltage is applied to the power system, FAN6920MR provides a high current to charge the external $V_{DD}$ capacitor to speed up controller's startup time and build up normal rated output voltage within three seconds. To save power consumption, after $V_{DD}$ voltage exceeds turn-on voltage and enters normal operation; this high-voltage startup circuit is shut down to avoid power loss from startup resistor.

Figure 38 shows the characteristic curve of $V_{DD}$ voltage and operating current $I_{DD}$. When $V_{DD}$ voltage is lower than $V_{DD-PWM-OFF}$, FAN6920MR stops all switching operation and turns off unnecessary internal circuits to reduce operating current. By doing so, the period from $V_{DD-PWM-OFF}$ to $V_{DD-OFF}$ can be extended and the hiccup mode frequency can be decreased to reduce the input power in case of output short circuit. Figure 39 shows the typical waveforms of $V_{DD}$ voltage and gate signal with hiccup mode operation.

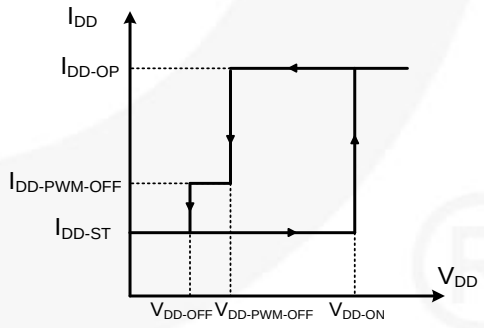



**Figure 38. $V_{DD}$ vs. $I_{DD-OP}$ Characteristic Curve**

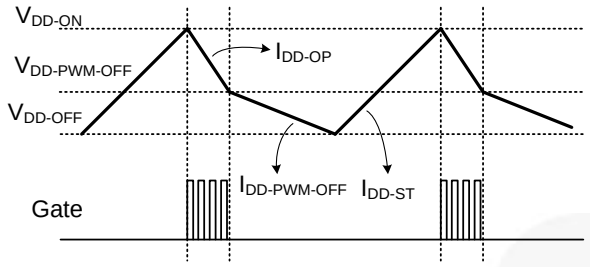



**Figure 39. Typical Waveform of $V_{DD}$ Voltage and Gate Signal at Hiccup Mode Operation**

### Green-Mode Operation and PFC-ON / OFF Control (FB Pin)

Green mode further reduces power loss in the system (e.g. switching loss). Through off-time modulation to regulate switching frequency according to FB pin voltage. When output loading decreases, FB voltage lowers due to secondary feedback movement and the $t_{OFF-MIN}$ is extended. After $t_{OFF-MIN}$ (determined by FB voltage), the internal valley-detection circuit is activated to detect the valley on the drain voltage of the PWM switch. When the valley signal is detected, FAN6920MR outputs a PWM gate signal to turn on the switch and begin a new switching cycle.

With green mode operation and valley detection, at light-load condition; the power system can perform extended valley switching a DCM operation and can further reduce switching loss for better conversion efficiency. The FB pin voltage versus $t_{OFF-MIN}$ time characteristic curve is shown in Figure 40. As Figure 40 shows, FAN6920MR can narrow down to 2.25 ms $t_{OFF}$ time, which is around 440 Hz switching frequency.

Referring to Figure 1 and Figure 2, FB pin voltage is not only used to receive secondary feedback signal to determine gate on-time, but also determines PFC stage operating mode.

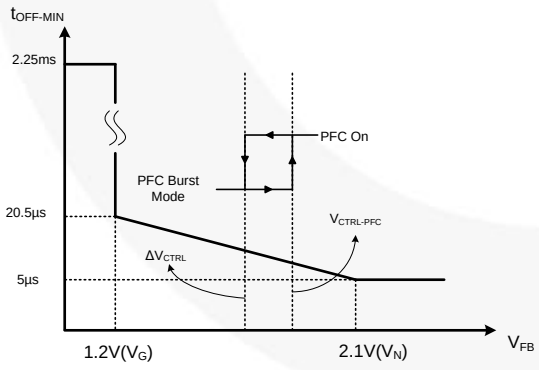



**Figure 40. $V_{FB}$ Voltage vs. $t_{OFF-MIN}$ Time Characteristic Curve**

### Valley Detection (DET Pin)

When FAN6920MR operates in Green Mode, $t_{OFF-MIN}$ is determined by the Green Mode circuit, according to the FB pin voltage level. After $t_{OFF-MIN}$, the internal valley-detection circuit is activated. During $t_{OFF}$ of the PWM switch, when transformer inductor current discharges to zero, the transformer inductor and parasitic capacitor of PWM switch start to resonate concurrently. When the drain voltage on the PWM switch falls, the voltage across on auxiliary winding $V_{AUX}$ also decreases since the auxiliary winding is coupled to the primary winding. Once the $V_{AUX}$ voltage resonates and falls to negative, $V_{DET}$ voltage is clamped by the DET pin (*refer to Figure 41*) and FAN6920MR is forced to flow out a current $I_{DET}$. FAN6920MR reflects and compares this $I_{DET}$ current. If this source current rises to a threshold current, the PWM gate signal is sent out after a fixed delay time (200 ns typical).

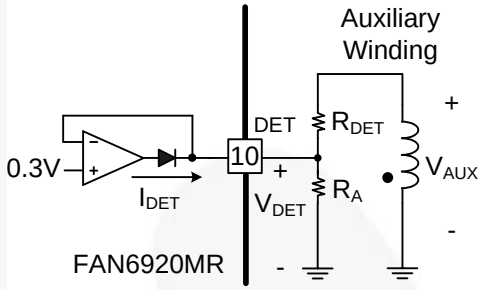



**Figure 41. Valley Detection**

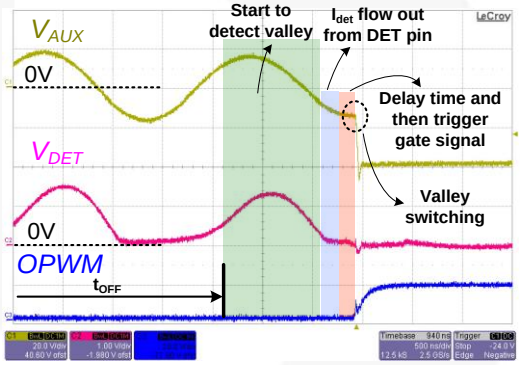



**Figure 42. Measured Waveform of Valley Detection**

### High / Low Line Over-Power Compensation (DET Pin)

Generally, when the power switch turns off, there is a delay from gate signal falling edge to power switch off. This delay is produced by an internal propagation delay of the controller and the turn-off delay of the PWM switch due to gate resistor and gate-source capacitor $C_{ISS}$. At different AC input voltages, this delay produces different maximum output power with the same PWM current limit level. Higher input voltage generates higher maximum output power because applied voltage on primary winding is higher and causes higher rising slope inductor current. It results in higher peak inductor current at the same delay. Furthermore, under the same output wattage, the peak switching current at high line is lower than that at low line. Therefore, to make the maximum output power close at different input voltages, the controller needs to regulate $V_{LIMIT}$ voltage of the CSPWM pin to control the PWM switch current.

Referring to Figure 43, during $t_{ON}$ of the PWM switch, the input voltage is applied to primary winding and the voltage across on auxiliary winding $V_{AUX}$ is proportional to primary winding voltage. As the input voltage increases, the reflected voltage on auxiliary winding

$V_{AUX}$ becomes higher as well. FAN6920MR also clamps the DET pin voltage and flows out current $I_{DET}$. Since the current $I_{DET}$ is in accordance with $V_{AUX}$ voltage, FAN6920MR depends on this current during $t_{ON}$ to regulate the current limit level of the PWM switch to perform high / low line over-power compensation.

As the input voltage increases, the reflected voltage on the auxiliary winding $V_{AUX}$ becomes higher as well as the current $I_{DET}$ and the controller regulates the $V_{LIMIT}$ to a lower level.

The $R_{DET}$ resistor is connected from auxiliary winding to the DET pin. Engineers can adjust this $R_{DET}$ resistor to get proper $V_{LIMIT}$ voltage to fit the specification of over-power or over-current protection. The characteristic curve of $I_{DET}$ current vs. $V_{LIMIT}$ voltage on CSPWM pin is shown in Figure 44.

$$I_{DET} = \left[V_{IN} \times \left(N_A / N_P\right)\right] / R_{DET} \quad (1)$$

where $V_{IN}$ is input voltage; $N_A$ is turn number of auxiliary winding; and $N_P$ is turn number of primary winding.

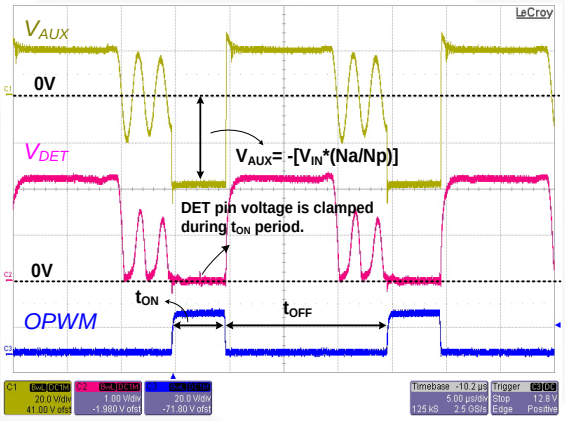



**Figure 43. Relationship between $V_{AUX}$ and $V_{IN}$**

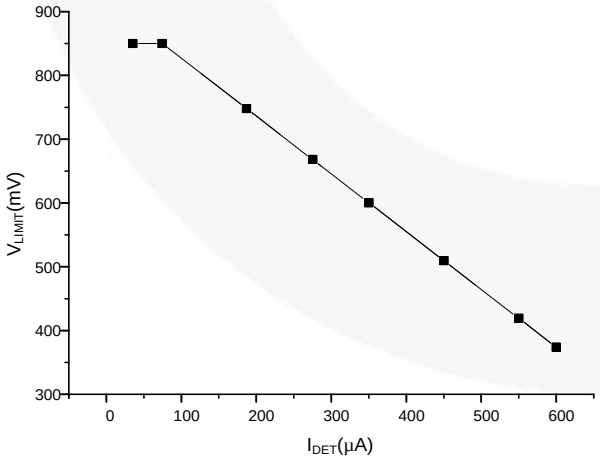



**Figure 44. $I_{DET}$ Current vs. $V_{LIMIT}$ Voltage Characteristic Curve**

### Leading-Edge Blanking (LEB)

When the PFC or PWM switches are turned on, a voltage spike is induced on the current-sense resistor due to the reciprocal effect by reverse-recovery energy of the output diode and $C_{OSS}$ of power MOSFET. To prevent this spike, a leading-edge blanking time is built-in and a small RC filter (e.g. 100 Ω, 470 pF) is recommended between the CSPWM pin and GND.

## Protection for PWM Stage

### VDD Pin Over-Voltage Protection (OVP)

$V_{DD}$ over-voltage protection prevents device damage once $V_{DD}$ voltage is higher than device stress rating voltage. In the case of $V_{DD}$ OVP, the controller stops all switching operation immediately and enters auto-recovery protection.

### Adjustable Over-Temperature Protection and Externally Protection Triggering (RT Pin)

Figure 45 is a typical application circuit with an internal block of RT pin. As shown, a constant current $I_{RT}$ flows out from the RT pin, so the voltage $V_{RT}$ on the RT pin can be obtained as $I_{RT}$ current multiplied by the resistor, which consists of NTC resistor and $R_A$ resistor. If the RT pin voltage is lower than 0.8 V and lasts for a debounce time, auto-recovery protection is activated and stops all PFC and PWM switching.

RT pin is usually used to achieve over-temperature protection with a NTC resistor and provide external protection triggering for additional protection. Engineers can use an external triggering circuit (e.g. transistor) to pull the RT pin low and activate controller auto-recovery protection.

Generally, the external protection triggering needs to activate rapidly since it is usually used to protect the power system from abnormal conditions. Therefore, the protection debounce time of the RT pin is set to around 110 µs once the RT pin voltage is lower than 0.5 V.

For over-temperature protection, because the temperature does not change immediately; the RT pin voltage is reduced slowly as well. The debounce time for adjustable OTP should not need a fast reaction. To prevent improper protection triggering on the RT pin due to exacting test condition (e.g. lightning test); when the RT pin triggering voltage is higher than 0.5 V, the protection debounce time is set to around 10 ms. To avoid improper triggering on the RT pin, add a small value capacitor (e.g. 1000 pF) paralleled with NTC and the $R_A$ resistor.

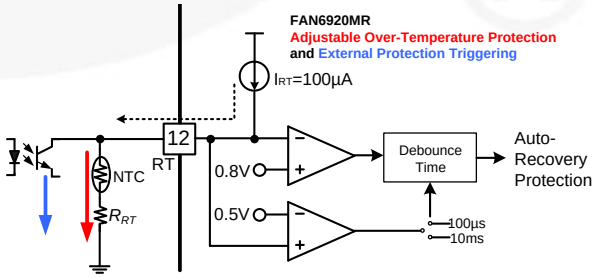



**Figure 45. Adjustable Over-Temperature Protection**

### Output Over-Voltage Protection (DET Pin)

Referring to Figure 46, during the discharge time of PWM transformer inductor; the voltage across on auxiliary winding is reflected from secondary winding and therefore the flat voltage on the DET pin is proportional to the output voltage. FAN6920MR can sample this flat voltage level after a $t_{OFF}$ blanking time to perform output over-voltage protection. This $t_{OFF}$ blanking time is used to ignore the voltage ringing from leakage inductance of PWM transformer. The sampling flat voltage level is compared with internal threshold voltage 2.5 V and, once the protection is activated, FAN6920MR enters auto-recovery protection.

The controller can protect rapidly by this kind of cycle-by-cycle sampling method in the case of output over voltage. The protection voltage level can be determined by the ratio of external resistor divider $R_A$ and $R_{DET}$. The flat voltage on DET pin can be expressed by the following equation:

$$V_{DET} = \left(N_A / N_S\right) \times V_O \times \frac{R_A}{R_{DET} + R_A} \quad (2)$$

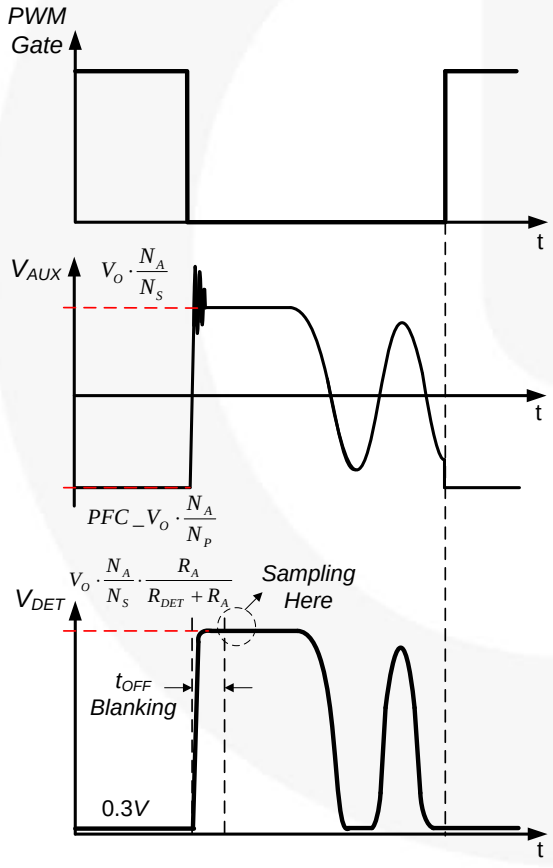



**Figure 46. Operation Waveform of Output Over-Voltage Detection**

### Open-Loop, Short-Circuit, and Overload Protection (FB Pin)

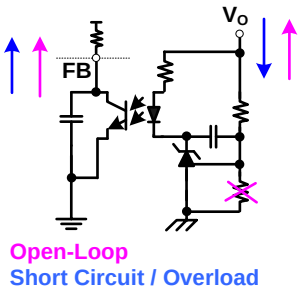


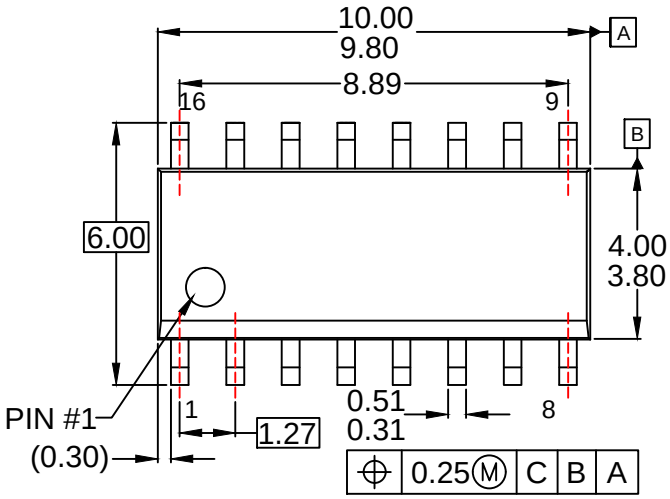

**Figure 47. FB Pin Open-Loop, Short Circuit, and Overload Protection**

Referring to Figure 47; outside of FAN6920MR, the FB pin is connected to the collector of transistor of an opto-coupler. Inside, the FB pin is connected to an internal voltage bias through a resistor of around 5 kΩ.

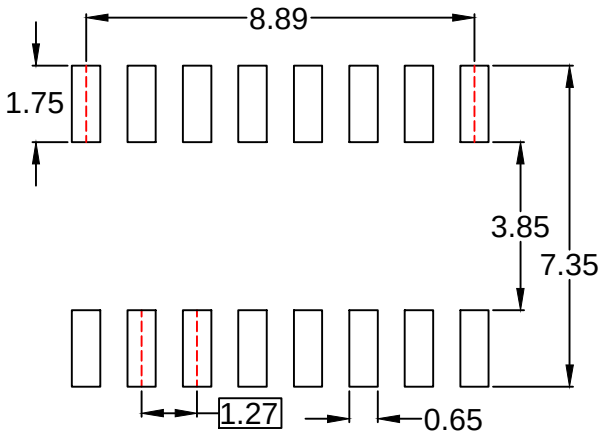
As the output loading is increased, the output voltage is decreased and the sink current of the transistor of the opto-coupler on primary side is reduced. The FB pin voltage is increased by internal voltage bias. In the case of an open loop, output short-circuit, or overload condition; this sink current is further reduced and the FB pin voltage is pulled HIGH by internal bias voltage. When the FB pin voltage is higher than 4.2 V for 50 ms, the FB pin protection is activated.

### Under-Voltage Lockout (UVLO, VDD Pin)

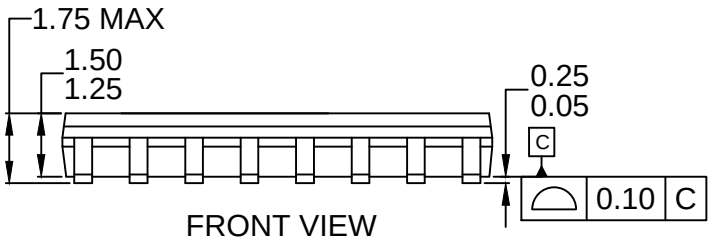
Referring to Figure 38 and Figure 39, the turn-on and turn-off $V_{DD}$ threshold voltages are fixed at 18 V and 10 V, respectively. During startup, the hold-up capacitor ($V_{DD}$ capacitor) is charged by HV startup current until $V_{DD}$ voltage reaches the turn-on voltage. Before the output voltage rises to rated voltage and delivers energy to the $V_{DD}$ capacitor from auxiliary winding, this hold-up capacitor must sustain the $V_{DD}$ voltage energy for operation. When $V_{DD}$ voltage reaches turn-on voltage, FAN6920MR starts all switching operation if no protection is triggered before $V_{DD}$ voltage drops to turn-off voltage $V_{DD\text{-}PWM\text{-}OFF}$.



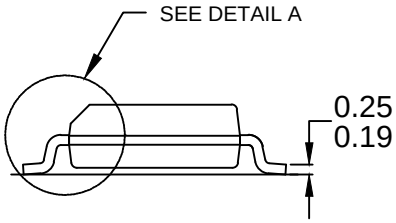

TOP VIEW

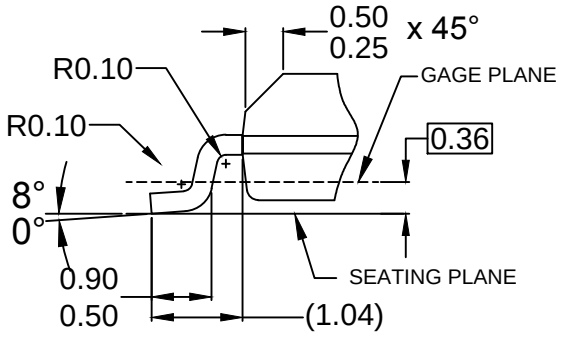



LAND PATTERN RECOMMENDATION




FRONT VIEW

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