MACH4-96/MACH4LV-96

High-Performance EE CMOS Programmable Logic

DISTINCTIVE CHARACTERISTICS

- **100 pins in TQFP**
- **96 macrocells**
- **7.5 ns t_{PD} Commercial, 10 ns t_{PD} Industrial**
- **133 MHz f_{CNT}**
- **48 I/Os; 4 dedicated inputs/clocks; 4 dedicated inputs**
- **144 flip-flops**
  - 96 Macrocell flip-flops
  - 48 Input flip-flops
- **Up to 20 product terms per macrocell, with XOR**
- **Flexible clocking**
  - Four global clock pins with selectable edges
  - Asynchronous mode available for each macrocell
- **3 MACH111SP-size blocks**
- **SpeedLocking™ for guaranteed fixed timing**
- **5-V and 3.3-V supply voltage options**
  - JEDEC compatible for both 5-V and 3.3-V versions
- **5-V or 3.3-V in-system programmable through JTAG (IEEE Std. 1149.1) interface**
- **JTAG boundary scan testing capability**
- **Input and output switch matrices for high routability and pinout retention**
- **Zero-hold-time input register option**
- **Peripheral Component Interconnect (PCI) compliant (-7/-10/-12 speed grades)**
- **Enhanced features**
  - Bus-Friendly™ inputs and I/Os
  - PAL® Block programmable power-down mode for further power savings
  - Individual output slew rate control
  - Both 5-V and 3.3-V supply voltage options are safe for mixed supply voltage system designs

GENERAL DESCRIPTION

The MACH4-96 (M4-96) and MACH4LV-96 (M4LV-96) are members of Vantis' high-performance EE CMOS MACH 4 family. This device has approximately 3 times the macrocell capability of the popular MACH111SP, with significant additional density and functional features.

The M4-96 (M4LV-96) consists of 6 PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output

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switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The M4-96 (M4LV-96) has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per macrocell can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The M4-96 (M4LV-96) macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer using software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

The M4-96 (M4LV-96) features include: each PAL block has a programmable power-down mode for further power saving of up to 50%; each I/O has an individually programmable output slew-rate control bit; and all inputs and I/Os feature the Bus-Friendly circuitry which weakly holds the voltage at the input to a logic low or high level depending on the last driven logic level. Both 5-V and 3.3-V supply operation versions are safe for mixed supply voltage system designs. The 3.3-V supply operation device has its power consumption significantly reduced due to the lower supply voltage, while providing the same high performance as the 5-V version.

Vantis offers software design support for MACH devices through its own development system and device fitters integrated into third-party CAE tools. Platform support extends across PCs, Sun and HP workstations under advanced operating systems such as Windows 3.1, Windows 95 and NT, SunOS and Solaris, and HPUX.

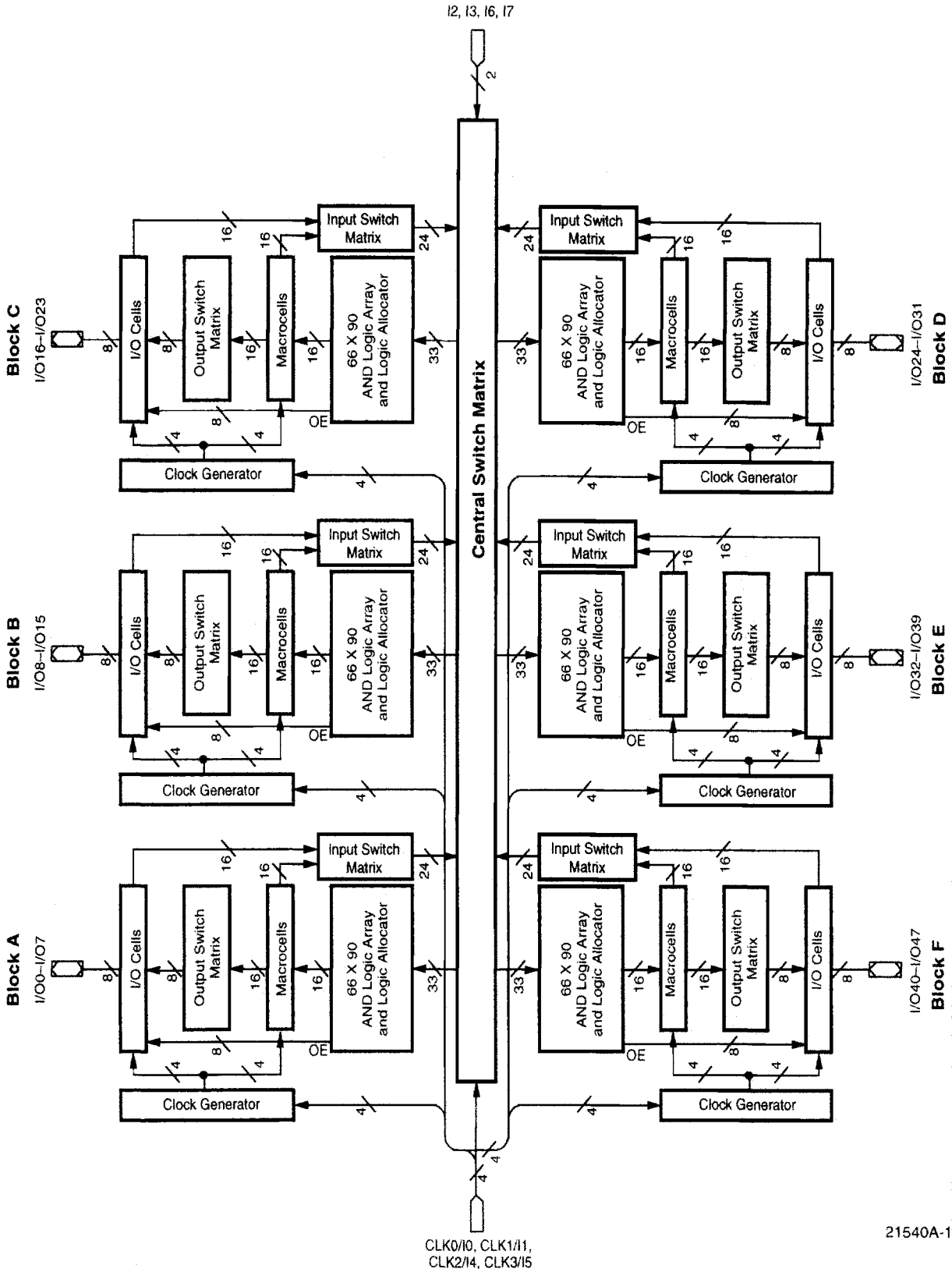
MACHXL® software is a complete development system for the PC, supporting Vantis' MACH devices. It supports design entry with Boolean and behavioral syntax, state machine syntax and truth tables. Functional simulation and static timing analysis are also included in this easy-to-use system. This development system includes high-performance device fitters for all MACH devices.

The same fitter technology included in MACHXL software is seamlessly incorporated into third-party tools from leading CAE vendors such as Synario, Viewlogic, Mentor Graphics, Cadence and MINC. Interface kits and MACHXL configurations are also available to support design entry and verification with other leading vendors such as Synopsys, Exemplar, OrCAD, Synplicity and Model Technology. These MACHXL configurations and interfaces accept EDIF 2.0.0 netlists, generate JEDEC files for MACH devices, and create industry-standard SDF, VITAL-compliant VHDL and Verilog output files for design simulation.

Vantis offers in-system programming support for MACH devices through its MACHPRO® software enabling MACH device programmability through JTAG compliant ports and easy-to-use PC interface. Additionally, MACHPRO generated vectors work seamlessly with HP3070, GenRad and Teradyne testers to program MACH devices or test them for connectivity.

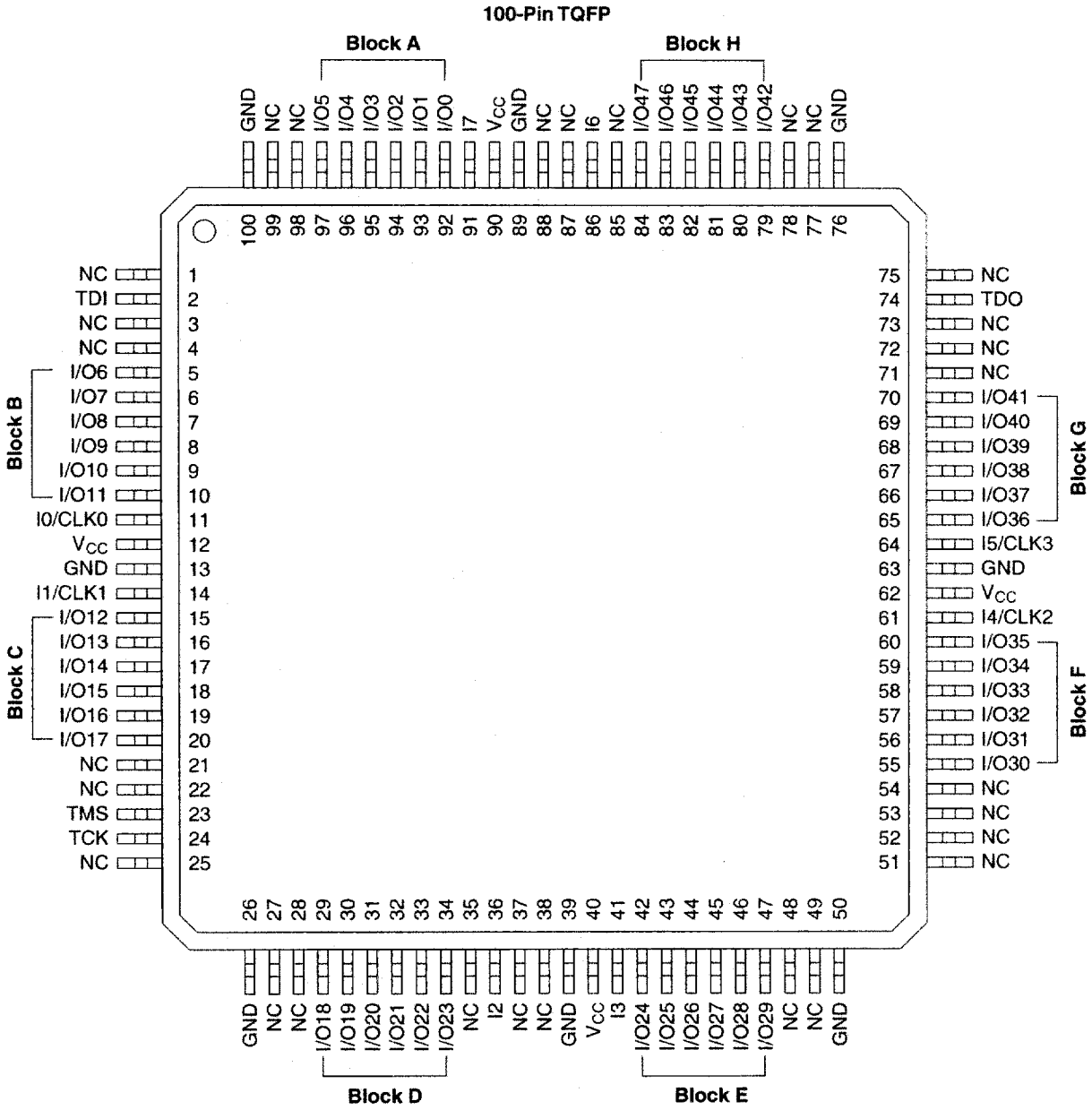
All MACH devices are supported by industry standard programmers available from a number of vendors. These programmer vendors include Advin Systems, BP Microsystems, Data I/O Corporation, Hi-Lo Systems, SMS GmbH, Stag House, and System General.

BLOCK DIAGRAM



CONNECTION DIAGRAM

Top View



PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
NC = No connect
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = 0°C to +70°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4		3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	All PAL Blocks low-power V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 1 MHz, T_A = 25°C (Note 5)		60		mA
		All PAL Blocks full-power V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 1 MHz, T_A = 25°C (Note 5)		105		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1 *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note1)

Parameter Symbol	Parameter Description				-7		-10		-12		-15		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				3	7.5	3	10	3	12	3	15	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	3.5		4		5		8		ns
				T-type	4.5		5		6		9		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				3.5		4		5		8		ns
t_{COA}	Product Term Clock to Output				4	9.5	4	12	4	14	4	18	ns
t_{WLA}	Product Term, Clock Width			LOW	4		5		8		9		ns
t_{WHA}				HIGH	4		5		8		9		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	74.0		62.5		52.6		38.5		MHz
				T-type	71.4		58.8		50.0		37		MHz
		Internal Feedback (f_{CNTA})		D-type	90.9		71.4		58.8		47.6		MHz
				T-type	83.3		66.7		55.6		45.4		MHz
		No Feedback (Note 3)	$1/(t_{WLA} + t_{WHA})$		125		100		62.5		55.6		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	5.5		6		7		10		ns
				T-type	6.5		7		8		11		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		0		ns
t_{COS}	Global Clock to Output				2	5.5	2	6.5	2	8	2	10	ns
t_{WLS}	Global Clock Width			LOW	3		5		6		6		ns
t_{WHS}				HIGH	3		5		6		6		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	90		80		66.7		50		MHz
				T-type	83.3		74.1		62.5		47.6		MHz
		Internal Feedback (f_{CNTS})		D-type	133		100		83.3		66.6		MHz
				T-type	117		90.9		76.9		62.5		MHz
		No Feedback (Note 3)	$1/(t_{WLS} + t_{WHS})$		166.7		100		83.3		88.3		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				4		4		5		8		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note1)

Parameter Symbol	Parameter Description		-7		-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{HLA}	Latch Data Hold Time Using Product Term Clock		4		4		5		8		ns
t_{GOA}	Product Term Gate to Output			11		13		16		19	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		4		5		6		9		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		6		7		8		10		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		0		ns
t_{GOS}	Gate to Output		6			7.5		10		11	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		5		6		6		ns
t_{ICO}	Input Register Clock to Combinatorial Output			14		15.5		18		20	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	7		8		9		15		
		T-type	8		9		10		16		
t_{WICL}	Input Register Clock Width	LOW	4.5		5		6		6		ns
t_{WICH}		HIGH	4.5		5		6		6		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	110		100		83.3		83.3		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			12		14		16		20	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			14		16		18		22	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		4		4		14		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		9		9		16		ns
t_{WIGL}	Input Latch Gate Width LOW		5		5		6		6		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			12		14		16		20	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		10		10		12		15		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		8		8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			12		14		16		20	ns
t_{APW}	Asynchronous Preset Width (Note 2)		10		10		12		15		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		8		8		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	9.5	2	10	2	12	2	15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	9.5	2	10	2	12	2	15	ns
Input Register with Standard-Hold-Time Option											
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			10		12		14		17	ns
t_{SIR}	Input Register Setup Time		2		2		2		2		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note1)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HIR}	Input Register Hold Time	3		3		3		4		ns
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	3		3		3		4		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		4		4		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	7		8		9		12		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		12		14		16		19	ns
Input Register with Zero-Hold-Time Option										
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		16		18		20		23	ns
t_{SIR}^{I}	Input Register Setup Time	6		6		6		6		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		6		6		6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	11		13		16		16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	12		15		18		18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		18		20		22		25	ns
Power-Down Mode and Slow Slew Rate Option										
t_{LP}	Power-down mode delay adder. For macrocells in a power-down mode PAL block, this parameter must be added to: t_{PD}, t_{COA}, t_{SS}, t_{GOA}, t_{SLS}, t_{ICO}, t_{ICS}, t_{IGO}, t_{IGOL}, t_{IGSS}, t_{AR}, t_{ARR}, t_{AP}, t_{APR}, t_{EA}, t_{ER}, t_{PDL}, t_{SLLS}, t_{PDLL}		2.5		2.5		2.5		2.5	ns
t_{SLW}	Slow slew rate delay adder. For an output configured with slow slew rate option, this parameter must be added to: t_{PD}, t_{COA}, t_{COS}, t_{GOA}, t_{GOS}, t_{ICO}, t_{IGO}, t_{IGOL}, t_{AP}, t_{AR}, t_{PDL}, t_{PDLL}		2.5		2.5		2.5		2.5	ns

Notes:

1 *See Switching Test Circuit for test conditions.*

2 *These parameters are not 100% tested, but are evaluated at initial characterization.*

3 *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +4.5 V

DC Input Voltage . . . . . –0.5 V to 6.0 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = 0°C to +70°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 µA	V_{CC} – 0.2			V
			I_{OH} = –3.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2	V
			I_{OL} = 24 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		–0.3		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–5	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				5	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				–5	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–15		–160	mA
I_{CC}	Supply Current	All PAL Blocks low-power, V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 1 MHz, T_A = 25°C (Note 4)			60		mA
		All PAL Blocks full-power, V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 1 MHz, T_A = 25°C (Note 4)			105		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note1)

Parameter Symbol	Parameter Description				-7		-10		-12		-15		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				3	7.5	3	10	3	12	3	15	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	3.5		4		5		8		ns
				T-type	4.5		5		6		9		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				3.5		4		5		8		ns
t_{COA}	Product Term Clock to Output				4		4	12	4	14	4	18	ns
t_{WLA}	Product Term, Clock Width			LOW	4		5		8		9		ns
t_{WHA}				HIGH	4		5		8		9		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	74.0		62.5		52.6		38.5		MHz
				T-type	71.4		58.8		50.0		37		MHz
		Internal Feedback (f_{CNTA})		D-type	90.9		71.4		58.8		47.6		MHz
				T-type	83.3		66.7		55.6		45.4		MHz
		No Feedback (Note 3)	$1/(t_{WLA} + t_{WHA})$		125		100		62.5		55.6		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	5.5		6		7		10		ns
				T-type	6.5		7		8		11		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		0		ns
t_{COS}	Global Clock to Output				2	5.5	2	6.5	2	8	2	10	ns
t_{WLS}	Global Clock Width			LOW	3		5		6		6		ns
t_{WHS}				HIGH	3		5		6		6		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	90		80		66.7		50		MHz
				T-type	83.3		74.1		62.5		47.6		MHz
		Internal Feedback (f_{CNTS})		D-type	133		100		83.3		66.6		MHz
				T-type	117		90.9		76.9		62.5		MHz
		No Feedback (Note 3)	$1/(t_{WLS} + t_{WHS})$		166.7		100		83.3		88.3		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				4		4		5		8		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note1)

Parameter Symbol	Parameter Description		-7		-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{HLA}	Latch Data Hold Time Using Product Term Clock		4		4		5		8		ns
t_{GOA}	Product Term Gate to Output			11		13		16		19	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		4		5		6		9		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		6		7		8		10		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		0		ns
t_{GOS}	Gate to Output		6			7.5		10		11	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		5		6		6		ns
t_{ICO}	Input Register Clock to Combinatorial Output		14			15.5		18		20	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	7		8		9		15		
		T-type	8		9		10		16		
t_{WICL}	Input Register Clock Width	LOW	4.5		5		6		6		ns
t_{WICH}		HIGH	4.5		5		6		6		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	110		100		83.3		83.3		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			12		14		16		20	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			14		16		18		22	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		4		4		14		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		9		9		16		ns
t_{WIGL}	Input Latch Gate Width LOW		5		5		6		6		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			12		14		16		20	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		10		10		12		15		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		8		8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			12		14		16		20	ns
t_{APW}	Asynchronous Preset Width (Note 2)		10		10		12		15		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		8		8		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	9.5	2	10	2	12	2	15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	9.5	2	10	2	12	2	15	ns
Input Register with Standard-Hold-Time Option											
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			10		12		14		17	ns
t_{SIR}	Input Register Setup Time		2		2		2		2		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note1)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HIR}	Input Register Hold Time	3		3		3		4		ns
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	3		3		3		4		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		4		4		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	7		8		9		12		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches	12			14		16		19	ns
Input Register with Zero-Hold-Time Option										
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		16		18		20		23	ns
t_{SIR}^{I}	Input Register Setup Time	6		6		6		6		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		6		6		6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	11		13		16		16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	12		15		18		18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		18		20		22		25	ns
Power-Down Mode and Slow Slew Rate Option										
t_{LP}	Power-down mode delay adder. For macrocells in a power-down mode PAL block, this parameter must be added to: t_{PD}, t_{COA}, t_{SS}, t_{GOA}, t_{SLS}, t_{ICO}, t_{ICS}, t_{IGO}, t_{IGOL}, t_{IGSS}, t_{AR}, t_{ARR}, t_{AP}, t_{APR}, t_{EA}, t_{ER}, t_{PDL}, t_{SLLS}, t_{PDLL}		2.5		2.5		2.5		2.5	ns
t_{SLW}	Slow slew rate delay adder. For an output configured with slow slew rate option, this parameter must be added to: t_{PD}, t_{COA}, t_{COS}, t_{GOA}, t_{GOS}, t_{ICO}, t_{IGO}, t_{IGOL}, t_{AP}, t_{AR}, t_{PDL}, t_{PDLL}		2.5		2.5		2.5		2.5	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.50 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4		3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	-30		-160	mA
I_{CC}	Supply Current	All PAL Blocks low-power V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 1 MHz, T_A = 25°C (Note 5)		60		mA
		All PAL Blocks full-power V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 1 MHz, T_A = 25°C (Note 5)		105		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note1)

Parameter Symbol	Parameter Description				-10		-12		-14		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				3	10	3	12	3	14	3	18	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	4		5		8		10		ns
				T-type	5		6		9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				4		5		8		10		ns
t_{COA}	Product Term Clock to Output				4	12	4	14	4	18	4	20	ns
t_{WLA}	Product Term, Clock Width			LOW	5		8		9		10		ns
t_{WHA}				HIGH	5		8		9		10		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	62.5		52.6		38.5		33.3		MHz
				T-type	58.8		50.0		37		32.2		MHz
		Internal Feedback (f_{CNTA})		D-type	71.4		58.8		47.6		35.7		MHz
				T-type	66.7		55.6		45.4		34.4		MHz
		No Feedback (Note 3)	$1/(t_{WLA} + t_{WHA})$		100		62.5		55.6		50.0		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	6		7		10		12		ns
				T-type	7		8		11		13		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		0		ns
t_{COS}	Global Clock to Output				2	6.5	2	8	2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	5		6		6		7		ns
t_{WHS}				HIGH	5		6		6		7		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	80		66.7		50		41.7		MHz
				T-type	74.1		62.5		47.6		40.0		MHz
		Internal Feedback (f_{CNTS})		D-type	100		83.3		66.6		58.8		MHz
				T-type	90.9		76.9		62.5		55.5		MHz
		No Feedback (Note 3)	$1/(t_{WLS} + t_{WHS})$		100		83.3		88.3		71.4		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				4		5		8		10		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note1)

Parameter Symbol	Parameter Description		-10		-12		-14		-18		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{HLA}	Latch Data Hold Time Using Product Term Clock		4		5		8		10		ns
t_{GOA}	Product Term Gate to Output			13		16		19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		6		9		11		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		7		8		10		12		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		0		ns
t_{GOS}	Gate to Output			7.5		10		11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		6		6		7		ns
t_{ICO}	Input Register Clock to Combinatorial Output			15.5		18		20		22	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	8		9		15		17		
		T-type	9		10		16		18		
t_{WICL}	Input Register Clock Width	LOW	5		6		6		7		ns
t_{WICH}		HIGH	5		6		6		7		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	100		83.3		83.3		71.4		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			14		16		20		22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			16		18		22		24	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		4		14		16		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		9		16		18		ns
t_{WIGL}	Input Latch Gate Width LOW		5		6		6		7		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			14		16		20		22	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		10		12		15		17		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		8		10		15		17		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			14		16		20		22	ns
t_{APW}	Asynchronous Preset Width (Note 2)		10		12		15		17		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		8		15		17		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	10	2	12	2	15	2	17	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	10	2	12	2	15	2	17	ns
Input Register with Standard-Hold-Time Option											
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			12		14		17		20	ns
t_{SIR}	Input Register Setup Time		2		2		2		2		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note1)

Parameter Symbol	Parameter Description	-10		-12		-14		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HIR}	Input Register Hold Time	3		3		4		4		ns
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	3		3		4		4		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		4		4		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	8		9		12		15		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		14		16		19		22	ns
Input Register with Zero-Hold-Time Option										
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		18		20		23		26	ns
t_{SIR}^{I}	Input Register Setup Time	6		6		6		6		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		6		6		6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	13		16		16		16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	15		18		18		18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		20		22		25		27	ns
Power-Down Mode and Slow Slew Rate Option										
t_{LP}	Power-down mode delay adder. For macrocells in a power-down mode PAL block, this parameter must be added to: t_{PD}, t_{COA}, t_{SS}, t_{GOA}, t_{SLS}, t_{ICO}, t_{ICS}, t_{IGO}, t_{IGOL}, t_{IGSS}, t_{AR}, t_{ARR}, t_{AP}, t_{APR}, t_{EA}, t_{ER}, t_{PDL}, t_{SLLS}, t_{PDLL}		2.5		2.5		2.5		2.5	ns
t_{SLW}	Slow slew rate delay adder. For an output configured with slow slew rate option, this parameter must be added to: t_{PD}, t_{COA}, t_{COS}, t_{GOA}, t_{GOS}, t_{ICO}, t_{IGO}, t_{IGOL}, t_{AP}, t_{AR}, t_{PDL}, t_{PDLL}		2.5		2.5		2.5		2.5	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +4.5 V

DC Input Voltage . . . . . -0.5 V to 6.0 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -100 µA	V_{CC} - 0.2			V
			I_{OH} = -3.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2	V
			I_{OL} = 24 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		-0.3		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				-5	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				5	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				-5	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		-15		-160	mA
I_{CC}	Supply Current	All PAL Blocks low-power, V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 1 MHz, T_A = 25°C (Note 4)			60		mA
		All PAL Blocks full-power, V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 1 MHz, T_A = 25°C (Note 4)			105		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note1)

Parameter Symbol	Parameter Description				-10		-12		-14		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				3	10	3	12	3	14	3	18	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	4		5		8		10		ns
				T-type	5		6		9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				4		5		8		10		ns
t_{COA}	Product Term Clock to Output				4	12	4	14	4	18	4	20	ns
t_{WLA}	Product Term, Clock Width			LOW	5		8		9		10		ns
t_{WHA}				HIGH	5		8		9		10		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	62.5		52.6		38.5		33.3		MHz
				T-type	58.8		50.0		37		32.2		MHz
		Internal Feedback (f_{CNTA})		D-type	71.4		58.8		47.6		35.7		MHz
				T-type	66.7		55.6		45.4		34.4		MHz
		No Feedback (Note 3)	$1/(t_{WLA} + t_{WHA})$		100		62.5		55.6		50.0		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	6		7		10		12		ns
				T-type	7		8		11		13		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		0		ns
t_{COS}	Global Clock to Output				2	6.5	2	8	2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	5		6		6		7		ns
t_{WHS}				HIGH	5		6		6		7		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	80		66.7		50		41.7		MHz
				T-type	74.1		62.5		47.6		40.0		MHz
		Internal Feedback (f_{CNTS})		D-type	100		83.3		66.6		58.8		MHz
				T-type	90.9		76.9		62.5		55.5		MHz
		No Feedback (Note 3)	$1/(t_{WLS} + t_{WHS})$		100		83.3		88.3		71.4		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				4		5		8		10		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note1)

Parameter Symbol	Parameter Description		-10		-12		-14		-18		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{HLA}	Latch Data Hold Time Using Product Term Clock		4		5		8		10		ns
t_{GOA}	Product Term Gate to Output			13		16		19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		6		9		11		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		7		8		10		12		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		0		ns
t_{GOS}	Gate to Output			7.5		10		11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		6		6		7		ns
t_{ICO}	Input Register Clock to Combinatorial Output			15.5		18		20		22	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	8		9		15		17		
		T-type	9		10		16		18		
t_{WICL}	Input Register Clock Width	LOW	5		6		6		7		ns
t_{WICH}		HIGH	5		6		6		7		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	100		83.3		83.3		71.4		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			14		16		20		22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			16		18		22		24	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		4		14		16		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		9		16		18		ns
t_{WIGL}	Input Latch Gate Width LOW		5		6		6		7		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			14		16		20		22	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		10		12		15		17		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		8		10		15		17		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			14		16		20		22	ns
t_{APW}	Asynchronous Preset Width (Note 2)		10		12		15		17		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		8		15		17		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	10	2	12	2	15	2	17	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	10	2	12	2	15	2	17	ns
Input Register with Standard-Hold-Time Option											
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			12		14		17		20	ns
t_{SIR}	Input Register Setup Time		2		2		2		2		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note1)

Parameter Symbol	Parameter Description	-10		-12		-14		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HIR}	Input Register Hold Time	3		3		4		4		ns
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	3		3		4		4		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		4		4		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	8		9		12		15		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		14		16		19		22	ns
Input Register with Zero-Hold-Time Option										
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		18		20		23		26	ns
t_{SIR}^{I}	Input Register Setup Time	6		6		6		6		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		6		6		6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	13		16		16		16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	15		18		18		18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		20		22		25		27	ns
Power-Down Mode and Slow Slew Rate Option										
t_{LP}	Power-down mode delay adder. For macrocells in a power-down mode PAL block, this parameter must be added to: t_{PD}, t_{COA}, t_{SS}, t_{GOA}, t_{SLS}, t_{ICO}, t_{ICS}, t_{IGO}, t_{IGOL}, t_{IGSS}, t_{AR}, t_{ARR}, t_{AP}, t_{APR}, t_{EA}, t_{ER}, t_{PDL}, t_{SLLS}, t_{PDLL}		2.5		2.5		2.5		2.5	ns
t_{SLW}	Slow slew rate delay adder. For an output configured with slow slew rate option, this parameter must be added to: t_{PD}, t_{COA}, t_{COS}, t_{GOA}, t_{GOS}, t_{ICO}, t_{IGO}, t_{IGOL}, t_{AP}, t_{AR}, t_{PDL}, t_{PDLL}		2.5		2.5		2.5		2.5	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*