VANTIS

BEYOND PERFORMANCE

ADVANCE INFORMATION

MACH® 4A CPLD Family

High Performance EE CMOS Programmable Logic With Maximum Ease Of Use

DISTINCTIVE CHARACTERISTICS

Features

- **High-performance, EE CMOS 3.3-V CPLD Family**
- **Flexible architecture for rapid logic designs**
  - — Excellent First-Time-Fit™ and Refit
  - — SpeedLocking™ for guaranteed fixed timing
  - — Central, input and output switch matrices for 100% routability and 100% pin-out retention
- **High Speed**
  - — 5.0ns tPD Commercial and 7.5ns t_{PD} Industrial
  - — 175MHz f_{CNT}
- **32 to 256 macrocells; 32 to 384 Registers**
- **44 to 256 Pins in PLCC, PQFP, TQFP and BGA packages**
- **Advanced capabilities for easy system integration**
  - — 3.3-V JEDEC-compliant operations
  - — JTAG (IEEE 1149.1) complaint for boundary scan testing
  - — 3.3-V JTAG in-system programming
  - — PCI Compliant (-50/-55/-60/-65/-7/-10/-12 speed grades)
  - — Safe for mixed supply voltage system designs
  - — Programmable Pull-up or Bus-Friendly™ inputs and I/Os
  - — Hot-socketing
  - — Programmable security bit
- **Flexible architecture for a wide range of design styles**
  - — D/T registers and latches
  - — Synchronous or asynchronous mode
  - — Programmable polarity
  - — Reset/ preset swapping
  - — Individual output slew rate control
- **Advanced EE CMOS process provides high performance, cost effective solutions**
- **Supported by Vantis' software for rapid logic development**
  - — Supports HDL design methodologies with results optimized for Vantis
  - — Flexibility to adapt to user requirements
  - — Software partnerships that ensure customer success
- **Vantis and third-party hardware programming support**
  - — VantisPRO™ (formerly known as MACHPRO®) software for in-system programmability support on PCs and automated test equipment
  - — Programming support on all major programmers including Data I/O, BP Microsystems, Advin, and System General.

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Amendment/**0** Issue Date: **October 1998**

Table 1. MACH 4A Device Features

Feature	M4A-32/32	M4A-64/32	M4A-96/48	M4A-128/64	M4A-192/96	M4A-256/128
Macrocells	32	64	96	128	192	256
Maximum user I/O pins	32	32	48	64	96	128
t_{PD} (ns)	5.0	5.0	5.0	5.0	5.0	5.0
f_{CNT} (MHz)	175	175	175	175	175	175
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.0	4.0
t_{SS} (ns)	3.5	3.5	3.5	3.5	3.5	3.5
Static Power (mA)	TBD	TBD	TBD	TBD	TBD	TBD
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes

Table 2. MACH 4A Speed Grades

	Speed Grade[1]							
Device	-50[2]	-55	-60[2]	-65	-7	-10	-12	-14
M4A-32/32	C	C	C	C	C, I	C, I	C, I	I
M4A-64/32	C	C	C	C	C, I	C, I	C, I	I
M4A-96/48	C	C	C	C	C, I	C, I	C, I	I
M4A-128/64	C	C	C	C	C, I	C, I	C, I	I
M4A-192/96	C	C	C	C	C, I	C, I	C, I	I
M4A-256/128	C	C	C	C	C, I	C, I	C, I	I

1. C = Commercial
I = Industrial
2. This is Advance Information. Please contact a Vantis sales representative for details on availability.

Table 3. MACH 4A Package and I/O Options (Number of I/Os in table)

Package	M4A-32/32	M4A-64/32	M4A-96/48	M4A-128/64	M4A-192/96	M4A-256/128
44-pin PLCC	32	32				
44-pin TQFP	32	32				
48-pin TQFP	32	32				
100-pin TQFP			48	64		
100-pin PQFP				64		
144-pin TQFP					96	
208-pin PQFP						128
256-pin BGA						128

ABSOLUTE MAXIMUM RATINGS

MACH 4A

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +4.5 V

DC Input Voltage . . . . . –0.5 V to 6.0 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.50 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3 VDC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4			V
		I_{OH} = 0 mA, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL}			3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA

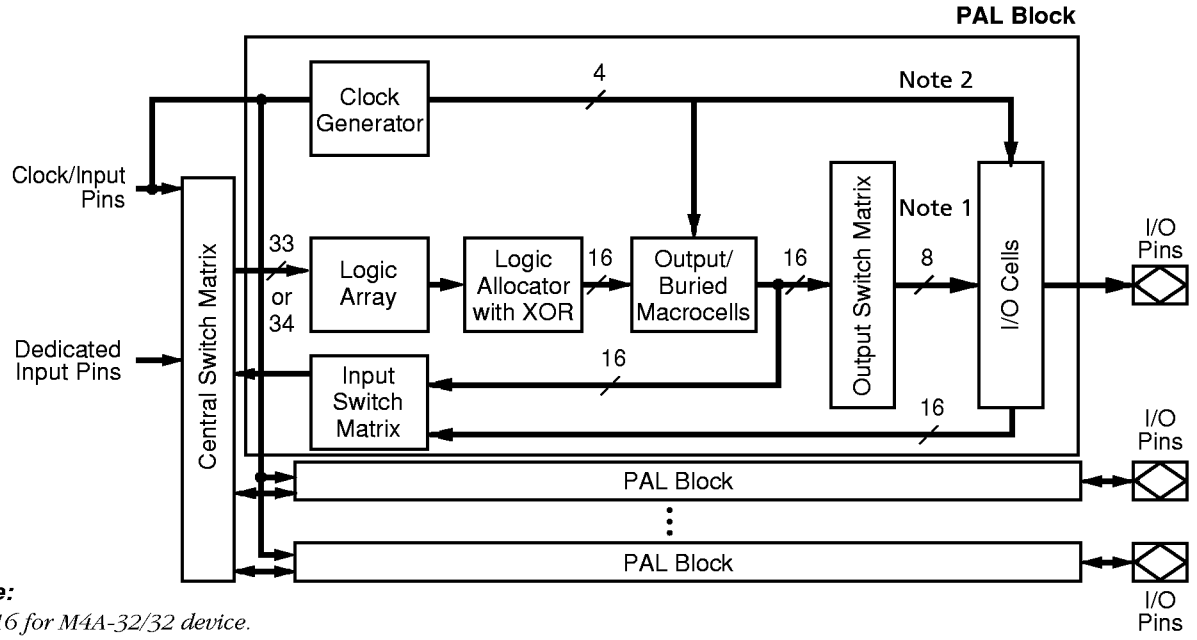
Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

FUNCTIONAL DESCRIPTION

The architecture of MACH 4A devices (Figure 1) consists of multiple optimized PAL® blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect schemes. In MACH 4A architecture, the macrocells have been decoupled from the product terms through the logic allocator; and the I/O pins have been decoupled from the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to place and route designs efficiently.



Note:

1. *16 for M4A-32/32 device.*
2. *Block clocks do not go to I/O cells in M4A-32/32*

M005-DS-1-001

Figure 1. MACH 4A Block Diagram and PAL Block Structure

MACH 4A TIMING MODEL

The Primary focus of the MACH 4A timing model is to accurately represent the timing in a MACH 4A device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between internal feedback and external feedback. A signal uses internal feedback when it goes into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF}, is defined as the time it takes to go from feedback through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an "i". By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A digram representing the modularized MACH 4A tiing model is shown in figure 15. Refer to the technical note entitled "MACH 4 Timing and High Speed Design" for a more detailed discussion about the timing parameters.

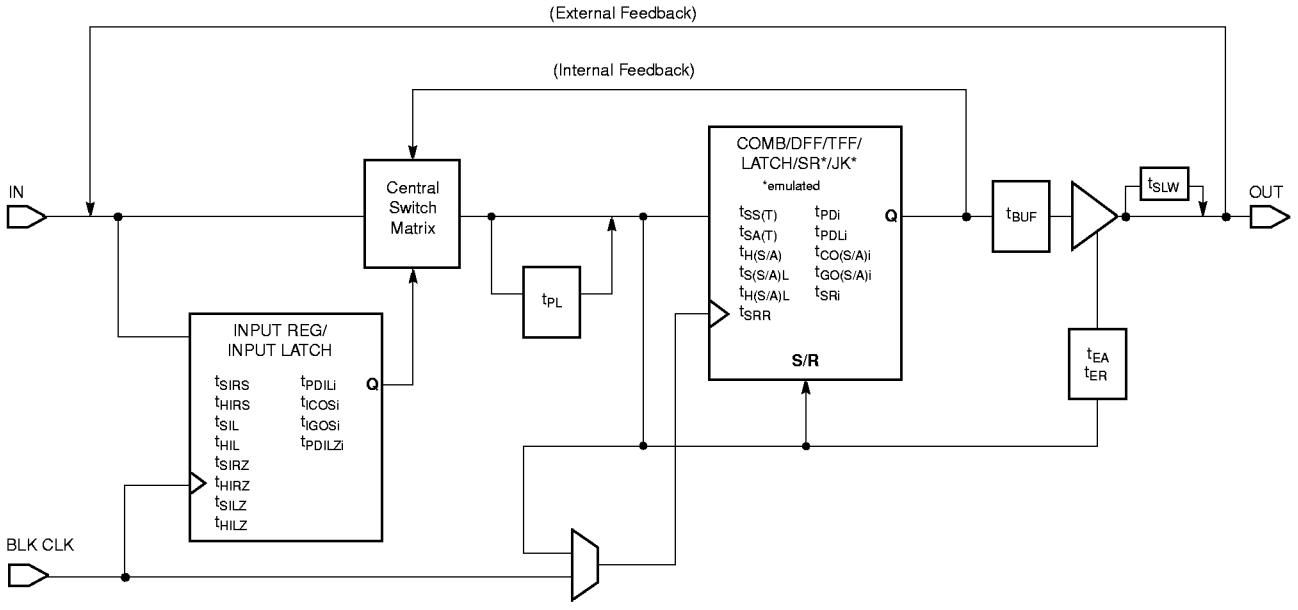


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Figure 2. MACH 4A Timing Model

Table 4. MACH 4A Timing Over Operating Ranges[1]

		-50		-55		-60		-65		-7		-10		-12		-14		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
Combinatorial Delay:																		
t_{PDi}	Internal combinatorial propagation delay		3.2		3.7		4.0		4.5		5.5		8.0		10.0		12.0	ns
t_{PD}	Combinatorial propagation delay		5.0		5.5		6.0		6.5		7.5		10.0		12.0		14.0	ns
Registered Delays:																		
t_{SS}	Synchronous clock setup time, D-type register	3.5		3.5		4.0		4.0		5.5		6.0		7.0		10.0		ns
t_{SST}	Synchronous clock setup time, T-type register	4.0		4.0		4.5		4.5		6.5		7.0		8.0		11.0		ns
t_{SA}	Asynchronous clock setup time, D-type register	2.5		2.5		3.0		3.0		3.5		4.0		5.0		8.0		ns
t_{SAT}	Asynchronous clock setup time, T-type register	3.0		3.0		3.5		3.5		4.5		5.0		6.0		9.0		ns
t_{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HA}	Asynchronous clock hold time	2.5		2.5		3.0		3.0		3.5		4.0		5.0		8.0		ns
t_{COSi}	Synchronous clock to internal output		2.2		2.2		2.5		2.5		3.5		4.5		6.0		8.0	ns
t_{COS}	Synchronous clock to output		4.0		4.0		4.5		4.5		5.5		6.5		8.0		10.0	ns
t_{COAi}	Asynchronous clock to internal output		4.7		4.7		5.0		5.0		7.5		10.0		12.0		16.0	ns
t_{COA}	Asynchronous clock to output		6.5		6.5		7.0		7.0		9.5		12.0		14.0		18.0	ns
Latched Delays:																		
t_{SSL}	Synchronous latch setup time	4.0		4.0		4.5		4.5		6.0		7.0		8.0		10.0		ns
t_{SAL}	Asynchronous latch setup time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t_{HSL}	Synchronous latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HAL}	Asynchronous latch hold time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t_{PDLi}	Transparent latch to internal output		5.2		5.2		6.0		6.0		8.0		10.0		12.0		15.0	ns
t_{PDL}	Propagation delay through transparent latch to output		7.0		7.0		8.0		8.0		10.0		12.0		14.0		17.0	ns
t_{GOSi}	Synchronous gate to internal output		2.7		2.7		3.0		3.0		4.0		5.5		8.0		9.0	ns
t_{GOS}	Synchronous gate to output		4.5		4.5		5.0		5.0		6.0		7.5		10.0		11.0	ns
t_{GOAi}	Asynchronous gate to internal output		5.7		5.7		6.0		6.0		9.0		11.0		14.0		17.0	ns
t_{GOA}	Asynchronous gate to output		7.5		7.5		8.0		8.0		11.0		13.0		16.0		19.0	ns
Input Register Delays:																		
t_{SIRS}	Input register setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
t_{HIRS}	Input register hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
t_{ICOSi}	Input register clock to internal feedback		3.0		3.0		3.0		3.0		3.5		4.5		6.0		6.0	ns
Input Latch Delays:																		
t_{SIL}	Input latch setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
t_{HIL}	Input latch hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
t_{IGOSi}	Input latch gate to internal feedback		3.5		3.5		4.0		4.0		4.0		4.0		4.0		5.0	ns

Table 4. MACH 4A Timing Over Operating Ranges[1] (Continued)

		-50		-55		-60		-65		-7		-10		-12		-14		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{PDILi}	Transparent input latch to internal feedback		1.5		1.5		1..5		1.5		2.0		2.0		2.0		2.0	ns
Input Register Delays with ZHT Option:																		
t_{SIRZ}	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HIRZ}	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
Input Latch Delays with ZHT Option:																		
t_{SILZ}	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HILZ}	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{PDILZi}	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0	ns
Output Delays:																		
t_{BUF}	Output buffer delay		1.8		1.8		2.0		2.0		2.0		2.0		2.0		2.0	ns
t_{SLW}	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{EA}	Output enable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
t_{ER}	Output disable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
Power Delay:																		
t_{PL}	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
Reset and Preset Delays:																		
t_{SRi}	Asynchronous reset or preset to internal register output		7.2		7.2		8.0		8.0		10.0		12.0		14.0		18.0	ns
t_{SR}	Asynchronous reset or preset to register output		9.0		9.2		10.0		10.0		12.0		14.0		16.0		20.0	ns
t_{SRR} [2]	Asynchronous reset and preset register recovery time	7.0		7.0		7.5		7.5		8.0		8.0		10.0		15.0		ns
t_{SRW} [2]	Asynchronous reset or preset width	7.0		7.0		8.0		8.0		10.0		10.0		12.0		15.0		ns
Clock/LE Width:																		
t_{WLS}	Global clock width low	2.0		2.0		2.5		2.5		3.0		5.0		6.0		6.0		ns
t_{WHS}	Global clock width high	2.0		2.0		2.5		2.5		3.0		5.0		6.0		6.0		ns
t_{WLA}	Product term clock width low	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t_{WHA}	Product term clock width high	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t_{GWS}	Global gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns
t_{GWA}	Product term gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		9.0		ns
t_{WIRL}	Input register clock width low	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t_{WIRH}	Input register clock width high	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t_{WIL}	Input latch gate width	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns

Table 4. MACH 4A Timing Over Operating Ranges[1] (Continued)

		-50		-55		-60		-65		-7		-10		-12		-14		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency:																		
f_{MAXS}	External feedback, D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	133.3		133.3		117.6		117.6		90.9		80.0		66.7		50.0		MHz
	External feedback, T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COS})$	125.0		125.0		111.1		111.1		83.3		74.1		62.5		47.6		MHz
	Internal feedback (f_{CNT}), D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	175.4		175.4		153.8		153.8		111.1		95.2		76.9		55.6		MHz
	Internal feedback (f_{CNT}), T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COSi})$	161.3		161.3		142.9		142.9		100.0		87.0		71.4		52.6		MHz
	No feedback, Min of $1/(t_{WLS} + t_{WHS})$, $1/(t_{SS} + t_{HS})$ or $1/(t_{SST} + t_{HS})$	250.0		250.0		200.0		200.0		153.8		100.0		83.3		83.3		MHz
f_{MAXA}	External feedback, D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	111.1		111.1		100.0		100.0		76.9		62.5		52.6		38.5		MHz
	External feedback, T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COA})$	105.3		105.3		95.2		95.2		71.4		58.8		50.0		37.0		MHz
	Internal feedback (f_{CNTA}), D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	138.9		138.9		125.0		125.0		90.9		71.4		58.8		41.7		MHz
	Internal feedback (f_{CNTA}), T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COAi})$	129.9		129.9		117.6		117.6		83.3		66.7		55.6		40.0		MHz
	No feedback, Min of $1/(t_{WLA} + t_{WHA})$, $1/(t_{SA} + t_{HA})$ or $1/(t_{SAT} + t_{HA})$	166.7		166.7		142.9		142.9		125.0		100.0		62.5		55.6		MHz
f_{MAXI}	Maximum input register frequency, Min of $1/(t_{WIRH} + t_{WIRL})$ or $1/(t_{SIRS} + t_{HIRS})$	166.7		166.7		142.9		142.9		125.0		100.0		83.3		83.3		MHz

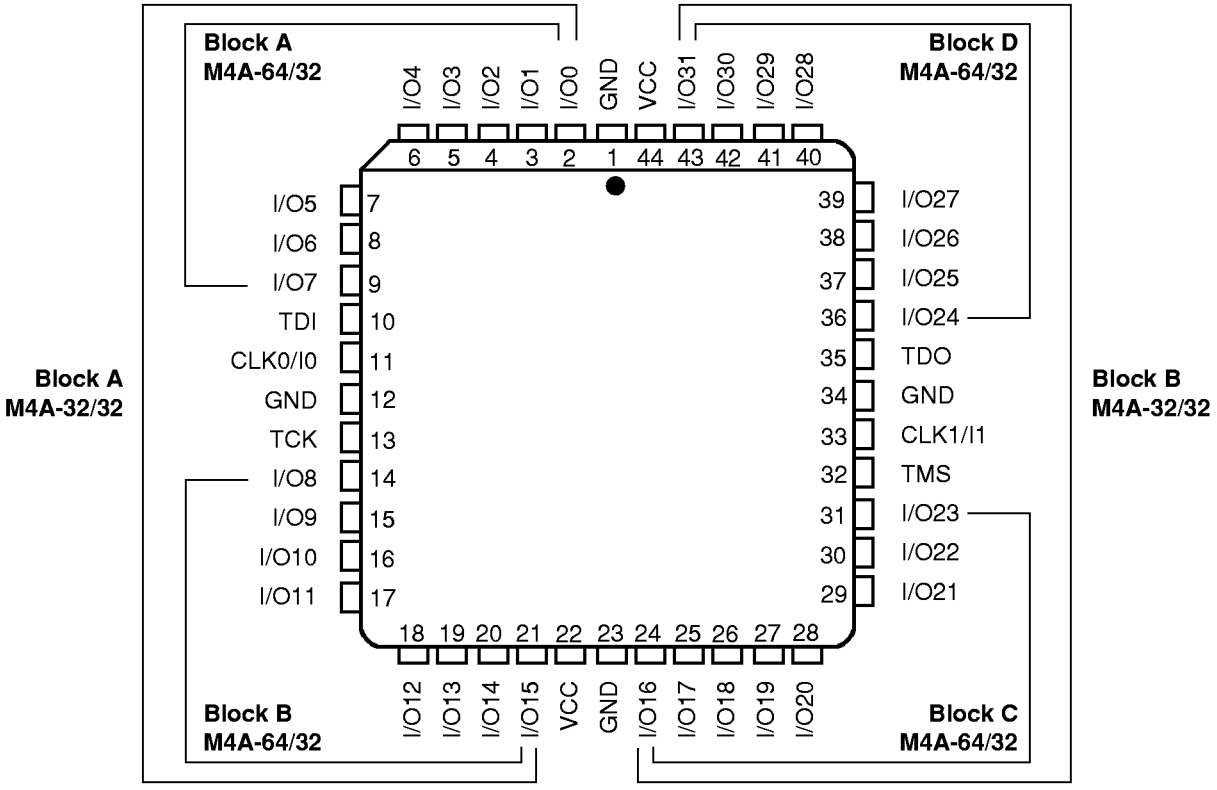
Note:

1. *See "Switching Test Circuits" in the General Information section of the Vantis 1999 Data Book.*
2. *These parameters are not tested, but they are evaluated at initial characterization.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

CONNECTION DIAGRAM (M4A-32/32 AND M4A-64/32)

Top View

44-Pin PLCC



Note:

1. Advance information for the M4A-32/32 and M4A-64/32

M005-DS-1-026

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

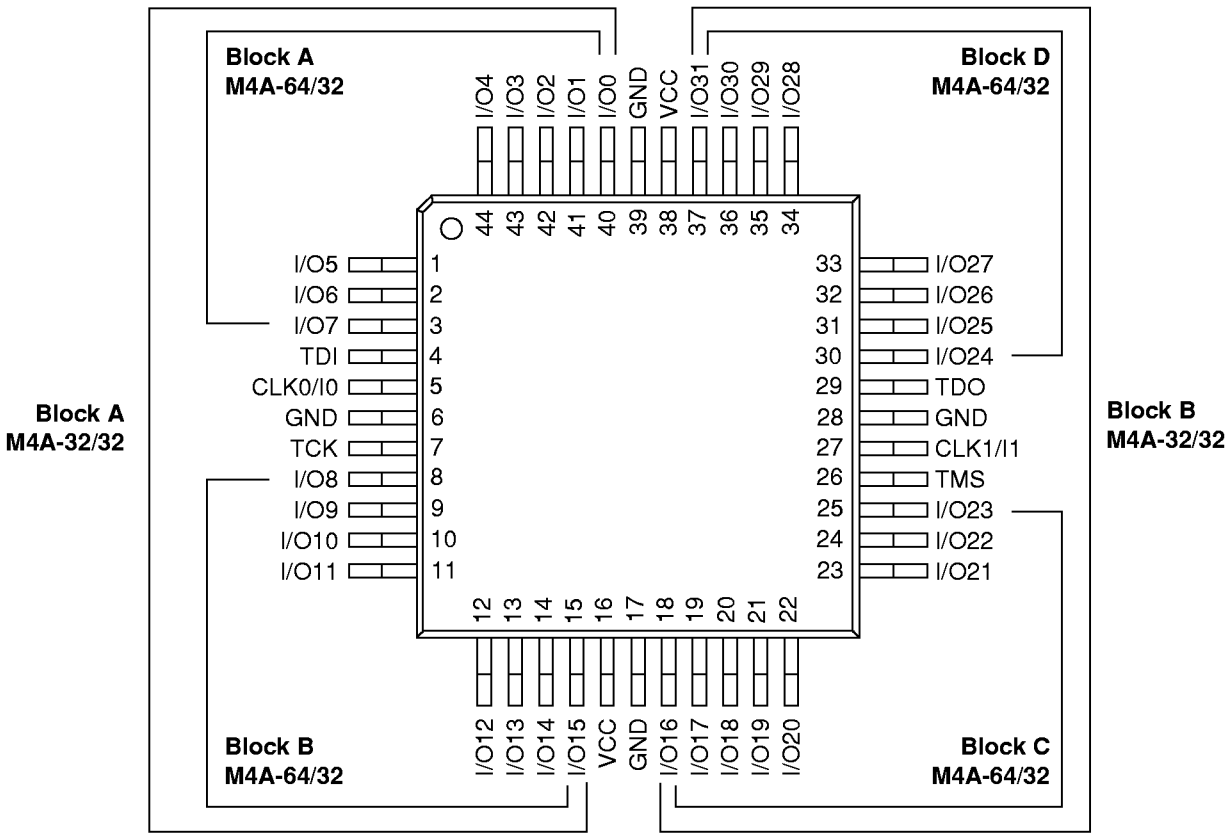
TMS = Test Mode Select

TDO = Test Data Out

CONNECTION DIAGRAM (M4A-32/32 AND M4A-64/32)

Top View

44-Pin TQFP



Note:

1. Advance information for the M4A-32/32 and M4A-64/32

M005-DS-1-027

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

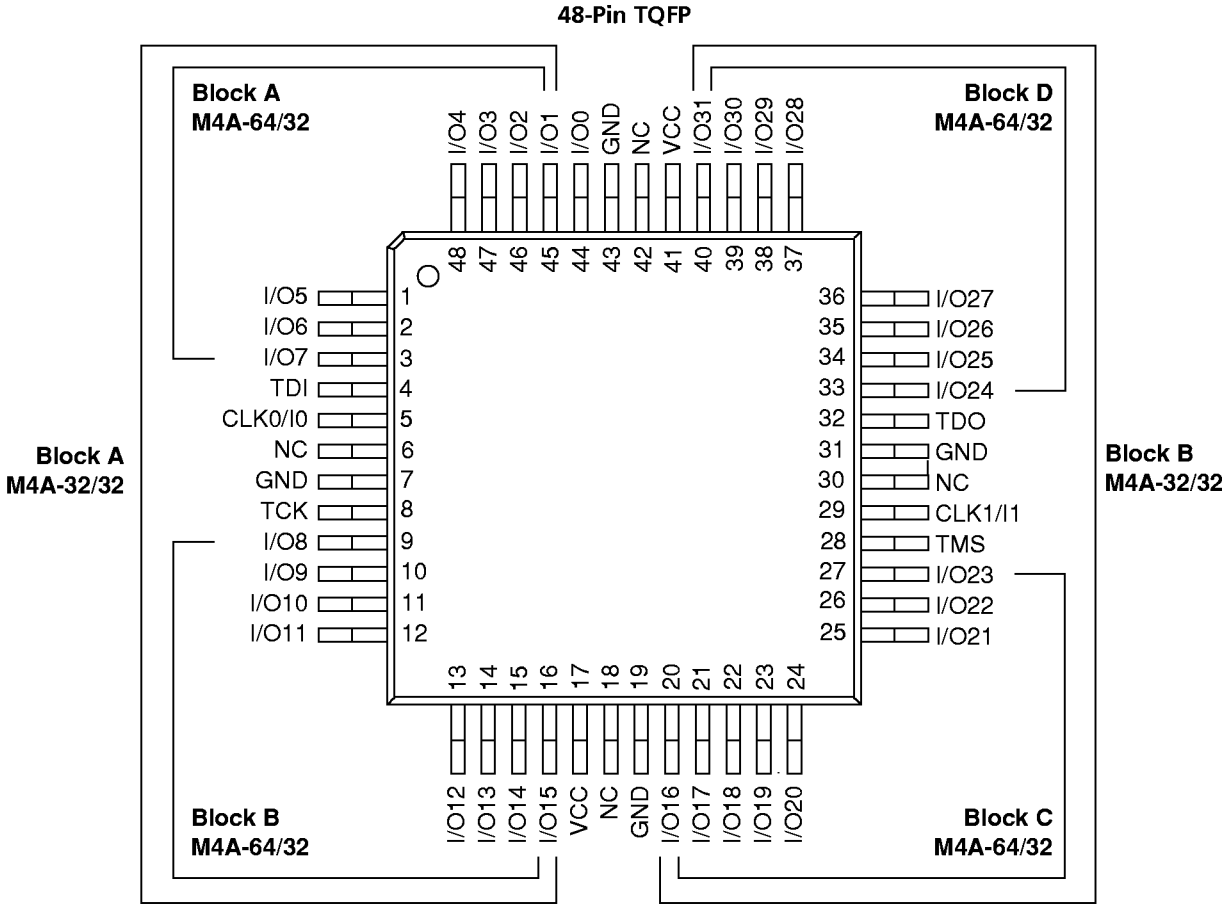
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

CONNECTION DIAGRAM (M4A-32/32 AND M4A-64/32)

Top View



Note:

1. Advance information for the M4A-32/32 and the M4A-64/32

M005-DS-1-028

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

NC = No Connect

TDI = Test Data In

TCK = Test Clock

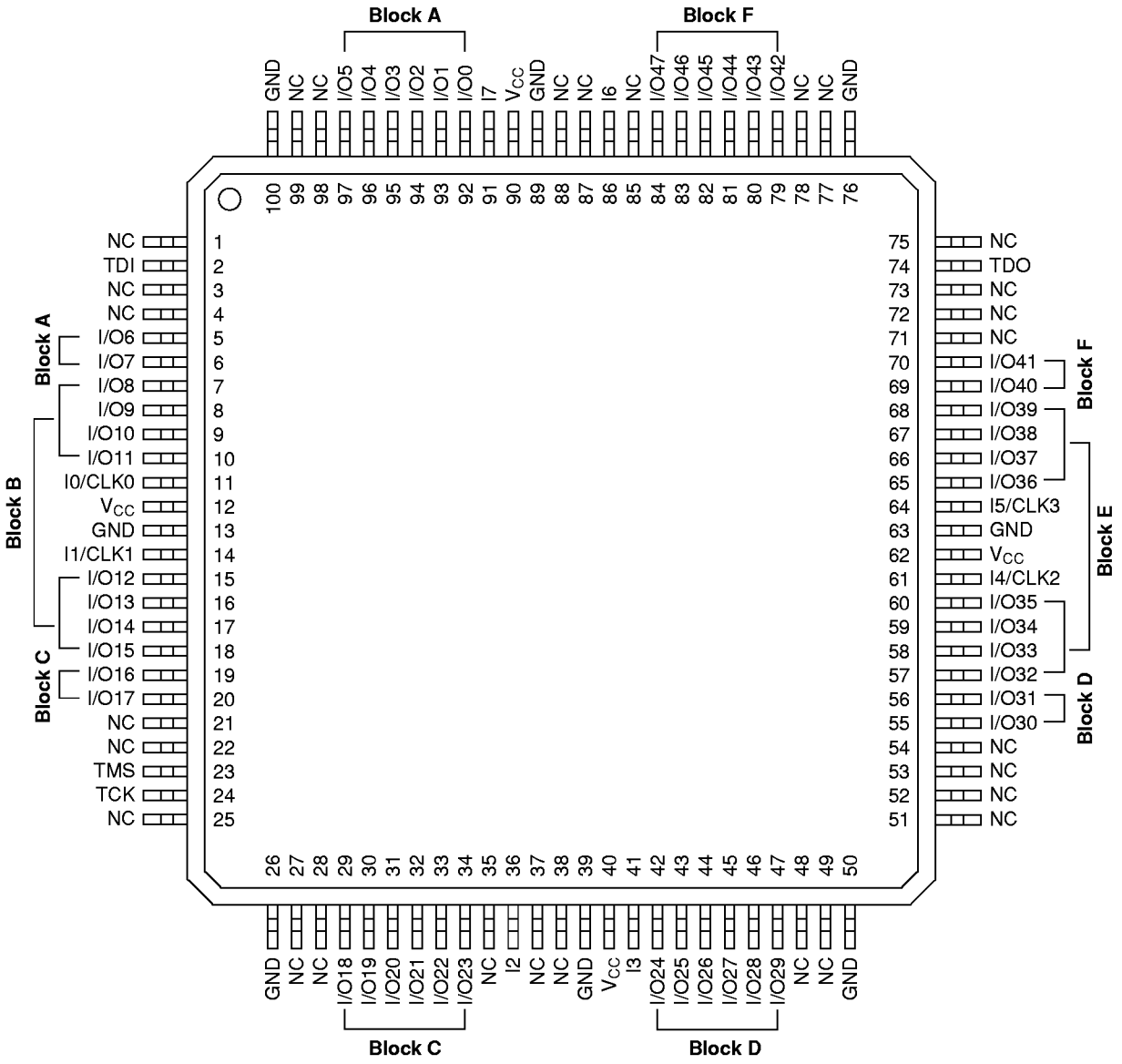
TMS = Test Mode Select

TDO = Test Data Out

CONNECTION DIAGRAM (M4A-96/48)

Top View

100-Pin TQFP



Note:

1. Advance information for the M4A-96/48

M005-DS-1-029

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

NC = No Connect

TDI = Test Data In

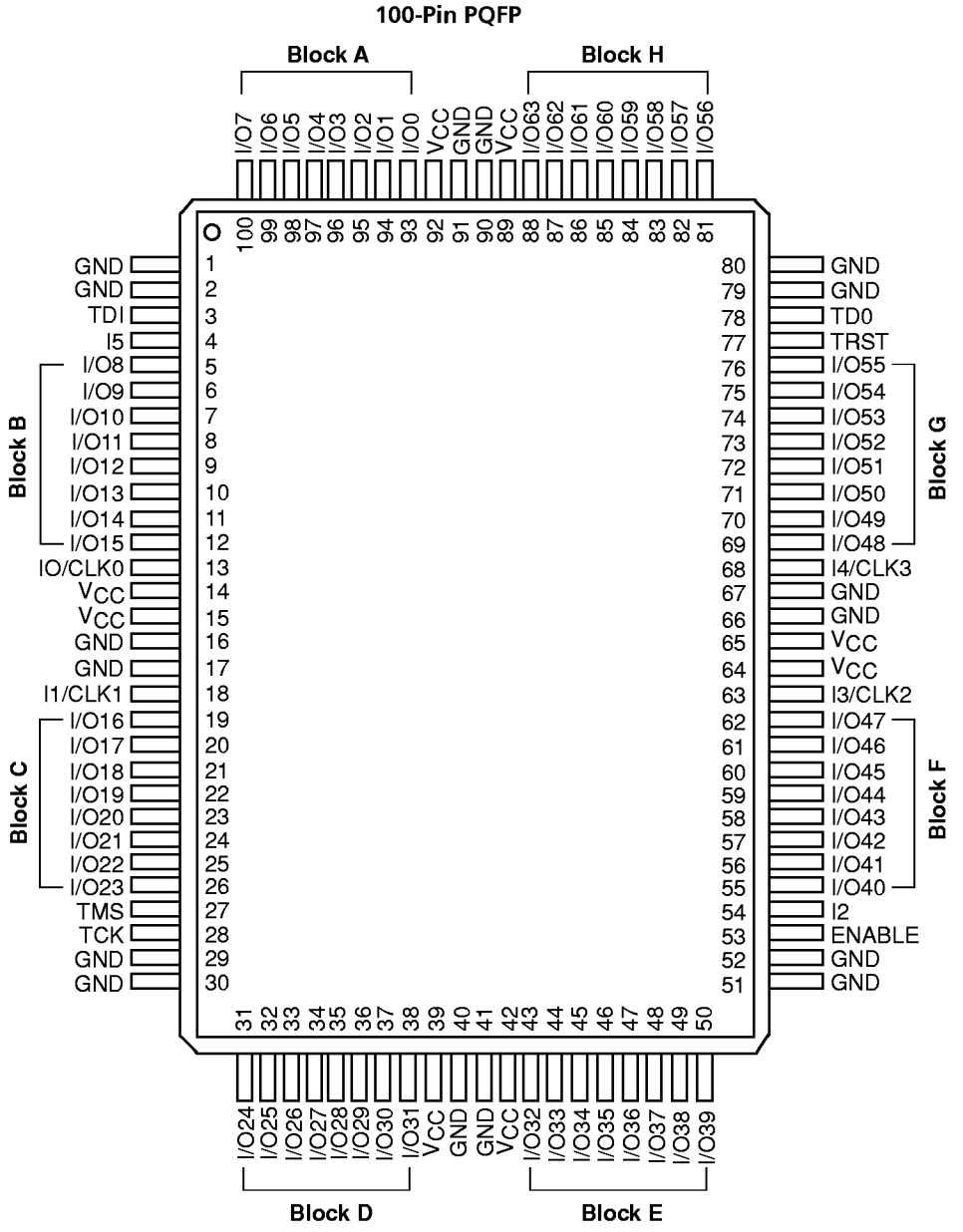
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

CONNECTION DIAGRAM (M4A-128/64)

Top View



M005-DS-1-064

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

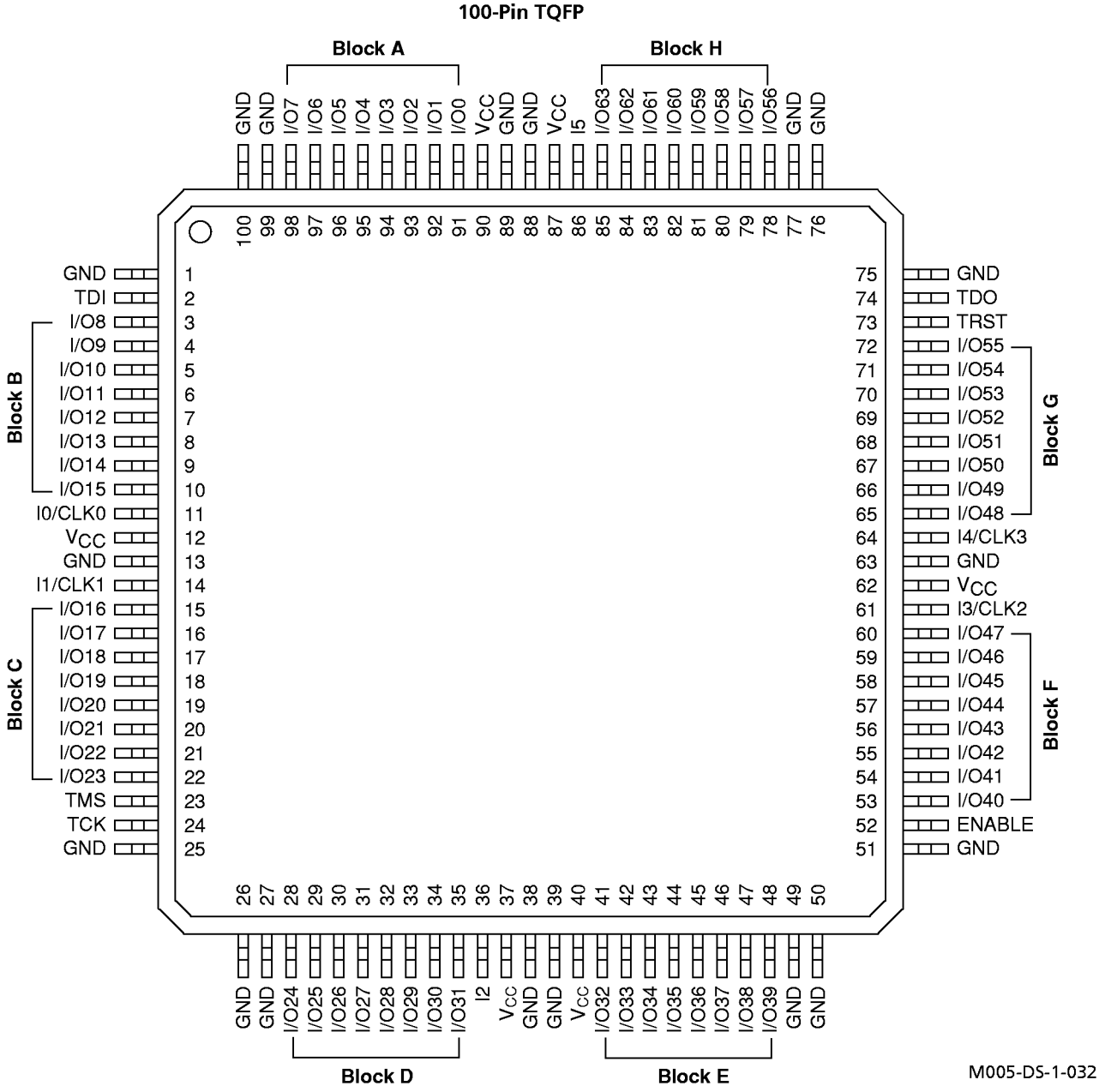
TDO = Test Data Out

TRST = Test Reset

Enable= Program

CONNECTION DIAGRAM (M4A-128/64)

Top View



M005-DS-1-032

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

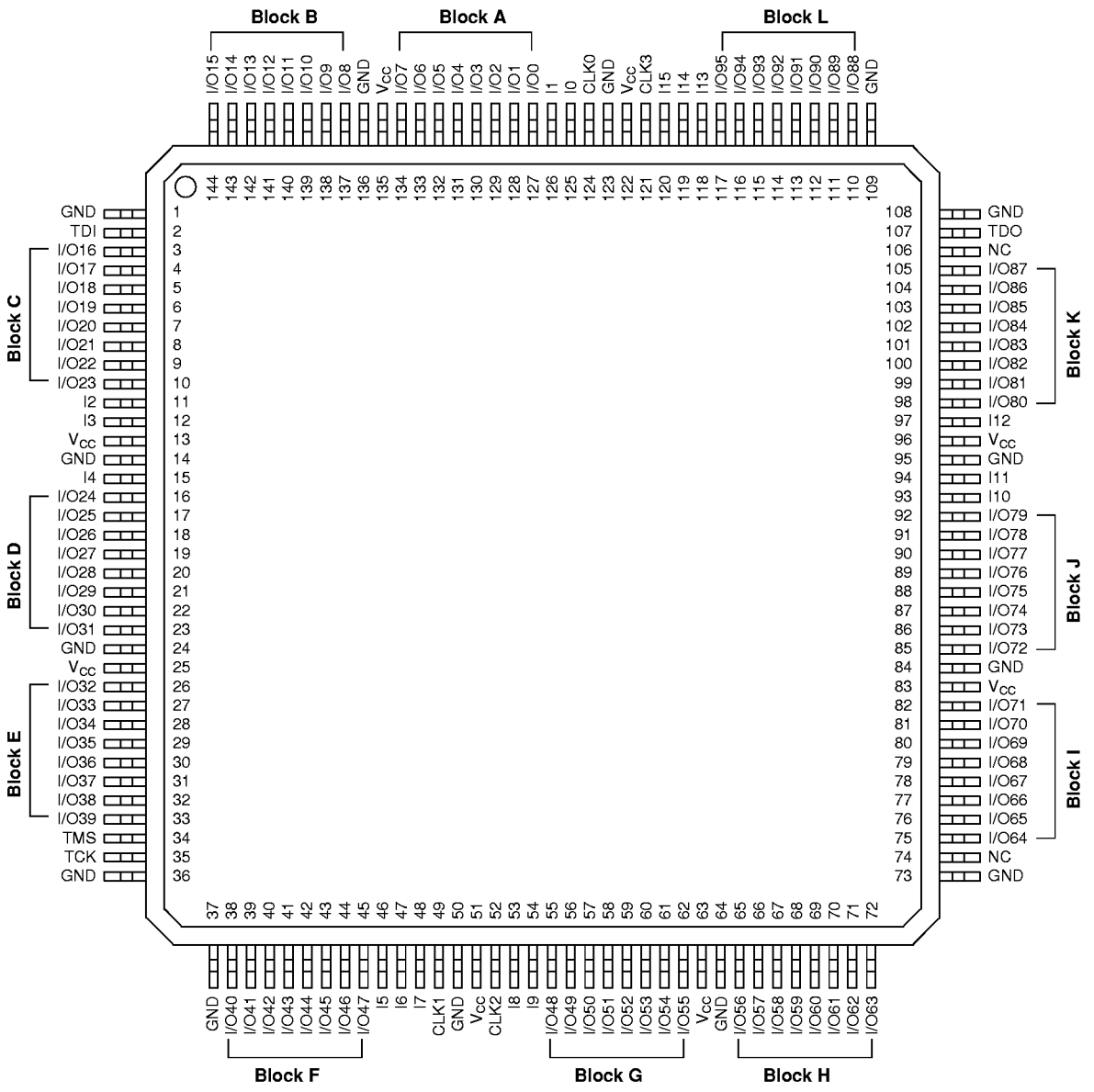
TRST = Test Reset

ENABLE= Program

CONNECTION DIAGRAM (M4A-192/96)

Top View

144-Pin TQFP



Note:

1. *Advance information for the M4A-192/96*

M005-DS-1-033

PIN DESIGNATIONS

CLK = Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

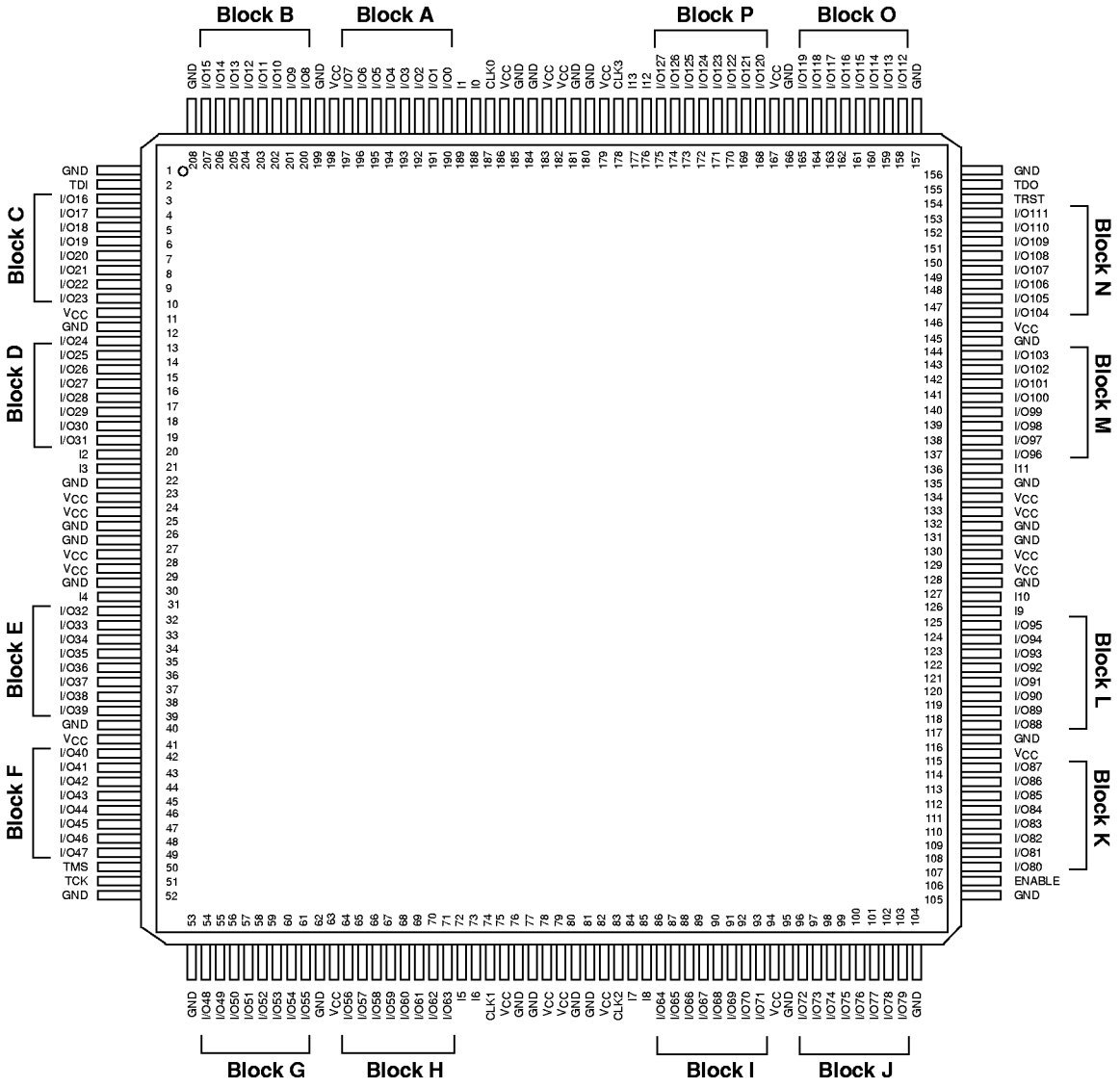
TMS = Test Mode Select

TDO = Test Data Out

CONNECTION DIAGRAM (M4A-256/128)

Top View

208-Pin PQFP



Note:

1. Advance information for the M4A-256/128

M005-DS-1-034

PIN DESIGNATIONS

CLK = Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

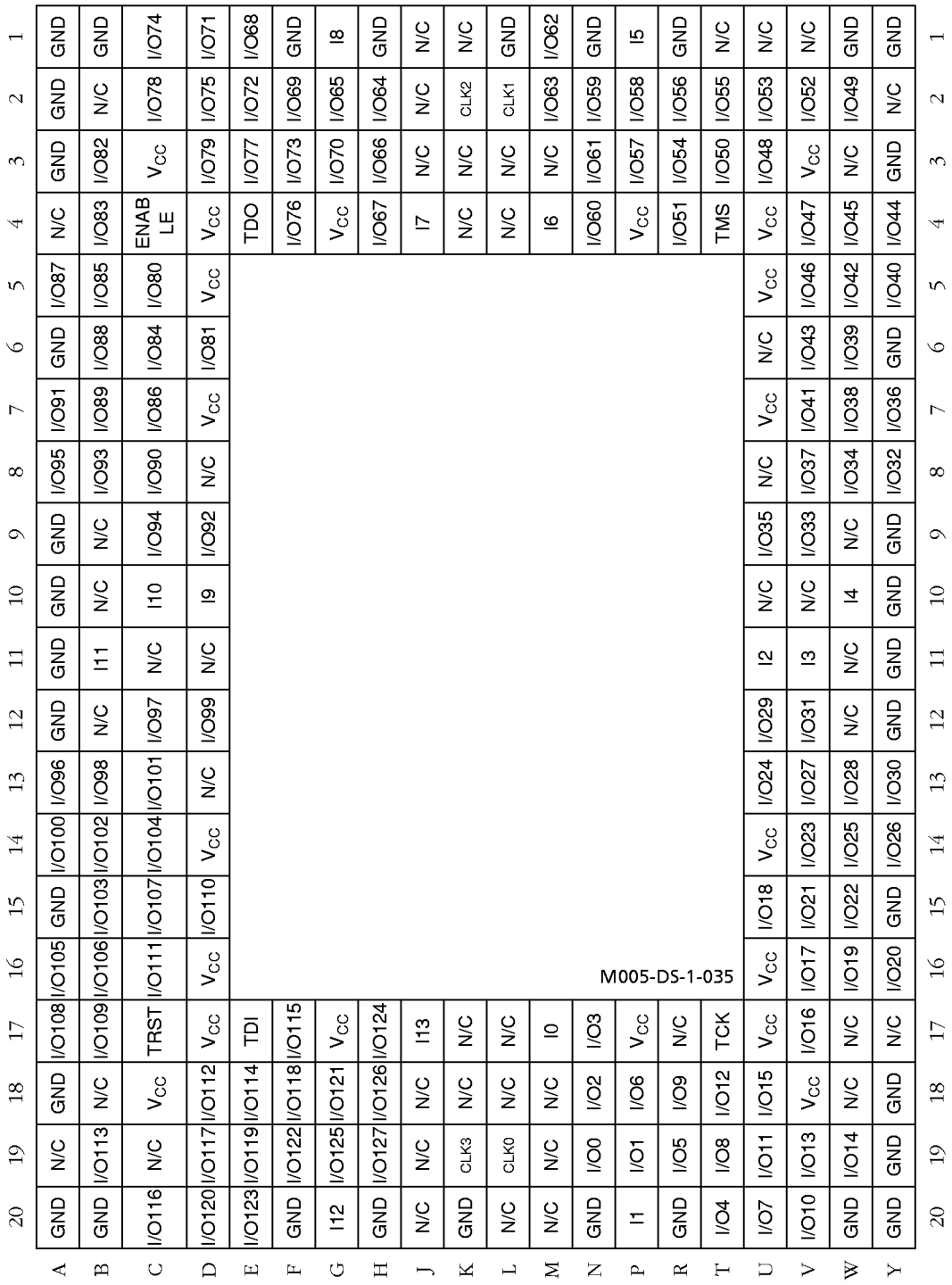
TRST = Test Reset

ENABLE= Program

CONNECTION DIAGRAM (M4A-256/128)

Bottom View

256-Pin BGA



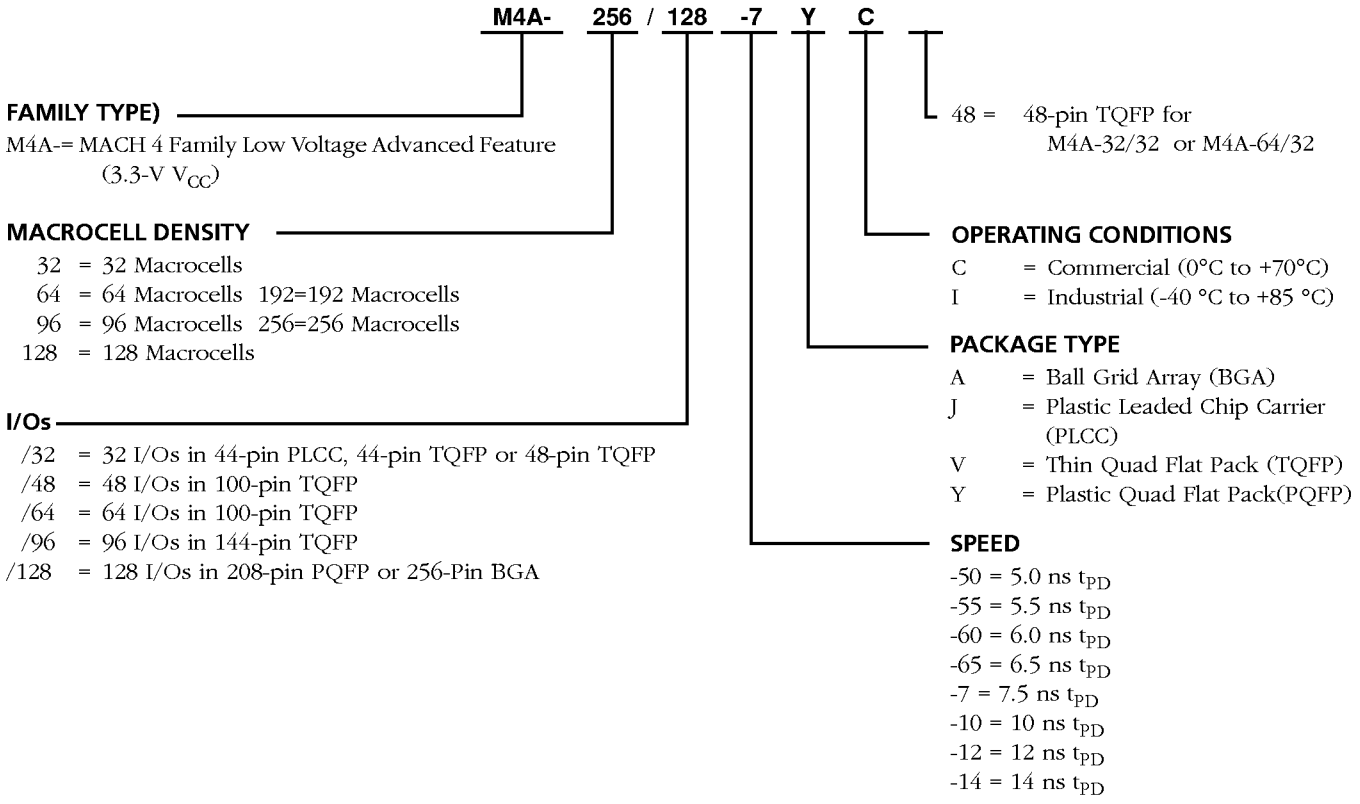
Note:

Advance information for the M4A-256/128

PRODUCT ORDERING INFORMATION

MACH 4A Commercial and Industrial

Vantis programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
M4A-32/32	-50, -55, -60, -65 -7, -10, -12	JC, VC, VC48
M4A-64/32		JC, VC, VC48
M4A-96/48		VC
M4A-128/64		YC, VC
M4A-192/96		VC
M4A-256/128		YC, AC

All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is one speed grade slower, i.e., M4A-128/64 - 7VC - 10VI

Valid Combinations		
M4A-32/32	-7, -10, -12, -14	JI, VI, VI48
M4A-64/32		JI, VI, VI48
M4A-96/48		VI
M4A-128/64		YI, VI
M4A-192/96		VI
M4A-256/128		YI, AI

Valid Combinations

Refer to the menu pages or consult the local Vantis sales office to confirm the availability of specific valid combinations.