LT8918L --- Product Brief

Dual-Port LVDS to MIPI DSI/CSI-2 Bridge

Features

- **Single/Dual-Port LVDS Receiver**
  - Compatible with VESA and JEIDA standard
  - 1~2 configurable port
  - 1 clock lane and 1~5 data lanes per port
  - Data lane and polarity swapping
  - Support Maximum Data Rate 1.2Gb/s/lane
  - Resolution up to 1080P 60Hz for dual-port mode
  - Input color depth supports 6-bit, 8-bit and10-bit
  - Support input De-SSC (30kHz +/- 5%)
- **Single-Port MIPI DSI Transmitter**
  - Compliant with DCS1.02, D-PHY1.1 & DSI1.02
  - 1 Clock Lane and 1~4 Configurable Data Lanes
  - 80Mb/s~1.5Gb/s per Data Lane
  - Resolution Up to 1080P 60Hz
  - Data Lane and Polarity Swapping
  - Both Non-Burst and Burst Video Mode Supported
  - Command Mode through Lane-0 Supported
  - Support RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2, 24-bit YCbCr 4:2:2 Video Format
- **Single-Port MIPI CSI-2 Transmitter**
  - Compliant with D-PHY1.1 & CSI-2 1.0
  - 1 Clock Lane and 1~4 Configurable Data Lanes
  - 80Mb/s~1.5Gb/s per Data Lane
  - Resolution Up to 1080P 60Hz
  - Data Lane and Polarity Swapping
  - Support RGB565, RGB666, RGB888, 8-bit YUV422 Video Format
- **Miscellaneous**
  - 1.8V Single Supply Power
  - Support 100KHz and 400KHz I2C slave
  - Support SPI slave
  - External 25MHz Crystal Reference Clock
  - Temperature Range: -40^{0}C ~ +85^{0}C
  - Packaged in QFN64 7.5mm x 7.5mm and BGA81 5mm x 5mm.

Description

The Lontium LT8918L is a high performance Dual-Port LVDS to MIPIDSI/CSI-2 bridge chip between AP and mobile display panel or camera .

LT8918L can be configured as single-port or dual-port with optional De-SSC function. The bridge deserializes input LVDS data, decodes packets and converts the formatted video data stream to MIPIDSI/CSI-2 transmitter output.

For MIPI DSI/CSI-2 output, LT8918L features a single port MIPI DSI or CSI-2 transmitter with 1 high-speed clock lane and 1~4 configurable high-speed data lanes operating at maximum 1.5Gb/s/lane, which can support a total bandwidth of up to 6Gb/s. LT8918L supports both Non-Burst and Burst DSI video data transferring, as well as Command Mode through Lane-0.

The LT8918L is fabricated in advanced CMOS process and implemented in a small outline 7.5mm x 7.5mm QFN64 package. This package is RoHS compliant and specified to operate from -40°C to +85°C.

Application

- Mobile systems
- Cellular handsets
- Digital video cameras
- Digital still cameras
- Tablet PC, Notebook PC
- Car Display and Camera System

Block Diagram

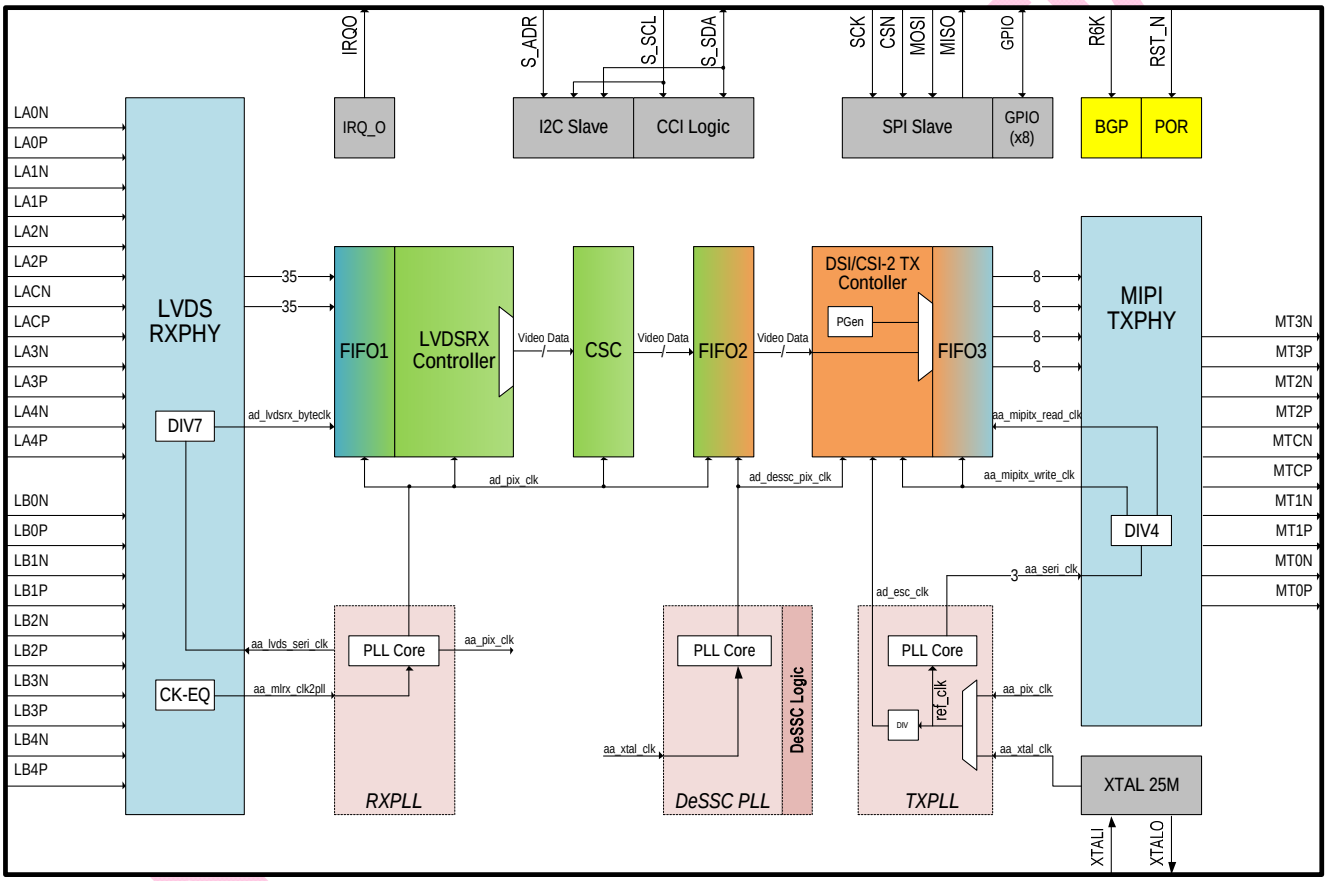
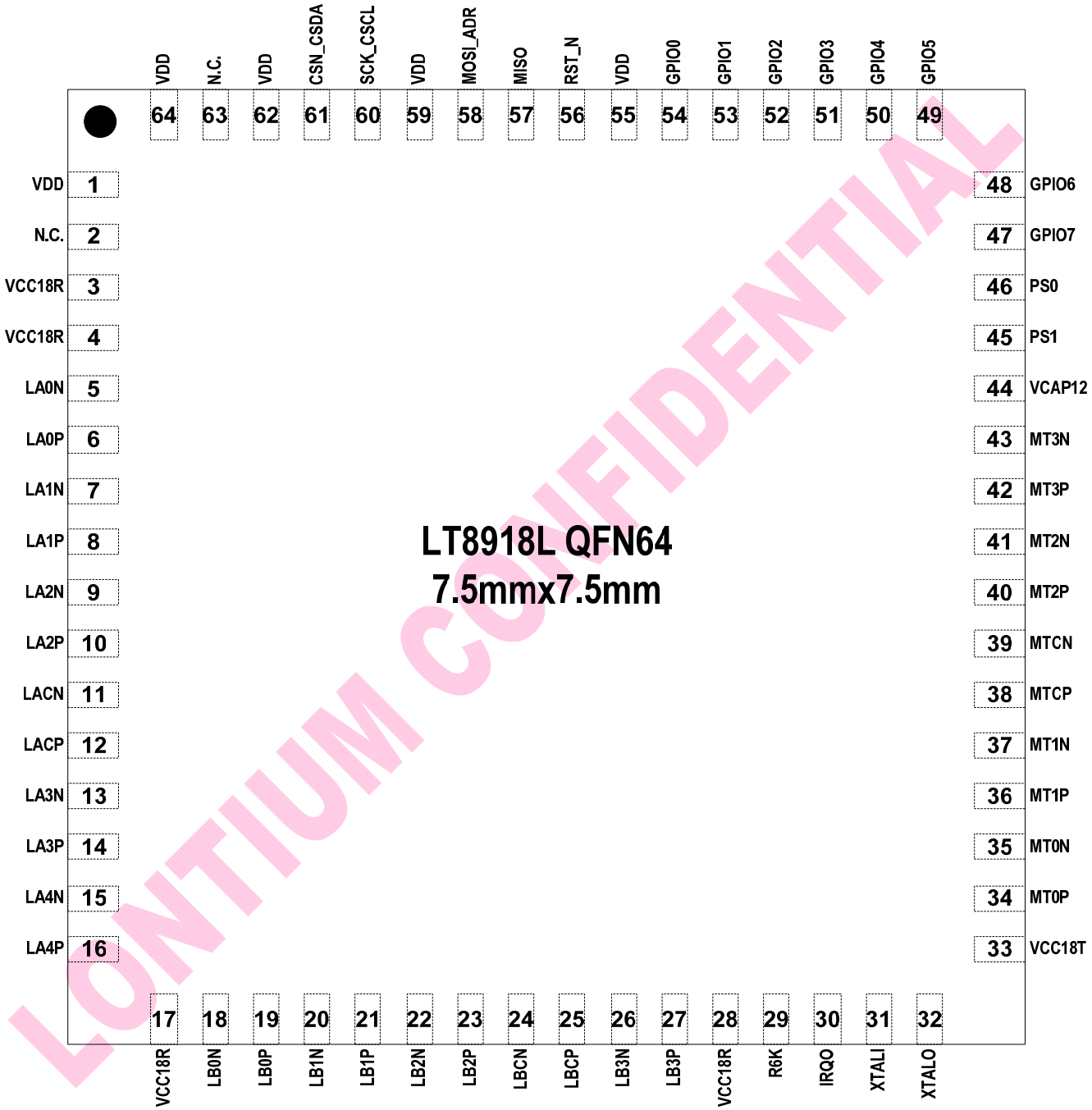


Fig1 Dual-Port LVDS to MIPI DSI/CSI-2 Functional Diagrams

Pin Diagram



Pin Definition

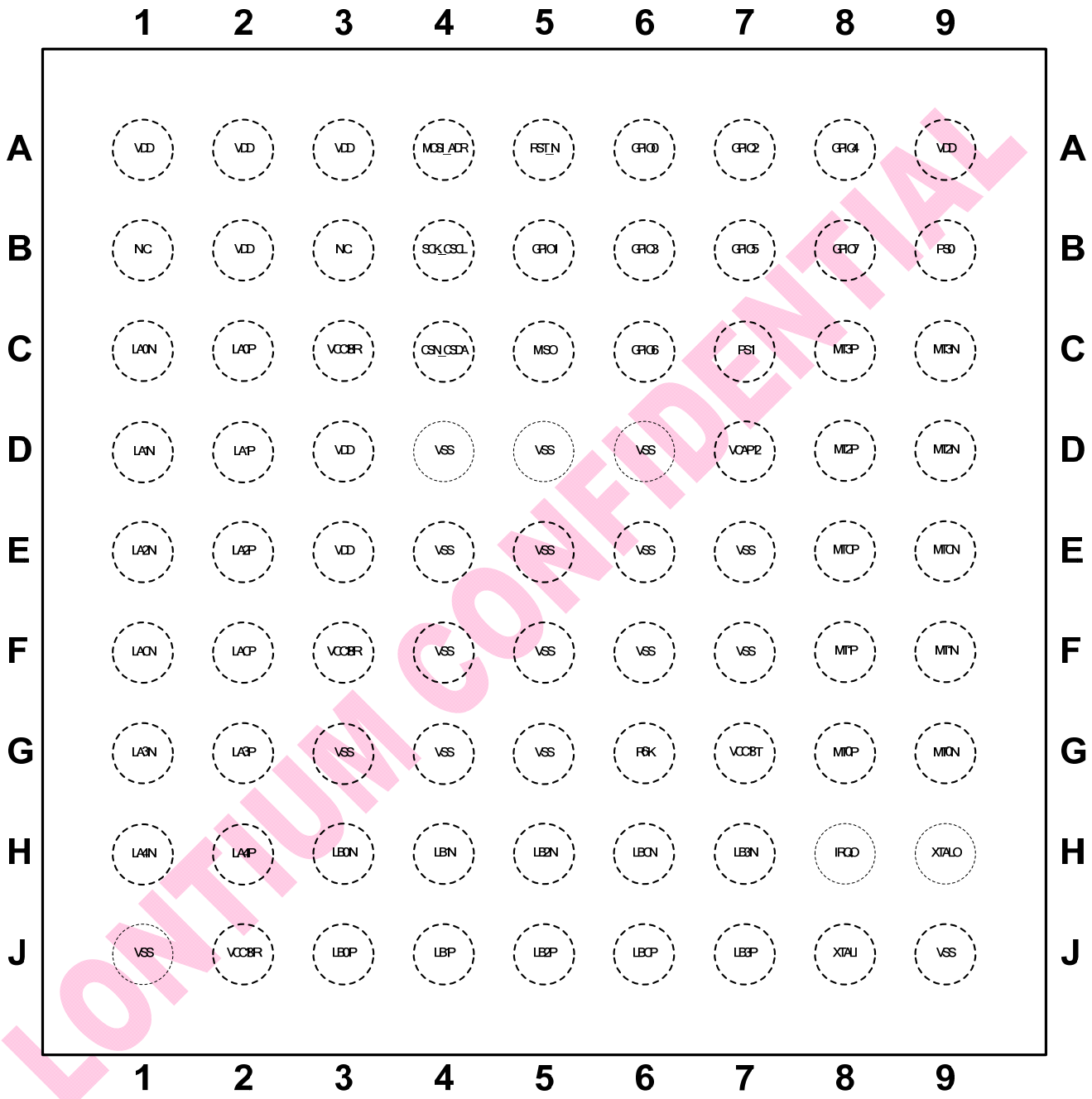
Pin No.	Pin Name	Pin Description
1	VDD	Digital core 1.8V Power 1.8V power for digital core
2	N.C.	No Connect. Floating
3	VCC18R	Analog 1.8V Power 1.8V power for LVDS Receiver Port-1
4	VCC18R	Analog 1.8V Power 1.8V power for LVDS Receiver Port-1
5	LA0N	LVDS Data Lane-0 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
6	LA0P	LVDS Data Port-A Lane-0 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
7	LA1N	LVDS Data Port-A Lane-1 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
8	LA1P	LVDS Data Port-A Lane-1 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
9	LA2N	LVDS Data Port-A Lane-2 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
10	LA2P	LVDS Data Port-A Lane-2 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
11	LACN	LVDS Data Port-A Lane-C Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
12	LACP	LVDS Data Port-A Lane-C Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
13	LA3N	LVDS Data Port-A Lane-3 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
14	LA3P	LVDS Data Port-A Lane-3 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
15	LA4N	LVDS Data Port-A Lane-4 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
16	LA4P	LVDS Data Port-A Lane-4 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
17	VCC18R	Analog 1.8V Power 1.8V power for RXPLL
18	LB0N	LVDS Data Port-B Lane-0 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
19	LB0P	LVDS Data Port-B Lane-0 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
20	LB1N	LVDS Data Port-B Lane-1 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.

Pin No.	Pin Name	Pin Description
21	LB1P	LVDS Data Port-B Lane-1 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
22	LB2N	LVDS Data Port-B Lane-2 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
23	LB2P	LVDS Data Port-B Lane-2 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
24	LBCN	LVDS Data Port-B Lane-C Negative Input (8-bit Mode) LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s. LVDS Data Port-B Lane-3 Negative Input (10-bit Mode) LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
25	LBCP	LVDS Data Port-B Lane-C Positive Input (8-bit Mode) LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s. LVDS Data Port-B Lane-3 Positive Input (10-bit Mode) LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
26	LB3N	LVDS Data Port-B Lane-3 Negative Input (8-bit Mode) LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s. LVDS Data Port-B Lane-4 Negative Input (10-bit Mode) LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
27	LB3P	LVDS Data Port-B Lane-3 Positive Input (8-bit Mode) LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s. LVDS Data Port-B Lane-4 Positive Input (10-bit Mode) LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
28	VCC18R	Analog 1.8V Power 1.8V power for LVDS Receiver Port-2 and Bandgap
29	R6K	BandGap External Resistor External 6K resistor for setting internal reference current.
30	IRQO	Interrupt Request Output In default, this pin is configured as interrupt request (IRQ) output. Analog Test Signal Output When this pin is configured as Hi-Z, it serves as analog test signal output.
31	XTALI	Crystal Clock Input A crystal oscillator should be attached between this pin and XTALO. However, a CMOS 1.8V compatible clock signal can also be connected to this pin as reference clock of LT8918L
32	XTALO	Crystal Clock Output A crystal oscillator should be attached between this pin and XTALI. If XTALI is used as reference clock input, this pin must be floating.
33	VCC18T	Analog 1.8V Power 1.8V power for MIPI Transmitter
34	MT0P	MIPI Data Lane-0 Positive Output MIPITX Positive output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s.
35	MT0N	MIPI Data Lane-0 Negative Output MIPITX Negative output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s.

Pin No.	Pin Name	Pin Description
36	MT1P	MIPI Data Lane-1 Positive Output MIPITX Positive output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s.
37	MT1N	MIPI Data Lane-1 Negative Output MIPITX Negative output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s.
38	MTCP	MIPI Data Lane-C Positive Output MIPITX Positive output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s.
39	MTCN	MIPI Data Lane-C Negative Output MIPITX Negative output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s.
40	MT2P	MIPI Data Lane-2 Positive Output MIPITX Positive output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s.
41	MT2N	MIPI Data Lane-2 Negative Output MIPITX Negative output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s.
42	MT3P	MIPI Data Lane-3 Positive Output MIPITX Positive output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s.
43	MT3N	MIPI Data Lane-3 Negative Output MIPITX Negative output of Bi-directional polarity swappable differential pairs up to 2.5Gb/s.
44	VCAP12	Internal 1.8V-to-1.2V LDO output Connect this pin to a bypass capacitor no less than 1uF. When configured as using internal bypass capacitor, please put this pin floating.
45	PS1	SPI Mode Select Input Bit-1 SPI mode select input bit-1.
46	PS0	SPI Mode Select Input Bit-0 SPI mode select input bit-0.
47	GPIO7	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin.
48	GPIO6	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin.
49	GPIO5	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin.
50	GPIO4	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin.
51	GPIO3	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin.
52	GPIO2	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin.

Pin No.	Pin Name	Pin Description
53	GPIO1	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin.
54	GPIO0	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please floating this pin.
55	VDD	Digital core 1.8V Power 1.8V power for digital core
56	RST_N	Hardware Reset Input Chip reset signal. Active LOW.
57	MISO	SPI Slave Serial Data Output It serves as the serial port data output for SPI slave register access.
58	MOSI_ADR	SPI Slave Serial Data Input It serves as the serial port data input for SPI slave register access. I2C Device Address Select It serves as the serial port address select for I2C slave register access.
59	VDD	Digital core 1.8V Power 1.8V power for digital core
60	SCK_CSCL	SPI Slave Serial Clock Input It serves as the serial port clock input for SPI slave register access. I2C Serial Clock Input It serves as the serial port data clock slave for I2C slave register access. Supports 1.8/3.3V CMOS logic.
61	CSN_CSDA	SPI Slave Select It serves as the chip select input for SPI slave register access. Active LOW. I2C Serial Data Input/Output It serves as the serial port data IO for I2C slave register access. Supports 1.8/3.3V CMOS logic.
62	VDD	Digital core 1.8V Power 1.8V power for digital core
63	N.C.	No Connect. Floating
64	VDD	Digital core 1.8V Power 1.8V power for digital core
65	#EPAD	EPAD

BGA81 Ball Map



Ball Definition

Ball No.	Ball Name	Ball Description
D4, D5, D6, E4, E5, E6, E7, F4, F5, F6, F7, G3, G4, G5, J1, J9	VSS	Chip Ground 1.8V ground for LT8918
B1, B3	N.C.	No Connect. Floating
A1, A2, A3, A9, B2, D3, E3	VDD	Digital core 1.8V Power 1.8V power for digital core
C3, F3, J2	VCC18R	Analog 1.8V Power 1.8V power for rxphy and rxpll
G7	VCC18T	Analog 1.8V Power 1.8V power for mipitx, txpll, and dessc pll
C9	MT3N	MIPI D-PHY Data Lane-3 Negative Input MIPITX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
C8	MT3P	MIPI D-PHY Data Lane-3 Positive Input MIPITX Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
D9	MT2N	MIPI D-PHY Data Lane-2 Negative Input MIPITX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
D8	MT2P	MIPI D-PHY Data Lane-2 Positive Input MIPITX Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
E9	MTCN	MIPI D-PHY Clock Lane Negative Input MIPITX Negative input of DDR clock differential pairs up to 1.25GHz in quadrature phase with data signals
E8	MTCP	MIPI D-PHY Clock Lane Positive Input MIPITX Positive input of DDR clock differential pairs up to 1.25GHz in quadrature phase with data signals
F9	MT1N	MIPI D-PHY Data Lane-1 Negative Input MIPITX Negative input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
F8	MT1P	MIPI D-PHY Data Lane-1 Positive Input MIPITX Positive input of Uni-directional polarity swappable differential pairs up to 1.5Gb/s.
G9	MT0N	MIPI D-PHY Data Lane-0 Negative Input MIPITX Negative input of Bi-directional polarity swappable differential pairs up to 1.5Gb/s.
G8	MT0P	MIPI D-PHY Data Lane-0 Positive Input MIPITX Positive input of Bi-directional polarity swappable differential pairs up to 1.5Gb/s.
G6	R6K	BandGap External Resistor External 6K resistor for setting internal reference current.

Ball No.	Ball Name	Ball Description
J8	XTALI	Crystal Clock Input A crystal oscillator should be attached between this pin and XTALO. However, a CMOS 1.8V compatible clock signal can also be connected to this pin as reference clock of LT8918L.
H9	XTALO	Crystal Clock Output A crystal oscillator should be attached between this pin and XTALI. If XTALI is used as reference clock input, this pin must be floating.
H8	IRQO	Interrupt Request Output In default, this pin is configured as interrupt request (IRQ) output. Analog Test Signal Output This pin can also be configured as analog debug pin.
D7	VCAP12	Internal 1.2V LDO Output 1.2V LDO output for MIPITX LPTX. Based on configuration, a bypass capacitor might be required to connect to this pin.
C1	LA0N	LVDS Data Lane-0 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
C2	LA0P	LVDS Data Port-A Lane-0 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
D1	LA1N	LVDS Data Port-A Lane-1 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
D2	LA1P	LVDS Data Port-A Lane-1 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
E1	LA2N	LVDS Data Port-A Lane-2 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
E2	LA2P	LVDS Data Port-A Lane-2 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
F1	LACN	LVDS Data Port-A Lane-C Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
F2	LACP	LVDS Data Port-A Lane-C Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
G1	LA3N	LVDS Data Port-A Lane-3 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
G2	LA3P	LVDS Data Port-A Lane-3 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
H1	LA4N	LVDS Data Port-A Lane-4 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
H2	LA4P	LVDS Data Port-A Lane-4 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
H3	LB0N	LVDS Data Port-B Lane-0 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
J3	LB0P	LVDS Data Port-B Lane-0 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.

Ball No.	Ball Name	Ball Description
H4	LB1N	LVDS Data Port-B Lane-1 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
J4	LB1P	LVDS Data Port-B Lane-1 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
H5	LB2N	LVDS Data Port-B Lane-2 Negative Input LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
J5	LB2P	LVDS Data Port-B Lane-2 Positive Input LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
H6	LBCN	LVDS Data Port-B Lane-C Negative Input (8-bit Mode) LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s. LVDS Data Port-B Lane-3 Negative Input (10-bit Mode) LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
J6	LBCP	LVDS Data Port-B Lane-C Positive Input (8-bit Mode) LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s. LVDS Data Port-B Lane-3 Positive Input (10-bit Mode) LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
H7	LB3N	LVDS Data Port-B Lane-3 Negative Input (8-bit Mode) LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s. LVDS Data Port-B Lane-4 Negative Input (10-bit Mode) LVDS Negative input of polarity swappable differential pairs up to 1.5Gb/s.
J7	LB3P	LVDS Data Port-B Lane-3 Positive Input (8-bit Mode) LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s. LVDS Data Port-B Lane-4 Positive Input (10-bit Mode) LVDS Positive input of polarity swappable differential pairs up to 1.5Gb/s.
C7	PS1	SPI Mode Select Input Bit-1 SPI mode select input bit-1.
B9	PS0	SPI Mode Select Input Bit-0 SPI mode select input bit-0.
B8	GPIO7	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please float this pin or connect to VSS.
C6	GPIO6	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please float this pin or connect to VSS.
B7	GPIO5	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please float this pin or connect to VSS.
A8	GPIO4	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please float this pin or connect to VSS.
B6	GPIO3	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please float this pin or connect to VSS.

Ball No.	Ball Name	Ball Description
A7	GPIO2	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please float this pin or connect to VSS.
B5	GPIO1	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please float this pin or connect to VSS.
A6	GPIO0	Digital Test Signal Output GPIO with internal 100K pull-down resistor for digital test signal output. When not used, please float this pin or connect to VSS.
A5	RST_N	Hardware Reset Input Chip reset signal. Active LOW.
C5	MISO	SPI Slave Serial Data Output It serves as the serial port data output for SPI slave register access.
A4	MOSI_ADR	SPI Slave Serial Data Input It serves as the serial port data input for SPI slave register access. I2C Device Address Select It serves as the serial port address select for I2C slave register access.
B4	SCK_CSCL	SPI Slave Serial Clock Input It serves as the serial port clock input for SPI slave register access. I2C Serial Clock Input It serves as the serial port data clock slave for I2C slave register access. Supports 1.8/3.3V CMOS logic.
C4	CSN_CSDA	SPI Slave Select It serves as the chip select input for SPI slave register access. Active LOW. I2C Serial Data Input/Output It serves as the serial port data IO for I2C slave register access. Supports 1.8/3.3V CMOS logic.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT8918	-40℃ to 85℃	7.5mmx7.5mm QFN64	Tape and Reel
LT8918	-40℃ to 85℃	5mm x 5mm BGA81	

Lontium Semiconductor Proprietary & Confidential

This document and the information it contains belong to Lontium Semiconductor. Any review, use, dissemination, distribution or copying of this document or its information outside the scope of a signed agreement with Lontium is strictly prohibited.

LONTIUM DISCLAIMS ALL WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THOSE OF NONINFRINGEMENT, MERCHANTABILITY, TITLE AND FITNESS FOR A PARTICULAR PURPOSE. CUSTOMERS EXPRESSLY ASSUME THEIR OWN RISH IN RELYING ON THIS DOCUMENT. LONTIUM PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN LIFE SUPPORT APPLIANCES, DEVICES OR SYSTEMS WHERE A MALFUNCTION OF A LONTIUM DEVICE COULD RESULT IN A PERSONAL INJURY OR LOSS OF LIFE.

Lontium assumes no responsibility for any errors in this document, and makes no commitment to update the information contained herein. Lontium reserves the right to change or discontinue this document and the products it describes at any time, without notice. Other than as set forth in a separate, signed, written agreement, Lontium grants the user of this document no right, title or interest in the document, the information it contains or the intellectual property in embodies.

Trademarks

Lontium™ and ClearedEdge™ is a registered trademark of Lontium Semiconductor. All Other brand names, product names, trademarks, and registered trademarks contained herein are the property of their respective owners.

Visit our corporate web page at: www.lontiumsemi.com
Technical support: support@lontium.com
Sales: sales@lontium.com