DS3815-1.3

MA8255

RADIATION HARD PROGRAMMABLE PERIPHERAL INTERFACE

The MA8255 is a general purpose programmable Input/Output device designed for use with the MA31750 microprocessor. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation.

In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be inputs or outputs. In the second mode (MODE 1), each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for hand-shaking and interrupt control signals. The third mode of operation (MODE 2) is the bidirectional bus mode, which uses 8 lines for a bidirectional bus and 5 lines, borrowing one from the other group, for hand-shaking.

FEATURES

- Radiation Hard to 1MRad (Si)
- High SEU Immunity, Latch Up Free
- Silicon-on-Sapphire Technology
- 24 Programmable I/O Pins
- All Inputs and Outputs are TTL Compatible
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Replaces Several MSI Packages
- Compatible with MA31750 (Mil-Std-1750A) Microprocessor

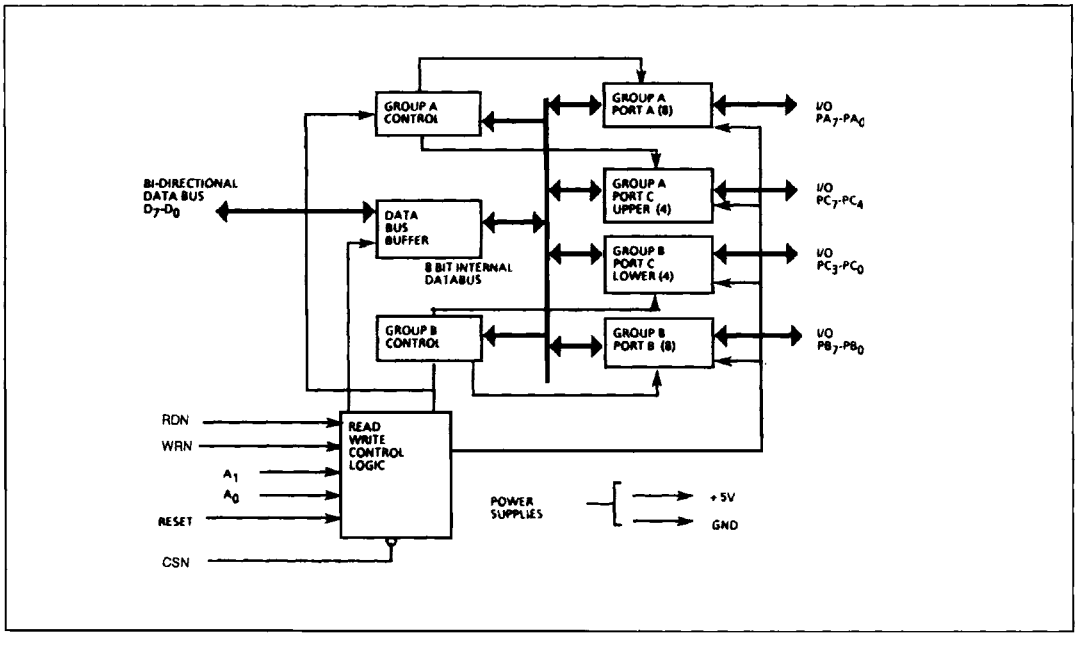


Figure 1: Block Diagram

FUNCTIONAL DESCRIPTION

The MA8255 is a programmable peripheral interface (PPI) device designed for use with MA31750. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the MA8255 is programmed by the system software so that, normally, no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the MA8255 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Reset (RESET)

A high on this input clears the control register and all ports (A,B,C) are set to the input mode.

Chip Select (CSN)

A low on this input pin enables the communication between the MA8255 and the CPU.

Read Select (RDN)

A low pulse on RDN indicates a CPU read from the MA8255.

Write Select (WRN)

A low pulse on WRN indicates a write from the CPU to the MA8255.

Port Select 0 and Port Select 1 (A0 and A1)

These input signals, in conjunction with the RDN and WRN inputs, control the selection of one of the three ports of the control word registers. They are normally connected to the least significant bits of the address bus.

Basic Operation

A1	A0	RDN	WRN	CSN	READ
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					WRITE
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE
x	x	x	x	1	DATA BUS → TRI-STATE
1	1	0	1	0	ILLEGAL CONDITION
x	x	1	1	0	DATA BUS → TRI-STATE

Table 1: Basic Operation

OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation, which can be selected by the system software:

Mode 0. Basic Input/Output
Mode 1. Strobed Input/Output
Mode 2 Bi-directional Bus

When the reset input goes high all ports will be set to the input mode (i.e. all 24 lines will be in the high impedance state) After the reset is removed the MA8255 can remain in the input mode with no additional initialisation required.

During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single MA8255 to service a variety of peripheral devices with a single software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status register, will be reset whenever the mode is changed.

Modes may be combined so that their functional definition can be tailored to almost any I/O structure. For instance; Group B can be programmed in Mode 0 whilst simultaneously Group A could be programmed in Mode 1.

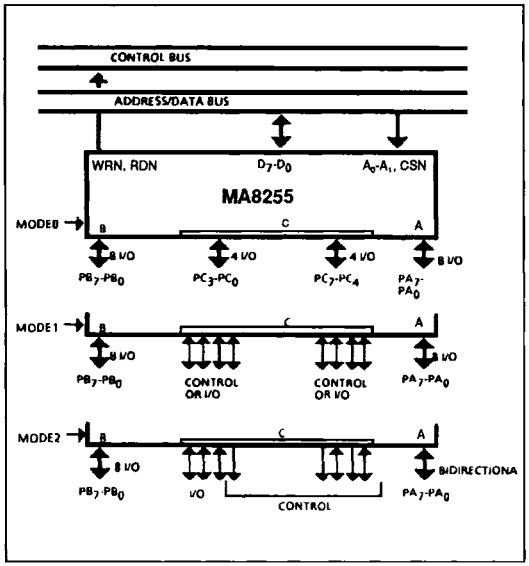


Figure 2: Basic Mode Definitions and Bus Interface

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single output instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as Status/Control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the MA8255 is programmed to operate in Mode 1 or 2, control signals are provided that can be used as interrupt request inputs to the CPU (figure 4). The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE register bit, using the Bit Set/Reset function of Port C.

This function allows the programmer to disallow or allow a specific I/O device to interrupt the CPU, without affecting any other device in the interrupt structure.

INTE register bit definitions:
(BIT-SET): INTE is SET -Interrupt enable
(BIT-RESET): INTE is RESET -Interrupt disable

Note: All mask register bits are automatically reset during mode selection and device reset.

Mode Definition Format (D_7= 1)

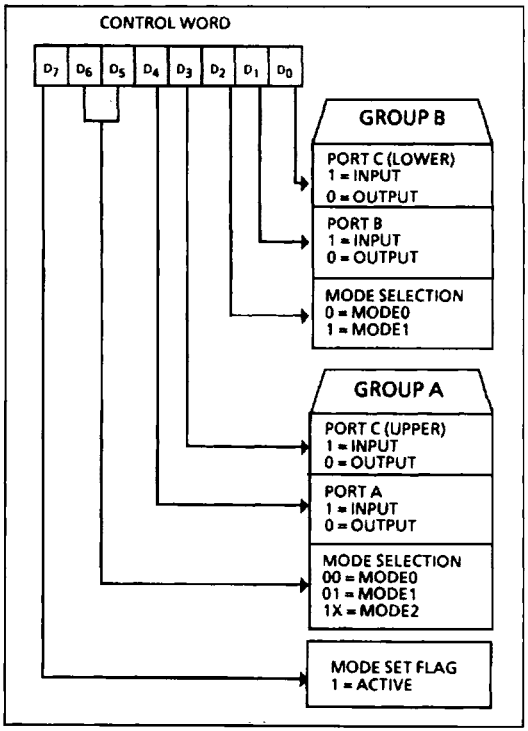


Figure 3: Mode Definition Format (D_7 = 1)

Bit Set/Reset Format (D_7 = 0)

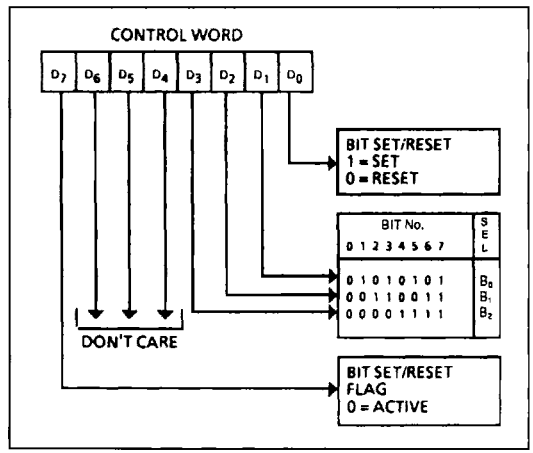


Figure 4: Bit Set/Reset Format (D_7 = 0)

Group A and Group B Controls

The functional configuration of each port is programmed by the system software. In essence, the CPU outputs a control word to the MA8255. The control word contains information such as mode, bit set, bit reset, etc., this initializes the functional configuration of the MA8255.

Each of the Control blocks (Group A and Group B) accept commands from the Read/Write Control Logic, receive control words from the internal data bus and issue the proper commands to its associated ports:

Control Group A - Port A and Port C upper (C7-C4) Control Group B - Port B and Port C lower (C3-C0)

The Control Word Register can only be written into. Therefore reading of the Control Word Register is not allowed.

Ports A, B and C

The MA8255 contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features to further enhance the power and flexibility of the MA8255.

Port A.

One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B.

One 8-bit data input/output latch/buffer and one 8-bit input buffer

Port C.

One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B

OPERATING MODE 0
(Basic Input/Output)

This functional configuration provides simple input and output operation for each of the three ports. No handshaking is required; data is simply written to or read from a specified port.

- Two 8-bit ports and 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

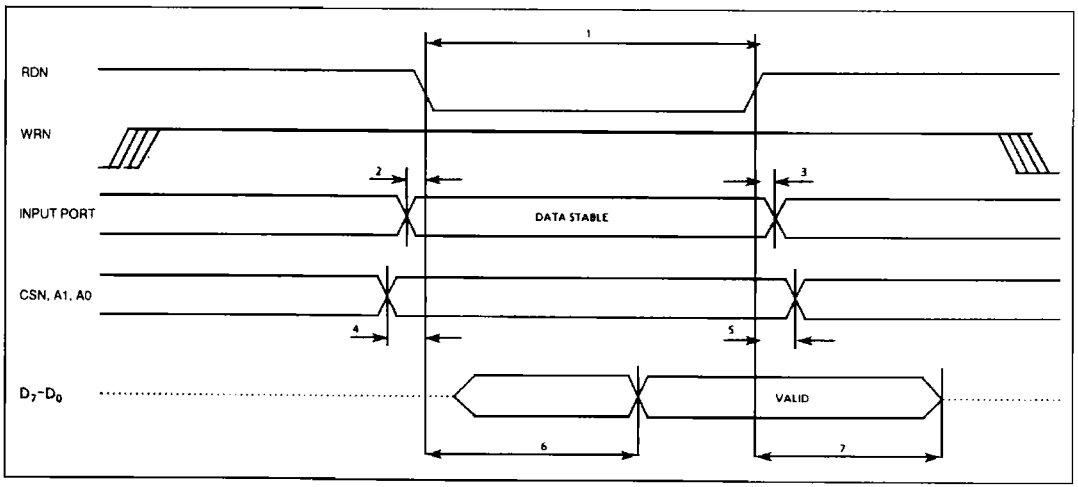


Figure 5: Basic Input (Read) Timing Diagram

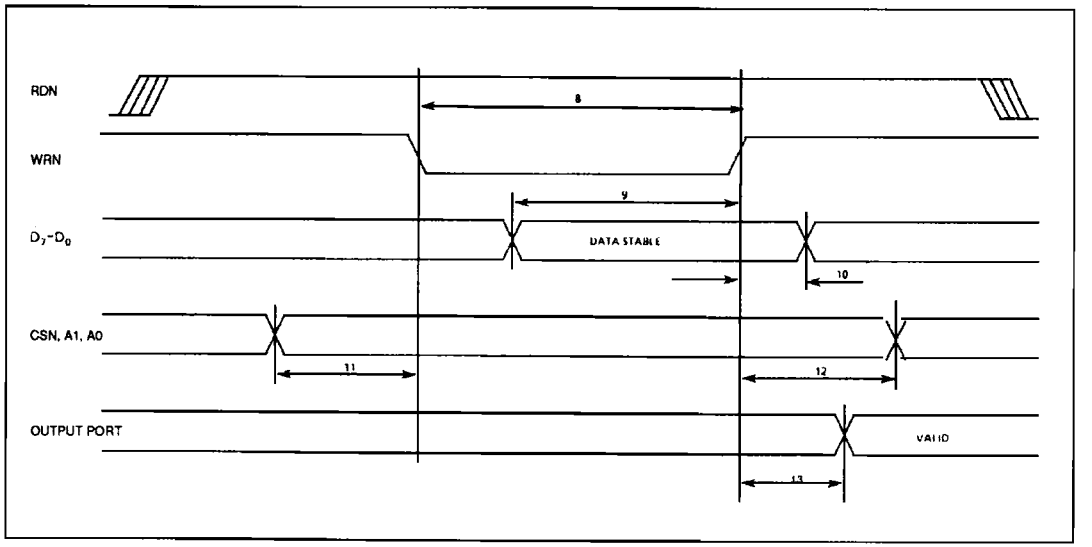


Figure 6: Basic Input (Write) Timing Diagram

Port Definition Mode 0

D_4	D_3	D_1	D_0	PORT A (UPPER)	PORT C	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	INPUT	INPUT
1	1	0	0	INPUT	INPUT	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	INPUT	INPUT

Table 2: Port Definition Mode 0 (See Also Figure 3)

OPERATING MODE 1
(Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or handshaking signals. In mode 1, port A and port B use the lines on port C to generate or accept these handshaking signals

- Two Groups (Group A and Group B) .
- Each Group contains one 8-bit data port and one 4-bit control/data port,
- The 8-bit data port can be either input or output, Both inputs and outputs are latched,
- The 4-bit port is used for control and status of the 8-bit data port.

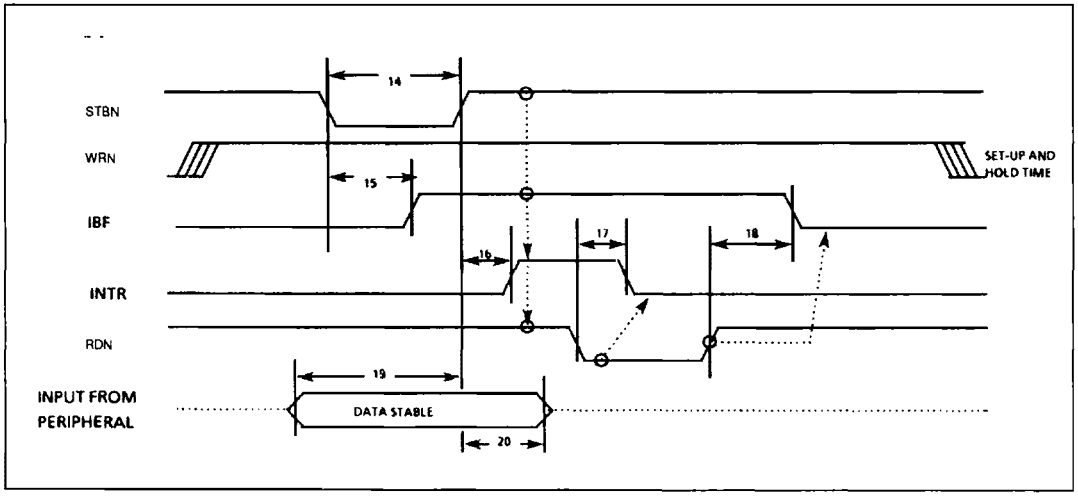


Figure 7: Strobed Input Timing Diagram

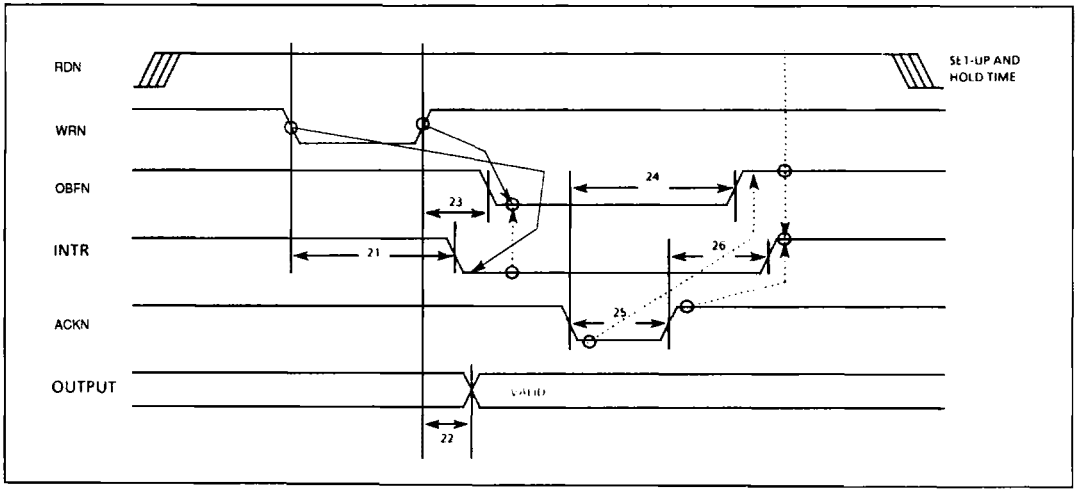


Figure 8: Strobed Output Timing Diagram

Input Control Signal Definition (Mode 1)

STBN (Strobe Input).

A low on this input loads data into the input latch.

IBF (Input Buffer Register Bit).

A high on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement.

IBF is set by STBN active pulse (which strobes data into the device) and is reset by the rising edge of RDN (which reads the latched data out of the device).

INTR (Interrupt Request).

A high on this output can be used to interrupt the CPU when an input device is requesting service, INTR is set by the STBN being high and IBF being high and INTE being enabled, It is reset by the falling edge of RDN, This procedure allows an input device to request service from the CPU by simply strobing its data into the port,

INTE A: Controlled by bit set/reset of PC_4

INTE B: Controlled by bit set/reset of PC_2

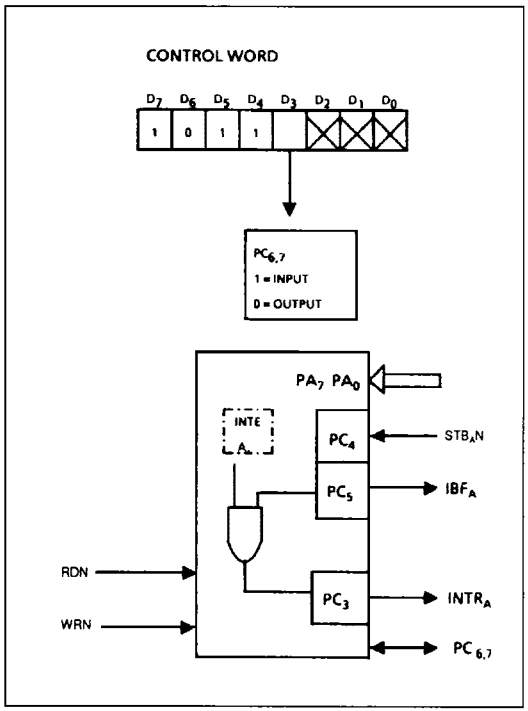


Figure 9: Strobed Input (PORT A)

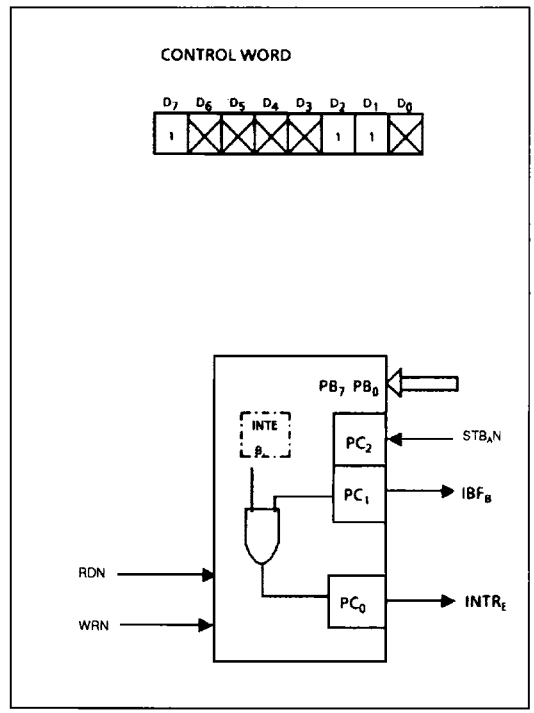


Figure 10: Strobed Input (PORT B)

Output Control Signal Definition (Mode 1)

OBFN (Output Buffer Full Register Bit).

The OBFN output will go low to indicate that the CPU has written data out to the specified port. The OBF register bit will be set by the rising edge of the WRN input and reset by ACKN input being low.

ACKN (Acknowledge Input).

A low on this input informs the 8255 that the data from port A or port B has been accepted; in essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request).

A high on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU, INTR is set when ACKN is high, OBF is high and INTE is high. It is reset by the falling edge of WRN.

INTE A: Controlled by bit set/reset of PC_6
INTE B: Controlled by bit set/reset of PC_2

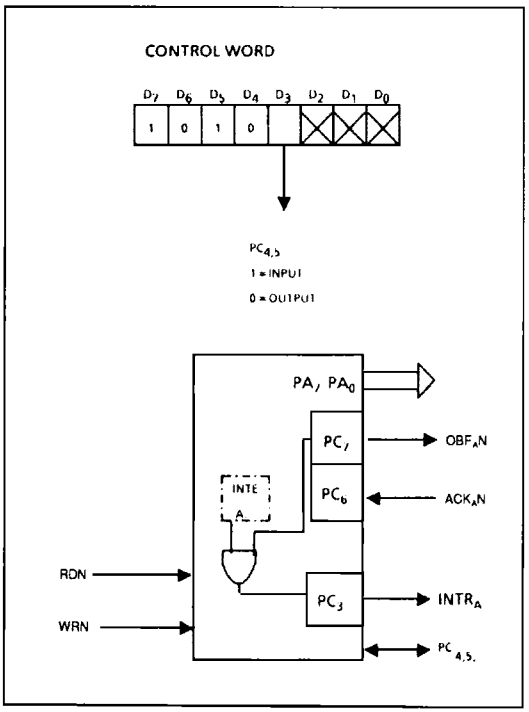


Figure 11: Strobed Output (PORT A)

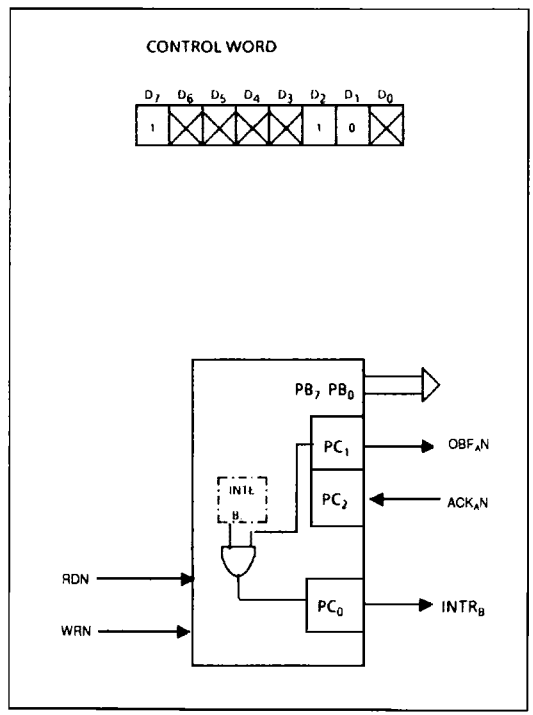


Figure 12: Strobed Output (PORT B)

Combinations of Mode 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

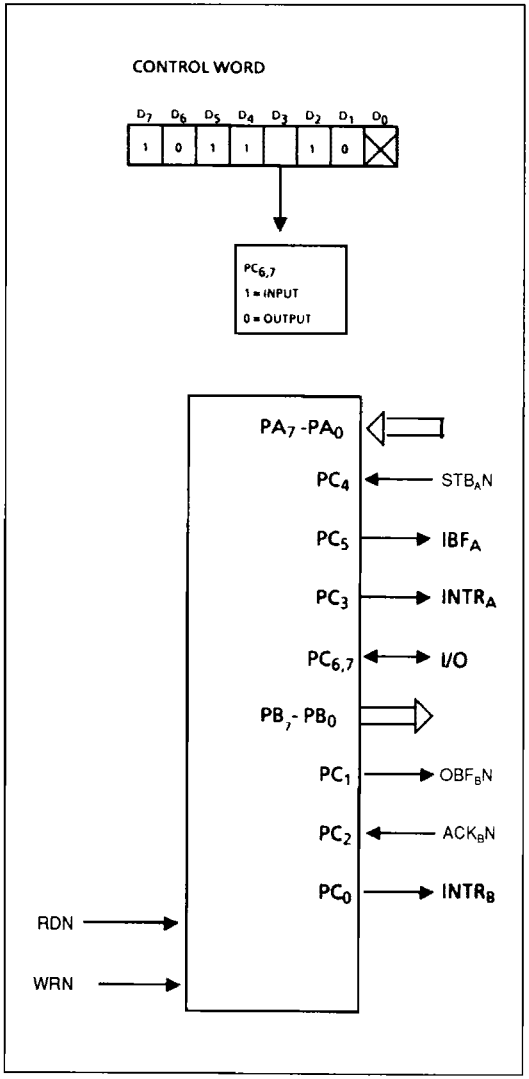


Figure 13: PORT A (STROBED INPUT) PORT B (STROBED OUTPUT)

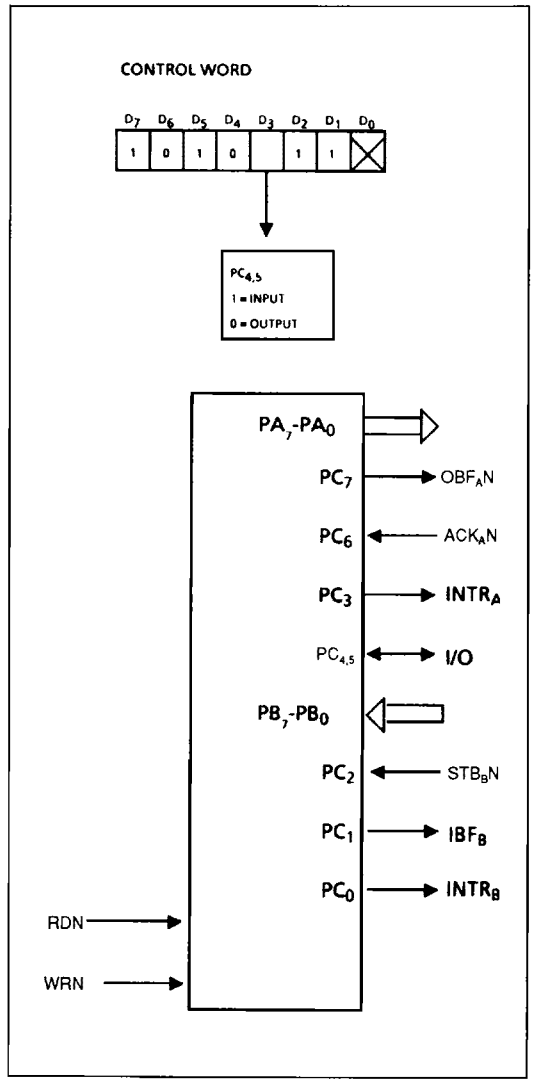
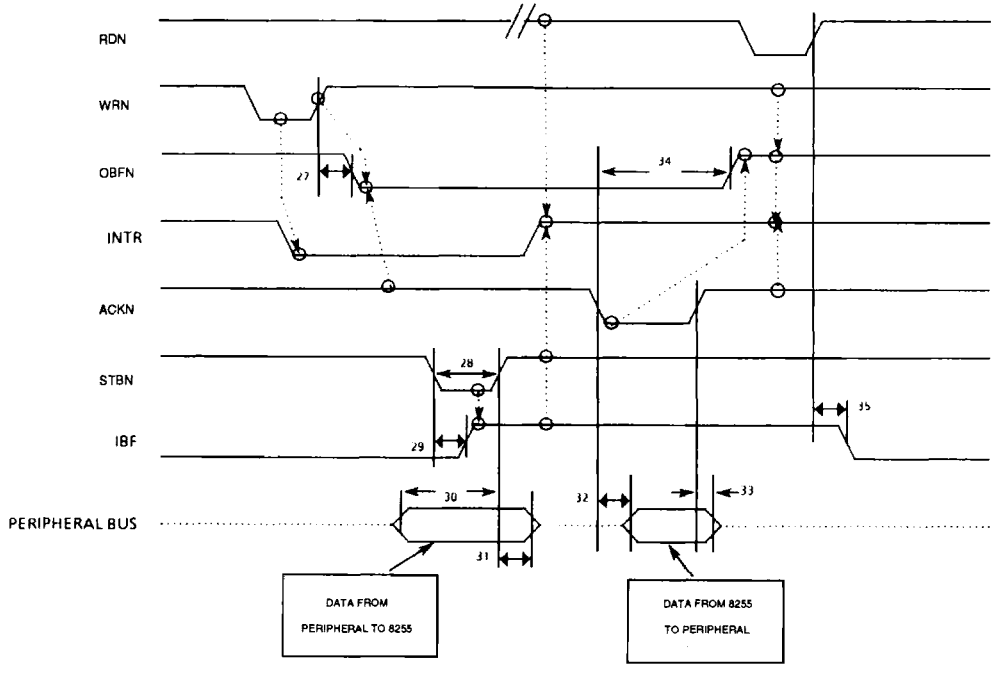


Figure 14: PORT A (STROBED OUTPUT) PORT B (STROBED INPUT)

OPERATING MODE 2
(Strobed Bidirectional Bus I/0)

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O) . Handshaking signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1, Interrupt generation and enable/disable functions are also available.

- Used in group A only.
- One 8-bit bidirectional bus port (port A) and 5-bit control port (port C).
- Both inputs and outputs are latched,
- The 5-bit control port (port C) is used for control and status of the 8-bit bidirectional bus port (port A).



The sequence of events to output information is:
WRN strobes data into the device on the rising edge of WRN. This in turn causes OBFN to go low. The ACKN pulse reads the data out, and also resets OBFN. An interrupt to obtain more data is generated when INTE1 (PC_6) = 1, WRN = 1, ACKN = 1, OBFN = 1. The next WRN will clear INTR.
The sequence of events to input information is: STBN strobes data into the device. This causes IBF to be set. An interrupt to forward the data is generated when INTE2 (PC_4) = 1, RDN = 1, STBN = 1, IBF = 1. INTR is reset by RDN.

Figure 15: Bidirectional Timing Diagram

BIDIRECTIONAL BUS L/O CONTROL

Signal Definition (Mode 2)

INTR (Interrupt Request):
A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

OBFN (Output Buffer Full):
The OBFN output will go low to indicate that the CPU has written data out to port A.

ACKN (Acknowledge):
A low on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state,

INTE 1 (INTE register bit associated with OBFN):
Controlled by Bit Set/Reset of PC_6.

Input Operations

STBN (Strobe input):
A low on this input loads data in to the input latch,

IBF (Input Buffer Full Register Bit):
A high on this output indicates data has been loaded in to the input latch,

INTE 2 (The INTE register bit associated with IBF).
Controlled by Bit Set/Reset of PC_4.

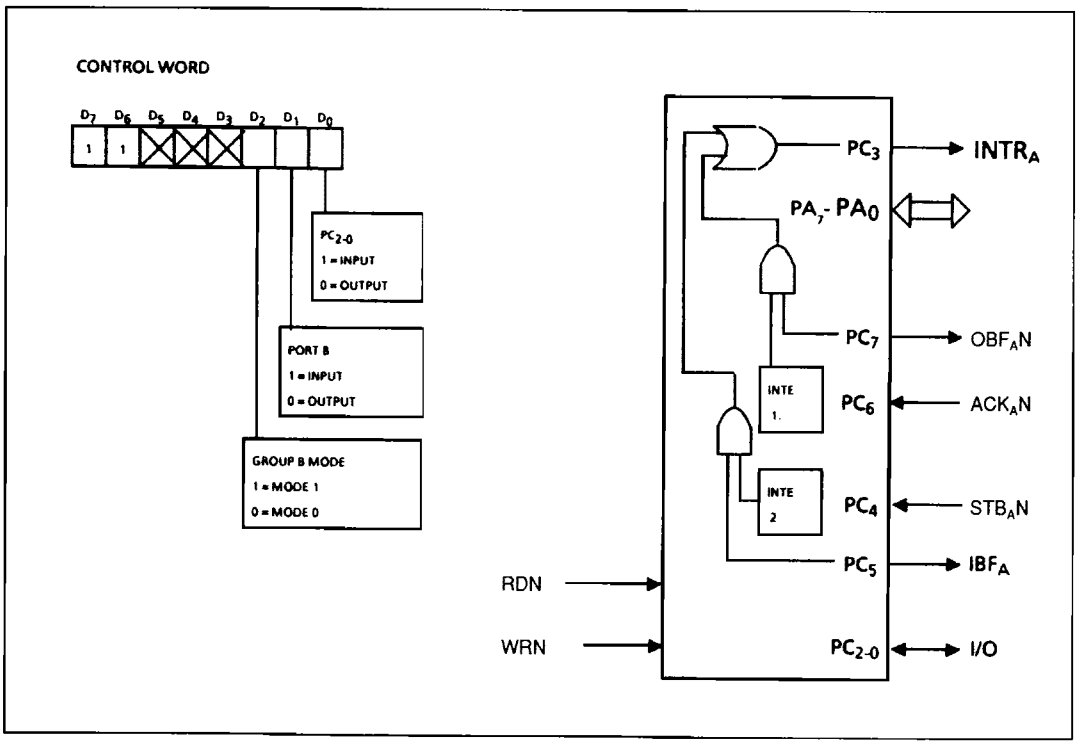


Figure 16: Mode 2 Bidirectional

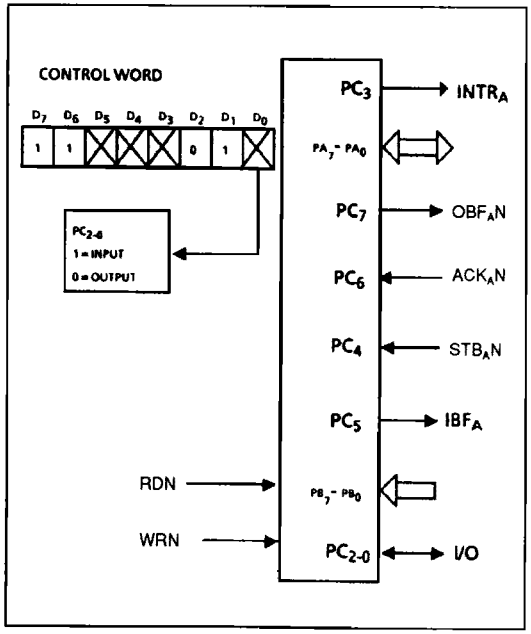


Figure 17a: Mode 2 and Mode 0 (Input)

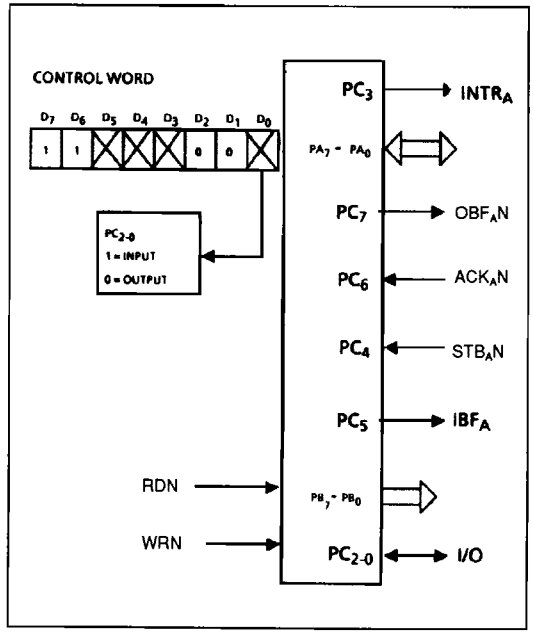


Figure 17b: Mode 2 and Mode 0 (Output)

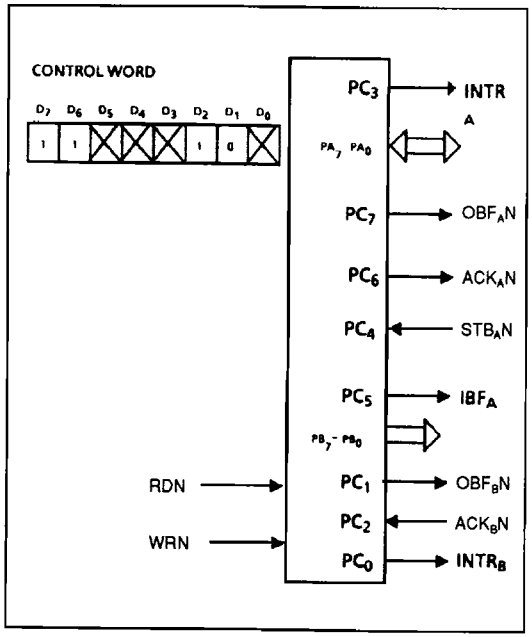


Figure 17c: Mode 2 and Mode 1 (Output)

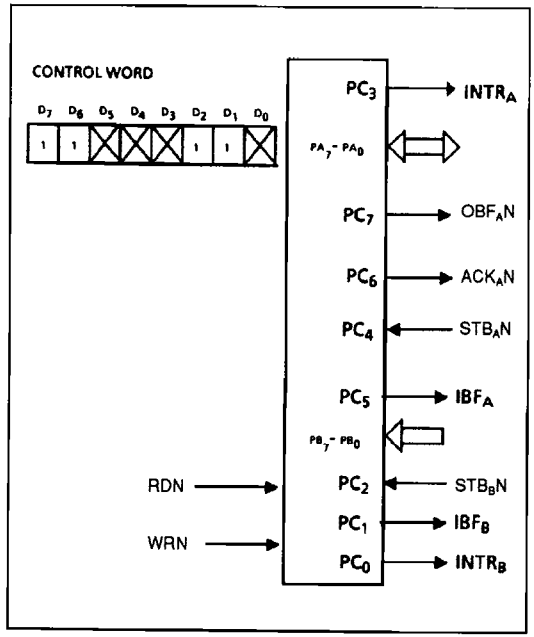


Figure 17d: Mode 2 and Mode 1 (Input)

Mode Definition Summary

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	
PA_0	IN	OUT	IN	OUT	⇐ ⇒
PA_1	IN	OUT	IN	OUT	⇐ ⇒
PA_2	IN	OUT	IN	OUT	⇐ ⇒
PA_3	IN	OUT	IN	OUT	⇐ ⇒
PA_4	IN	OUT	IN	OUT	⇐ ⇒
PA_5	IN	OUT	IN	OUT	⇐ ⇒
PA_6	IN	OUT	IN	OUT	⇐ ⇒
PA_7	IN	OUT	IN	OUT	⇐ ⇒
PB_0	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_1	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_2	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_3	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_4	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_5	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_6	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_7	IN	OUT	IN	OUT	Port B mode 0 or 1
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	OBF_BN	I/O
PC_2	IN	OUT	STB_BN	ACK_BN	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	STB_AN	I/O	STB_AN
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	ACK_AN	ACK_AN
PC_7	IN	OUT	I/O	OBF_AN	OBF_AN

Table 3: Mode Definition Summary

Special Mode Combination Considerations.

There are several combinations of modes when not all of the bits in port C are used for control or status. The remaining bits can be used as follows:

If programmmed as inputs-

All input lines can be accessed during normal port C read.

If programmed as outputs

Bits in C upper (PC7-PC4) must be individually accessed using a bit set/reset function.

Bits in C lower (PC3-PC0) can be accessed using the bit set/reset function or bits PC2-PC0 may also be accessed as a trio by writing into port C.

Reading Port C Status.

In Mode 0 Port C transfers data from or to the peripheral device, When the MA8255 is programmed to function in Modes 1 or 2 Port C generates or accepts handshaking signals with the peripheral device, Reading the contents of Port C allows the programmer to test or verify the status of each peripheral device and change the program flow accordingly.

There is no special instruction to read the Status Information from Port C. A normal read operation of Port C is executed to perform this function.

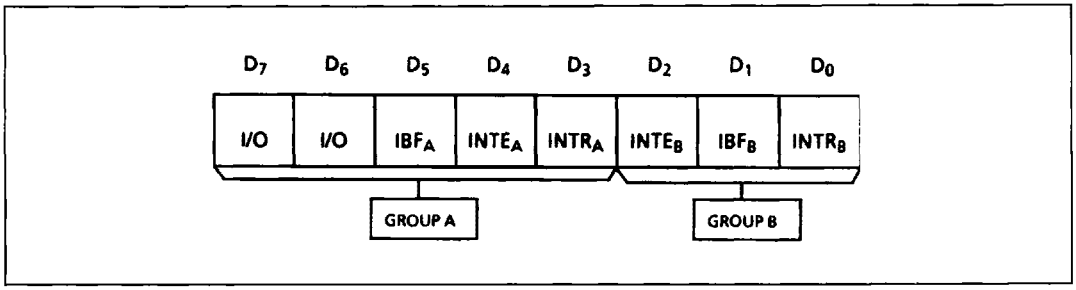


Figure 18a: Mode 1 Input Configuration

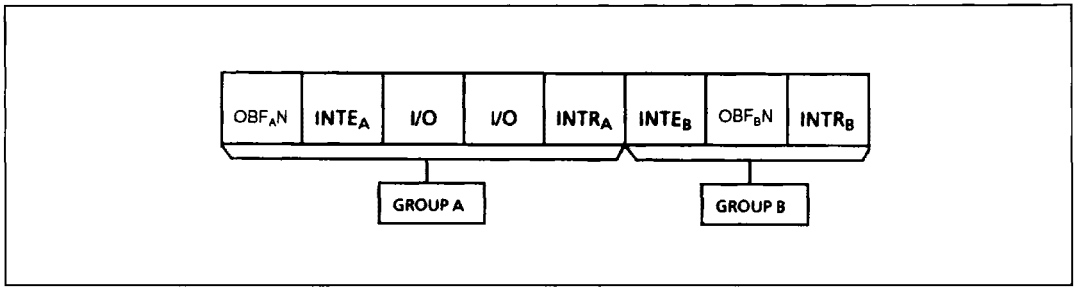


Figure 18b: Mode 1 Output Configuration

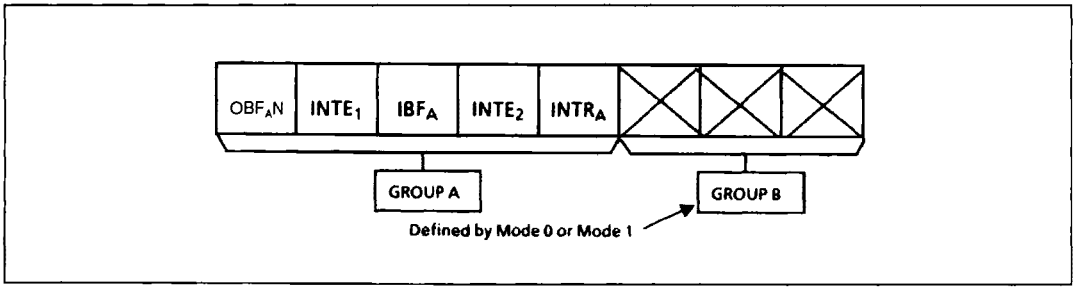


Figure 18c: Mode 2

Subgroup	Definition
1	Static characteristics specified in Table 6 at +25°C
2	Static characteristics specified in Table 6 at +125°C
3	Static characteristics specified in Table 6 at -55°C
7	Functional characteristics specified in Table 7 at +25°C
8A	Functional characteristics specified in Table 7 at +125°C
8B	Functional characteristics specified in Table 7 at -55°C
9	Switching characteristics specified in Table 7 at +25°C
10	Switching characteristics specified in Table 7 at +125°C
11	Switching characteristics specified in Table 7 at -55°C

Table 4: Definition of Subgroups

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Table 5: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad(Si)			Total dose ≤1M Rad(Si)		Units
			Min	Typ	Max	Min	Max	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	4.5	5.5	V
V_{IH}	Input High Voltage	-	2.0	-	-	2.0	-	V
V_{IL}	Input Low Voltage	-	-	-	0.8	-	0.3	V
V_{OH}	Output High Voltage	I_{OH} = -5mA	3.5	-	-	3.5	-	V
V_{OL}	Output Low Voltage	I_{OL} = 10mA	-	-	V_{SS}+0.4	-	V_{SS}+0.4	V
I_{IN}	Input Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±10	-	±100	µA
I_{OZ}	Tristate Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±50	-	±100	µA
I_{DD}	Power Supply Current	Static,	-	0.1	10	-	10	mA

Note 1: Guaranteed but not tested at -55C.
V_{DD} = 5V±10%, over full operating temperature range.
Mil-Std-883, method 5005, subgroups 1, 2, 3

Table 6: Electrical Characteristics

AC ELECTRICAL CHARACTERISTICS

	Parameter	Min.	Max.	Units		Parameter	Min.	Max	Units
					18	RDN ⇑ to IBF ⇑	-	65	ns
					19	Peripheral Data set up to STBN ⇑	100		ns
1	RDN pulse width	65	-	ns	20	Peripheral Data hold after STBN ⇑	100		ns
2	Peripheral Data set up to RDN	0	-	ns	21	WRN ⇓ to INTR ⇓ (note 4)	-	WRN +100	ns
3	Peripheral Data hold after RDN	10	-	ns	22	Output valid from WRN ⇑	-	100	ns
4	CSN, A1, AO setup to RDN ⇓	0	-	ns	23	WRN ⇑ to OBFN ⇓	-	105	ns
5	CSN, A1, AO hold after RDN ⇑	0	-	ns	24	ACKN ⇓ to OBFN ⇑	-	50	ns
6	Data valid from RDN ⇓	-	60	ns	25	ACKN pulse width	100	-	ns
7	Data float from RDN ⇑ (note 5)	10	100	ns	26	ACKN ⇑ INTR ⇑	-	80	ns
8	WRN pulse width	65	-	ns	27	WRN ⇑ to OBFN ⇓	-	105	ns
9	Data Set up to WRN ⇑	25	-	ns	28	STBN pulse width	100	-	ns
10	Data hold after WRN ⇑	30	-	ns	29	STBN ⇓ to IBF ⇑	-	65	ns
11	CSN, A1, AO setup to WRN ⇓	5	-	ns	30	Peripheral Data set up to STBN ⇑	0	-	ns
12	CSN, A1, AO hold after WRN ⇑	20	-	ns	31	Perlpheral Data hold after STBN ⇑	100	-	ns
13	Output valid from WRN ⇑	-	100	ns	32	Output valid from ACKN ⇓	-	45	ns
14	STBN pulse width	100	-	ns	33	Output float from ACKN ⇑ (note 5)	10	100	ns
15	STBN ⇓ to IBF ⇑	-	65	ns	34	ACKN ⇓ to OBFN ⇑	-	50	ns
16	STBN ⇑ to INTR ⇑	-	65	ns	35	RDN ⇑ to IBF ⇓	-	65	ns
17	RDN ⇓, to INTR ⇓	-	65	ns					

1. V_{DD} = 5V±10% and C_{CL} = 50pF, over full operating temperature range.
2. Input Pulse V_{SS} to 3.0 Volts.
3. Times Measurement Reference Level 1.5 Volts.
4. WRN = WRN Pulse Width.
5. Measured by a 1.0 Volt change in output voltage. Outputs tied to V_{SS} via 680Ω.

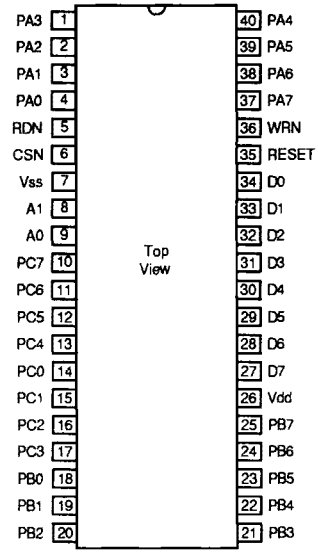
Mil-Std-883, method 5005, subgroups 7, 8A, 8B

Table 7: AC Electrical Characteristics

PACKAGE OUTLINES & PIN ASSIGNMENTS

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	51.31	-	-	2.020
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG405



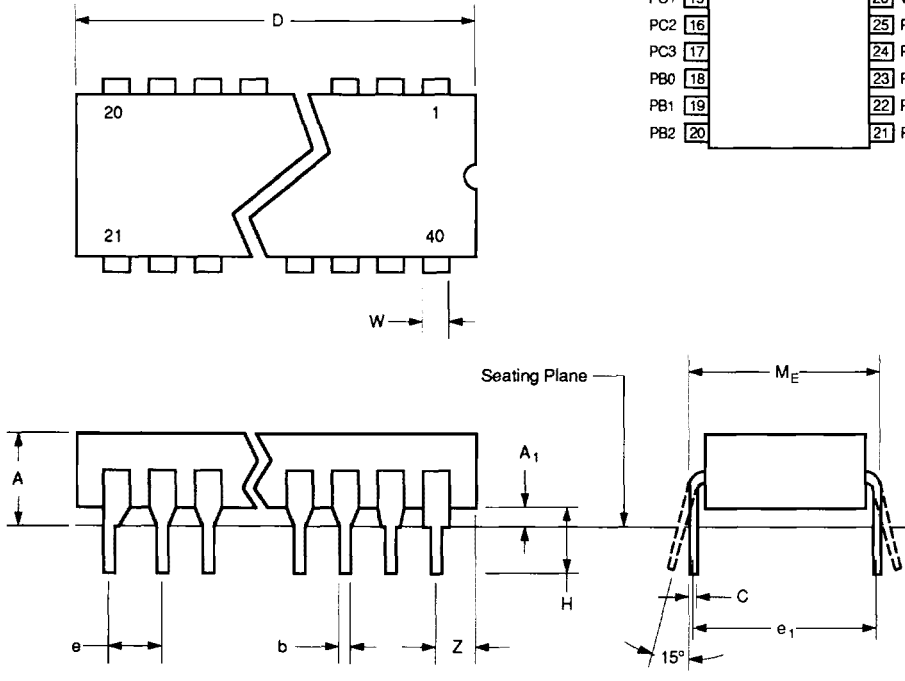


Figure 19: 40-Lead Ceramic DIL (Solder Seal) - Package Style C

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.41	-	-	0.095
b1	-	0.64	-	-	0.025	-
D	16.33	-	16.81	0.643	-	0.662
E	16.33	-	16.81	0.643	-	0.662
e	-	1.27	-	-	0.050	-
Z	-	1.91 Typ.	-	-	0.075 Typ.	-

XG446

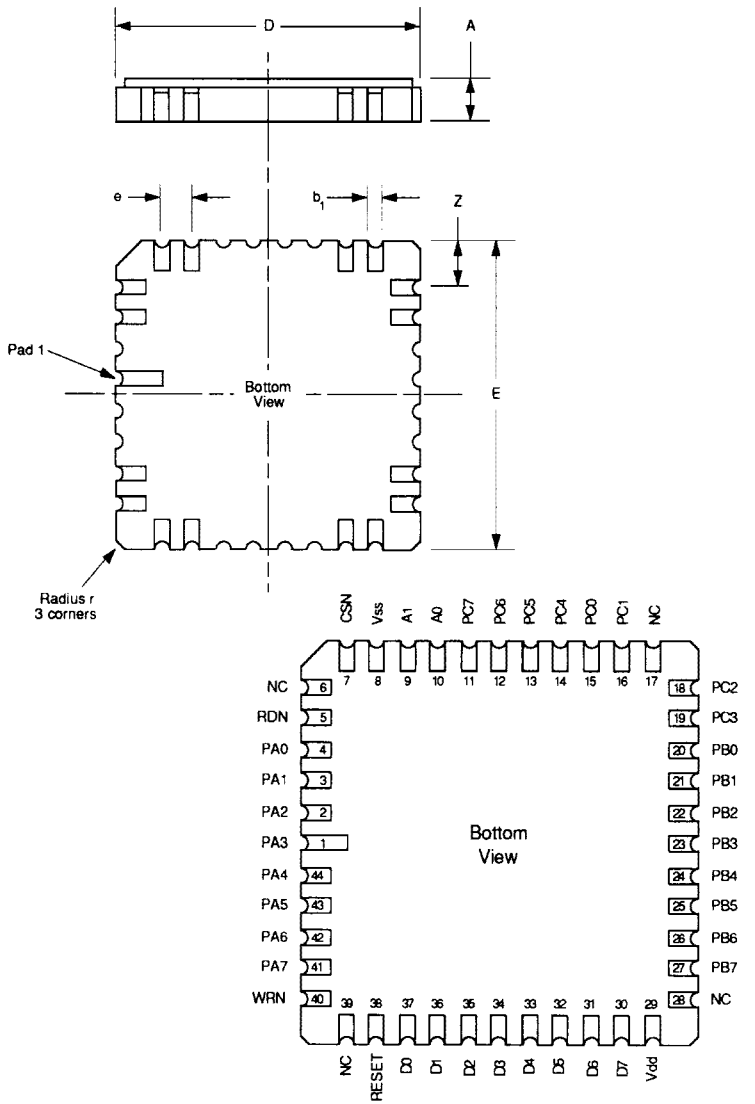


Figure 20: 44-Pad Leadless Chip Carrier (Package Style L)

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)	$3x10^5$ Rad(Si)
Transient Upset (Survivability)	$>10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$1x10^{15}$ neutrons/cm^2
Single Event Upset (GSO 10% worst case)	$<10^{-10}$ errors/bitday
Latch-up	Not possible

Figure 21: Radiation Hardness Parameters

ORDERING INFORMATION