

### **General Description**

The MAX14805/MAX14806 provide high-voltage switching on 16 channels for ultrasonic imaging. Both devices are ideal for the following applications: banks selection in biplane or triplane ultrasound probes and relays replacement. The devices utilize 200V process technology to provide sixteen high-voltage, low-charge injection SPST switches, controlled by a digital interface.

The MAX14805/MAX14806's output switches are configured as two sets of eight SPST analog switches. The switches are controlled by two input logic controls, DIN1 and DIN2 (respectively for switch 0 to 7 and switch 8 to 15). The MAX14806 features integrated  $40k\Omega$  bleed resistors on each switch terminal, which help to reduce voltage buildup in capacitive loads such as piezoelectric elements.

The MAX14805/MAX14806 operate with a wide range of high-voltage supplies, including VPP/VNN = +100V/-100V, +200V/0V, and +40V/-160V. The digital interface operates from a separate Vpp supply from +2.7V to +5.5V. Digital inputs DIN1, DIN2, and LE operate on the VDD supply voltage.

The MAX14805CCM+ is a drop-in replacement for the Supertex HV2631. The MAX14806CCM+ is a drop-in replacement for the Supertex HV2731. Both devices are available in the 48-pin, TQFP package and are specified for the extended -40°C to +85°C temperature range.

### **Features**

- HVCMOS Technology for High Performance
- ♦ Two Sets of 8-Channel SPST High-Voltage Analog **Switches**
- ♦ DC to 20MHz Low-Voltage Analog Signal **Frequency Range**
- ♦ +2.7V to +5.5V Logic Supply Voltage
- ◆ Ultra-Low (0.1µA) (typ) Quiescent Current
- ♦ Low-Charge Injection, Low-Capacitance 20Ω **Switches**
- ♦ -77dB (typ) Off-Isolation at 5MHz (50Ω)
- ♦ Flexible, High-Voltage Supplies (Vpp VNN = 230V)

Applications

Medical Ultrasound Imaging Nondestructive Test (NDT)

## **Ordering Information/Selector Guide**

PART	SWITCH CHANNELS	BLEED RESISTOR	SECOND SOURCE	PIN-PACKAGE
MAX14805CCM+	2 x 8	No	HV2631	48 TQFP
MAX14806CCM+	2 x 8	Yes	HV2731	48 TQFP

Note: All devices are specified over the extended -40°C to +85°C operating temperature range. +Denotes a lead(Pb)-free/RoHS-compliant package.

#### **ABSOLUTE MAXIMUM RATINGS**

(All voltages referenced to GND.)
VDD Logic Supply Voltage0.3V to +7V
VPP - VNN Supply Voltage230V
VPP Positive Supply Voltage0.3V to +220V
VNN Negative Supply Voltage+0.3V to -220V
Logic Inputs Voltage (LE, DIN1, DIN2)0.3V to +7V
Analog Signal Range (SW_)(-0.3V + VNN) to (VNN + 200V)
Peak Analog Signal Current per Channel3A
Continuous Power Dissipation (TA = +70°C)
48-Pin TQFP (derate 22.7mW/°C above +70°C) 1818mW

Junction-to-Ambient Thermal Resistance θJA (Note 1)	44°C/W
Junction-to-Case Thermal Resistance	
θJC (Note 1)	10°C/W
Operating Temperature Range	40°C to +85°C
Storage Temperature Range	65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

 $(V_{DD} = +2.7V \text{ to } +5.5V, V_{PP} = +40V \text{ to } (V_{NN} + 200V), V_{NN} = -40V \text{ to } -160V, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted.}$  Typical values are at  $T_A = +25^{\circ}\text{C.}$ ) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V <sub>DD</sub> Supply Voltage	V <sub>DD</sub>		2.7		5.5	V
Vpp Supply Voltage	VPP		40	100	V <sub>NN</sub> + 220	V
V <sub>NN</sub> Supply Voltage	V <sub>NN</sub>		-160	-100	-15	V
V <sub>DD</sub> Supply Quiescent Current	IDDQ				5	μΑ
V <sub>DD</sub> Supply Dynamic Current	IDDD	$V_{DD} = +5V$ , $\overline{LE} = GND$ , $f_{DIN1} = f_{DIN2} = 5MHz$			2	mA
Vpp Supply Quiescent Current	IPPQ				10	μΑ
	IPPD	$V_{PP} = +40V$ , $V_{NN} = -160V$ , $f_{SW} = 50kHz$ , $f_{DIN1} = f_{DIN2} = 50kHz$ , $\overline{LE} = GND$			5	
VPP Supply Dynamic Current (All Channel Switching Simultaneously)		$V_{PP} = +100V$ , $V_{NN} = -100V$ , $f_{SW} = 50kHz$ , $f_{DIN1} = f_{DIN2} = 50kHz$ , $\overline{LE} = GND$			6	mA
Cirruitaneously)		$V_{PP} = +160V$ , $V_{NN} = -40V$ , $f_{SW} = 50kHz$ , $f_{DIN1} = f_{DIN2} = 50kHz$ , $\overline{LE} = GND$			7	
V <sub>NN</sub> Supply Quiescent Current	I <sub>NNQ</sub>				10	μΑ
V <sub>NN</sub> Supply Dynamic Current (All Channel Switching Simultaneously)		$V_{PP} = +40V$ , $V_{NN} = -160V$ , $f_{SW} = 50kHz$ , $f_{DIN1} = f_{DIN2} = 50kHz$ , $\overline{LE} = GND$			5.5	
	INND	$\begin{aligned} V_{PP} &= +100V, \ V_{NN} = -100V, \ f_{SW} = 50kHz, \\ f_{DIN1} &= f_{DIN2} = 50kHz, \ \overline{LE} = GND \end{aligned}$			5	mA
		$V_{PP} = +160V$ , $V_{NN} = -40V$ , $f_{SW} = 50kHz$ , $f_{DIN1} = f_{DIN2} = 50kHz$ , $\overline{LE} = GND$			4.5	

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{DD} = +2.7V \text{ to } +5.5V, V_{PP} = +40V \text{ to } (V_{NN} + 200V), V_{NN} = -40V \text{ to } -160V, T_{A} = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted.}$  Typical values are at  $T_{A} = +25^{\circ}C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH CHARACTERISTICS							
Analog Signal Range	V <sub>SW</sub> _	(Note 3)		V <sub>NN</sub>		VPP - 10	V
		VPP = +40V, V <sub>NN</sub> = -160V,	Isw_ = 5mA		28	52	
		$V_{SW} = -100V$ , $V_{SW} = 0V$	I <sub>SW_</sub> = 200mA		22	37	
Small-Signal	Rons	VPP = +100V,	Isw_ = 5mA		22	34	
On-Resistance		$V_{NN} = -100V,$ $V_{SW} = 0V$	I <sub>SW_</sub> = 200mA		18	27	Ω
		VPP = +160V,	Isw_ = 5mA		20	30	
		$V_{NN} = -40V,$ $V_{SW} = 0V$	Isw_ = 200mA		16	23	
Small-Signal On-Resistance Matching	ΔRons	VPP = +100V, Vp	NN = -100V, ISW_ = 5mA		5		%
Large-Signal Switch On-Resistance	Ronl	Vsw_ = Vpp - 10V, Isw_ = 1A			15		Ω
Shunt Resistance	RINT	MAX14806 only		27	40	53	kΩ
Switch-Off Leakage	ISW_(OFF)	V <sub>SW</sub> = V <sub>PP</sub> - 10V or unconnected (MAX14805 only) (Figure 1)			0	2.5	μΑ
Switch-Off DC Offset		$R_L = 100$ k $\Omega$ (Figure 1)		-30		+30	mV
Switch Output Peak Current		100ns pulse width, 0.1% duty cycle			3		А
Switch Output Isolation Diode Current		300ns pulse width, 2% duty cycle (Figure 1)			2		А
SWITCH DYNAMIC CHARACTI	RISTICS						
Turn-On Time	ton	Vsw_ = Vpp - 10' Vnn = -40V to -1				5	μs
Turn-Off Time	toff	$V_{SW} = V_{PP} - 10V, R_L = 10k\Omega,$ $V_{NN} = -40V \text{ to } -160V \text{ (Figure 1)}$				5	μs
Output Switching Frequency	fsw	Duty cycle = 50%				50	kHz
Off-Isolation	VISO		$1k\Omega$ , $C_L = 15pF$ (Figure 1)		-50		dB
Croostall	Vot	$f = 5MHz$ , $R_L = 50\Omega$ (Figure 1) $f = 5MHz$ , $R_L = 50\Omega$ (Figure 1)			-77		4D
Crosstalk	VCT	$  1 = 3 V \Pi Z, \Pi L = 3$	DULZ (Figure 1)		-80		dB
Switch Off-Capacitance (Note 4)	Csw_(off)	Vsw_ = 0V, f = 1	MHz	4	11	18	рF
Switch On-Capacitance (Note 4)	C <sub>SW_(ON)</sub>	V <sub>SW</sub> _ = 0V, f = 1MHz		20	36	56	pF
Output Voltage Spike (Note 4)	Vspk	$R_L = 50\Omega$ (Figure 1)		-500		+250	mV
Small-Signal Analog Bandwidth	f <sub>BW</sub>	V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V, C <sub>L</sub> = 200pF			20		MHz

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{DD} = +2.7V \text{ to } +5.5V, V_{PP} = +40V \text{ to } (V_{NN} + 200V), V_{NN} = -40V \text{ to } -160V, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted.}$  Typical values are at  $T_A = +25^{\circ}C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
		VPP = +40V, V <sub>NN</sub> = -160V, V <sub>SW</sub> = 0V (Figure 1)		650			
Charge Injection	Q	VPP = +100V, V <sub>NN</sub> = -100V, V <sub>SW</sub> = 0V (Figure 1)		450		рС	
		VPP = +160V, V <sub>NN</sub> = -40V, V <sub>SW</sub> = 0V (Figure 1)		250			
LOGIC LEVELS (DIN1, DIN2, LE)							
Logic-Input Low Voltage	VIL				0.75	V	
Logic-Input High Voltage	VIH		V <sub>DD</sub> - 0.75			V	
Logic-Input Capacitance	CIN				10	pF	
Logic-Input Leakage Current	liN		-1		+1	μΑ	
LOGIC TIMING (See Timing Diagram, Figure 2)							
Setup Time	tsd		30			ns	
Hold Time	tHOLD				30	ns	
Time Width of LE	twlE		30			ns	

Note 2: All devices are 100% tested at TA = +85°C. Limits over the operating temperature range are guaranteed by design and characterization.

Note 3: The analog signal input  $V_{SW}$  must satisfy  $V_{NN} \le V_{SW} \le V_{PP}$  or remain unconnected during power-up.

Note 4: Guaranteed by characterization; not production tested.

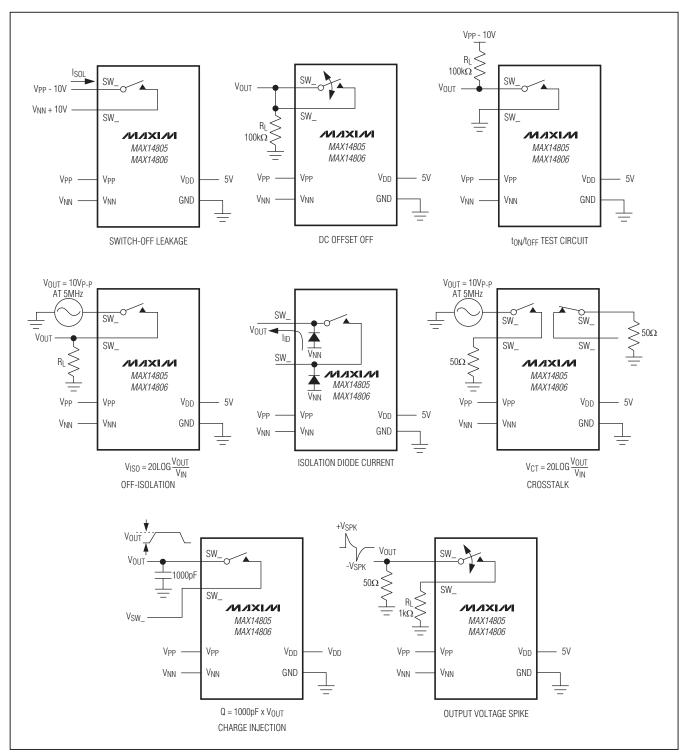
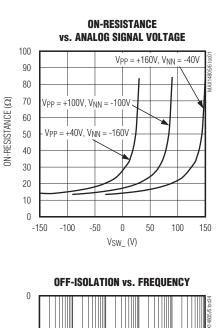
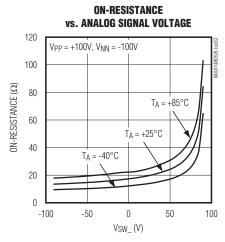


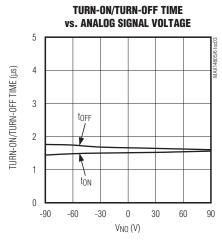
Figure 1. Test Circuits

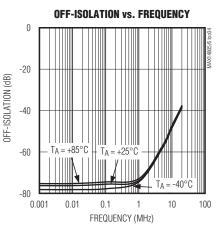
### **Typical Operating Characteristics**

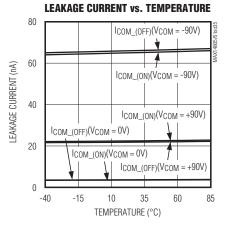
 $(V_{DD} = +3V, V_{PP} = +100V, V_{NN} = -100V, T_A = +25$ °C, unless otherwise noted.)

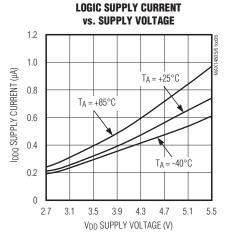




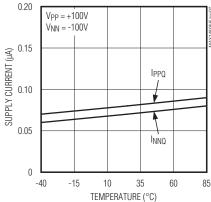




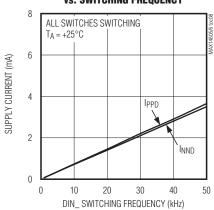




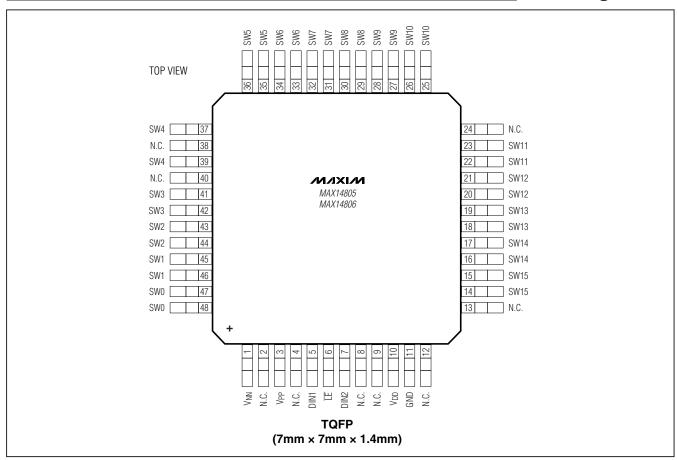
# HIGH-VOLTAGE SUPPLY CURRENT vs. Temperature



## HIGH-VOLTAGE SUPPLY CURRENT vs. SWITCHING FREQUENCY



## **Pin Configuration**



### **Pin Description**

PIN	NAME	FUNCTION
1	VNN	Negative High-Voltage Power Supply. Bypass V <sub>NN</sub> to GND with a 0.1µF or greater ceramic capacitor as close as possible to the device.
2, 4, 8, 9, 12, 13, 24, 38, 40	N.C.	No Connection. Not internally connected.
3	VPP	Positive High-Voltage Power Supply. Bypass Vpp to GND with a 0.1µF or greater ceramic capacitor as close as possible to the device.
5	DIN1	Data Input 1
6	ĪĒ	Active-Low Latch Enable Input. Drive $\overline{\text{LE}}$ low to latch data input. Drive $\overline{\text{LE}}$ high to hold data.
7	DIN2	Data Input 2
10	V <sub>DD</sub>	Digital Power Supply. Bypass V <sub>DD</sub> to GND with a 0.1µF or greater ceramic capacitor as close as possible to the device.
11	GND	Ground
14, 15	SW15	Analog Switch Terminal 15

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## Pin Description (continued)

PIN	NAME	FUNCTION
16, 17	SW14	Analog Switch Terminal 14
18, 19	SW13	Analog Switch Terminal 13
20, 21	SW12	Analog Switch Terminal 12
22, 23	SW11	Analog Switch Terminal 11
25, 26	SW10	Analog Switch Terminal 10
27, 28	SW9	Analog Switch Terminal 9
29, 30	SW8	Analog Switch Terminal 8
31, 32	SW7	Analog Switch Terminal 7
33, 34	SW6	Analog Switch Terminal 6
35, 36	SW5	Analog Switch Terminal 5
37, 39	SW4	Analog Switch Terminal 4
41, 42	SW3	Analog Switch Terminal 3
43, 44	SW2	Analog Switch Terminal 2
45, 46	SW1	Analog Switch Terminal 1
47, 48	SW0	Analog Switch Terminal 0

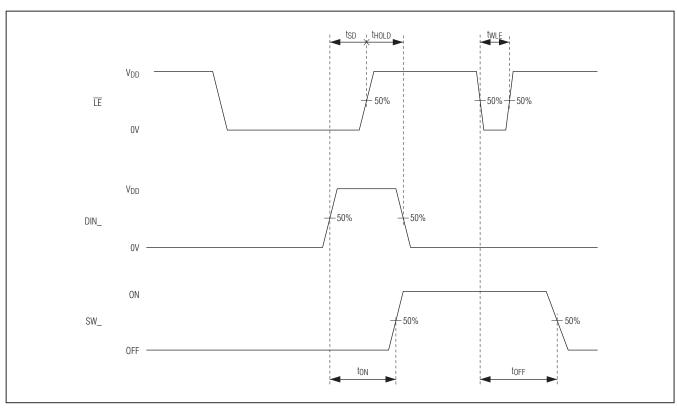


Figure 2. Digital Control (DIN1/DIN2/LE) Timing

**Table 1. Truth Table** 

CONTROL			ANALOG SWITCH			
DIN1	DIN2 <u>LE</u>		SW0-SW7	SW8-SW15		
Low	Low	Low	Off	Off		
High	Low	Low	On	Off		
Low	High	Low	Off	On		
High	High	Low	On	On		
X	X	High	Hold Previous State			

X = Don't care.

### **Detailed Description**

The MAX14805/MAX14806 provide high-voltage switching on 16 channels for ultrasonic imaging. Both devices are ideal for the following applications: bank selection in biplane or triplane ultrasound probes and relays replacement in medical ultrasound systems. The devices utilize 200V process technology to provide 16 high-voltage, low-charge injection SPST switches, controlled by a digital interface.

The MAX14805/MAX14806's output switches are configured as two sets of eight SPST analog switches. The switches are controlled by two input logic controls, DIN1 and DIN2 (respectively for switch 0 to 7 and switch 8 to 15). The MAX14806 features integrated  $40k\Omega$  bleed resistors on each switch terminal that help to reduce voltage buildup in capacitive loads such as piezoelectric elements.

The MAX14805/MAX14806 operate with a wide range of high-voltage supplies, including VPP/VNN = +100V/-100V, +200V/0V, and +40V/-160V. The digital interface operates from a separate VDD supply from +2.7V to +5.5V. Digital inputs DIN1, DIN2, and  $\overline{\text{LE}}$  operate on the VDD supply voltage.

The MAX14805CCM+ is a drop-in replacement for the Supertex HV2631. The MAX14806CCM+ is a drop-in replacement for the Supertex HV2731.

#### **Analog Switch**

The MAX14805/MAX14806 allow a peak-to-peak analog signal range from  $V_{NN}$  to ( $V_{PP}$  - 10V). During power-up and power-down, all analog switch inputs (SW\_) must be unconnected or satisfy  $V_{NN} \leq V_{SW} \leq V_{PP}$ .

#### **High-Voltage Supplies**

The MAX14805/MAX14806 allow a wide range of high-voltage supplies. The devices operate with V<sub>NN</sub> from -160V to 0V and V<sub>PP</sub> from +40V to (V<sub>NN</sub> + 220V). When V<sub>NN</sub> is connected to GND (single-supply applications), the devices operate with V<sub>PP</sub> up to +200V. The V<sub>PP</sub> and V<sub>NN</sub> high-voltage supplies are not required to be symmetrical, but the voltage difference (V<sub>PP</sub> - V<sub>NN</sub>) must not exceed 230V.

#### **Bleed Resistors (MAX14806)**

The MAX14806 features integrated  $40k\Omega$  bleed resistors to discharge capacitive loads such as piezoelectric transducers. Each analog switch terminal is connected to GND with a bleed resistor.

#### Data Input (DIN1/DIN2)

DIN1/DIN2 control the on/off state of the analog switches. DIN1 controls SW0–SW7 and DIN2 controls SW8–SW15 (see Table 1 and Figure 2). DIN1 and DIN2 operate on the V<sub>DD</sub> supply voltage.

### Latch Enable (LE)

Drive  $\overline{\text{LE}}$  logic-low to latch DIN1/DIN2 data input (see Figure 2). Drive  $\overline{\text{LE}}$  logic-high to hold data. The  $\overline{\text{LE}}$  input operates on the V<sub>DD</sub> supply voltage.

### \_Applications Information

For medical ultrasound applications, see Figures 3 and 4.

#### Supply Sequencing and Bypassing

The MAX14805/MAX14806 do not require special sequencing of the VDD, VPP, and VNN supply voltages; however, analog switch inputs must be unconnected or satisfy VNN  $\leq$  VSW\_  $\leq$  VPP during power-up and power-down. Bypass VDD, VPP, and VNN to GND with a 0.1µF ceramic capacitor as close as possible to the device.

## Application Diagram

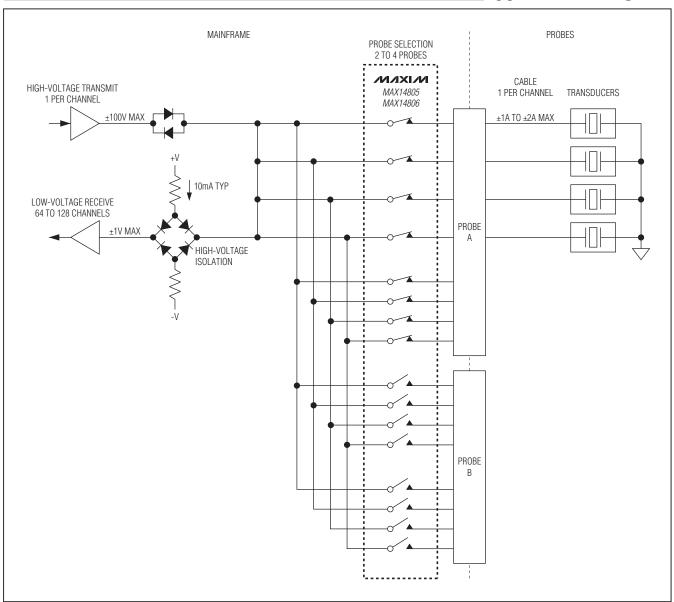


Figure 3. Relay Replacement Application in Medical System

## **Application Diagram (continued)**

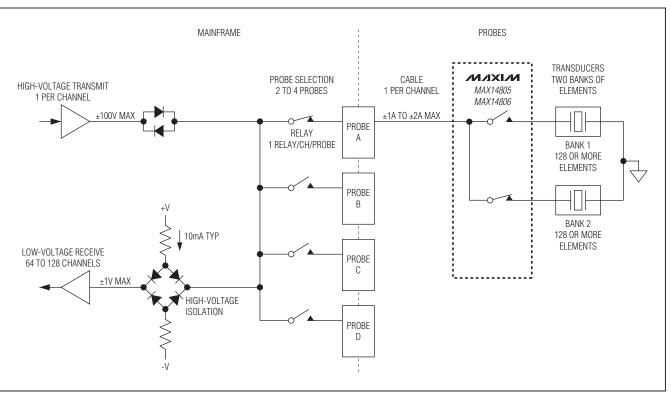
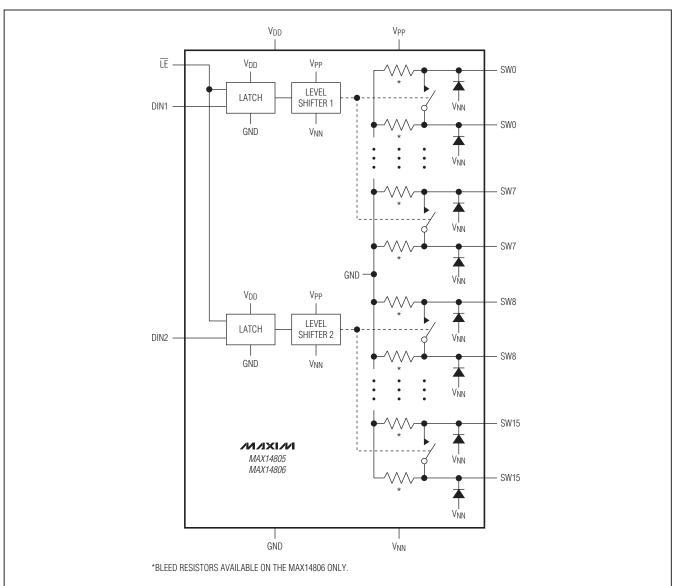


Figure 4. Probe Banks Selection in Biplane or Triplane Probe

### **Functional Diagram**



### **Chip Information**

### Package Information

PROCESS: BICMOS

For the latest package outline information and land patterns, go to <a href="www.maxim-ic.com/packages">www.maxim-ic.com/packages</a>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	
48 TQFP	C48-6	21-0054	

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## **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/10	Initial release	_

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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