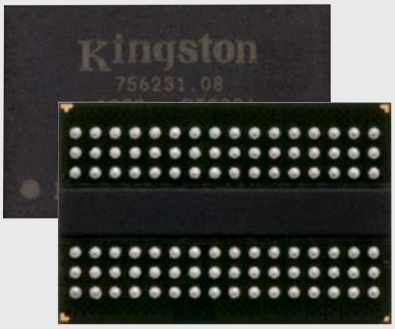
Kingston I-Temp DDR3/3L DRAM for embedded applications

Kingston DDR3/3L

Overview

Ideal for embedded applications, Kingston's I-Temp DRAM meets industrial operating temperature requirements (-40°C~+95°C) which makes it suitable for outdoor and harsh environments. It supports both low (1.35V) and standard (1.5V) voltage for design flexibility.



DDR3/3L Part Numbers and Specifications

I-Temp DDR3/3L PN	Capacity	Description	Package Size	Configuration (words x bits)	Speed	VDD, VDDQ	Operating Temperature
D2516EC4BXGGBI	4Gb	96 ball FBGA DDR3/3L IT	9.0x13.5x1.2	256MX16	1600/1333	1.35V*	-40°C~+95°C
D5128EC4BPGGBUI	4Gb	78 ball FBGA DDR3/3L IT	9.0x10.6x1.2	512Mx8	1600/1333	1.35V*	-40°C~+95°C

*Backward compatible to 1.5V VDD, VDDQ

Key Features

- Double-data-rate architecture: two data transfers per clock cycle
- High-speed data transfer is realized by 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DOS and /DQS) is transmitted/received with data for capturing data at the receiver
- DOS is edge-aligned with data for READS; center-aligned with data for WRITES
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DOS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODD for better signal quality)
  – Synchronous ODT
  – Dynamic CDT
  – Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DO drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- RESET pin for Power-up sequence and reset function
- SRT range: Normal/extended
- Programmable Output driver impedance control