

## NCE N-Channel Enhancement Mode Power MOSFET

### Description

The NCE3080K uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

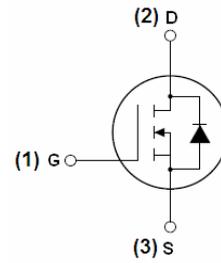
### General Features

- $V_{DS} = 30V, I_D = 80A$   
 $R_{DS(ON)} < 6.5m\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 10m\Omega @ V_{GS} = 5V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

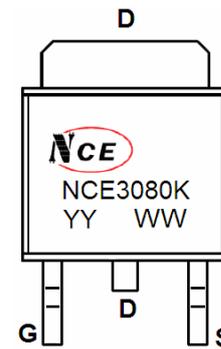
### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

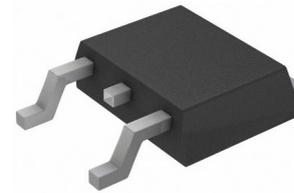
**100% UIS TESTED!**



Schematic diagram



Marking and pin assignment



TO-252-2L top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE3080K	NCE3080K	TO-252-2L	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	80	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	50	A
Pulsed Drain Current	$I_{DM}$	170	A
Maximum Power Dissipation	$P_D$	83	W
Derating factor		0.56	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	$E_{AS}$	306	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	1.8	$^{\circ}\text{C/W}$
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## Electrical Characteristics ( $T_C=25^{\circ}\text{C}$ unless otherwise noted)

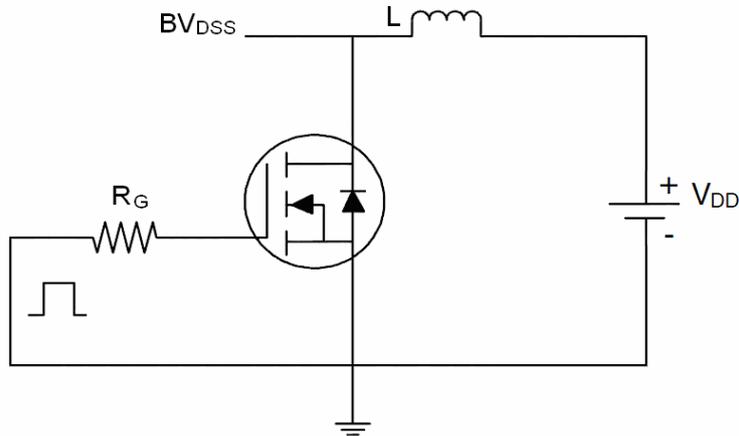
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=30V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.6	3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=30A$	-	5.5	6.5	m $\Omega$
		$V_{GS}=5V, I_D=24A$	-	7.5	10	
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=24A$	20	-	-	S
<b>Dynamic Characteristics (Note4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=15V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	2330	-	PF
Output Capacitance	$C_{oss}$		-	460	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	230	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=30A$ $V_{GS}=10V, R_{GEN}=2.7\Omega$	-	20	-	nS
Turn-on Rise Time	$t_r$		-	15	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	60	-	nS
Turn-Off Fall Time	$t_f$		-	10	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=10V, I_D=30A,$ $V_{GS}=10V$	-	51	-	nC
Gate-Source Charge	$Q_{gs}$		-	14	-	nC
Gate-Drain Charge	$Q_{gd}$		-	11	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=24A$	-	-	1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	80	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = 80A$ $di/dt = 100A/\mu s(\text{Note3})$	-	32	50	nS
Reverse Recovery Charge	$Q_{rr}$		-	12	20	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

### Notes:

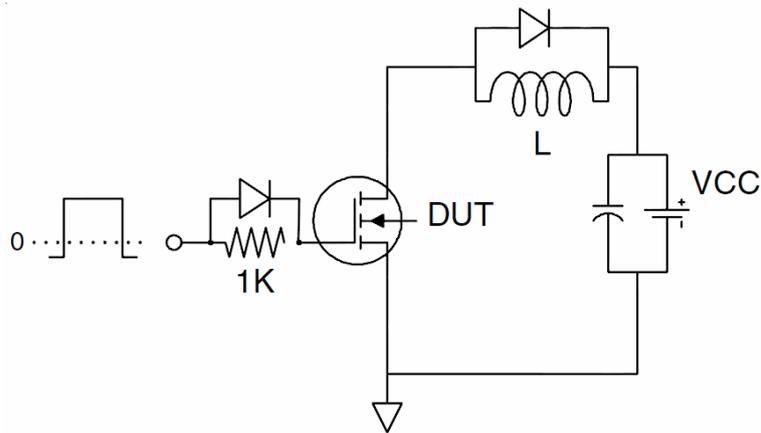
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^{\circ}\text{C}, V_{DD}=15V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega, I_{AS}=35A$

## Test Circuit

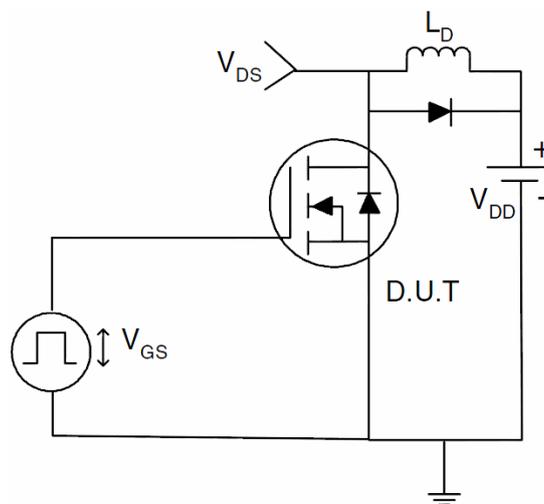
### 1) $E_{AS}$ Test Circuits



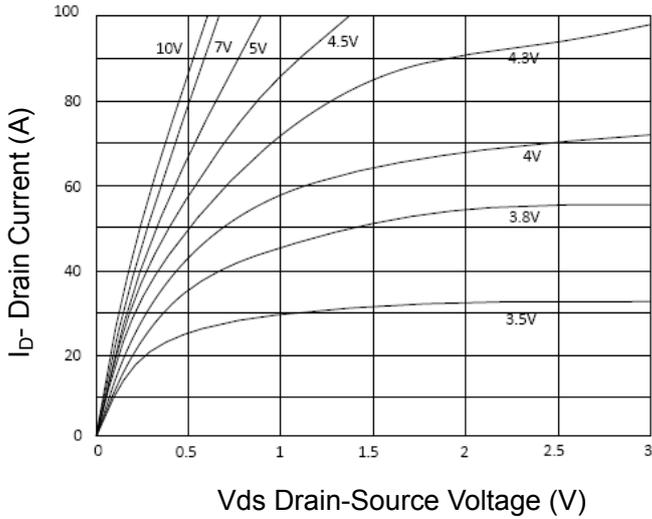
### 2) Gate Charge Test Circuit:



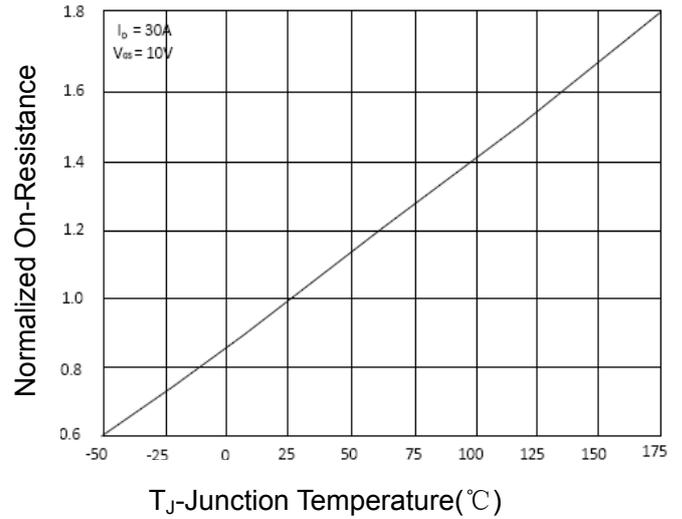
### 3) Switch Time Test Circuit:



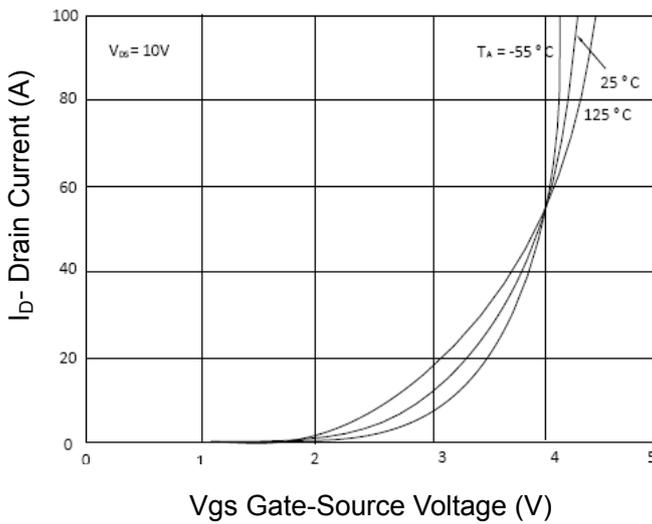
## Typical Electrical and Thermal Characteristics (Curves)



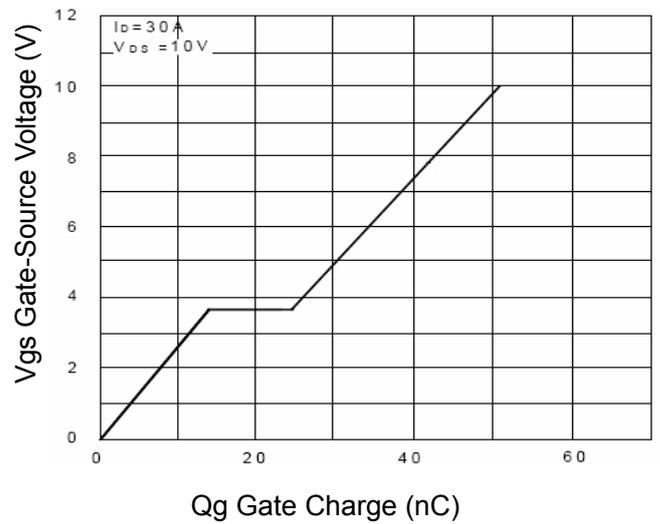
**Figure 1 Output Characteristics**



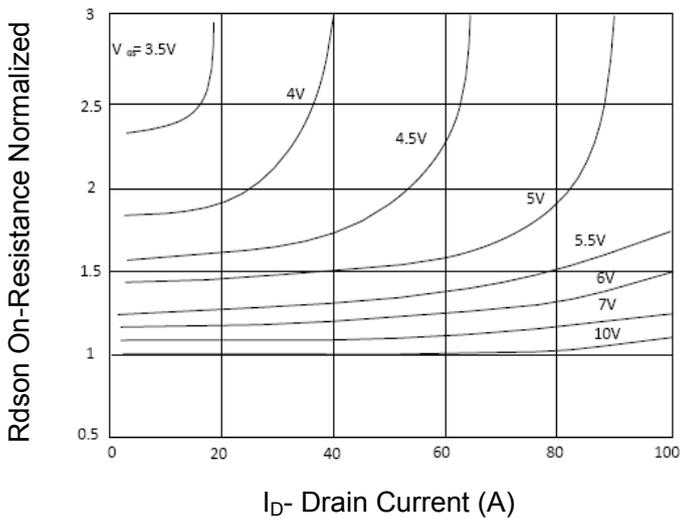
**Figure 4  $R_{dson}$ -Junction Temperature**



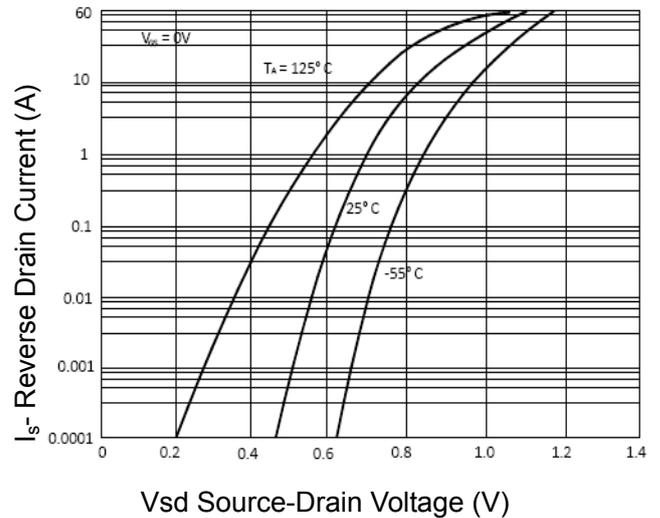
**Figure 2 Transfer Characteristics**



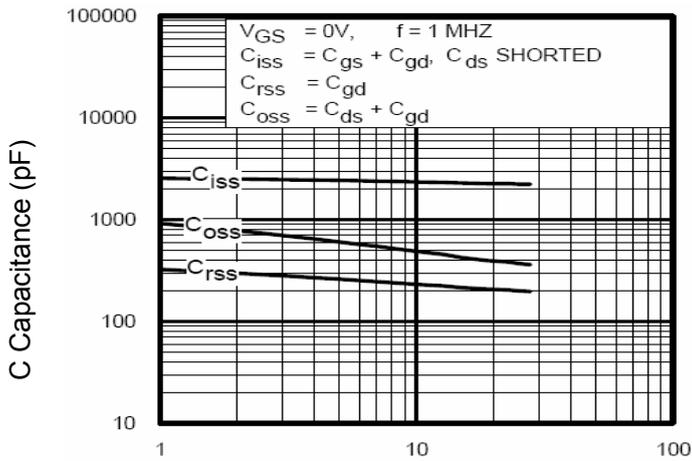
**Figure 5 Gate Charge**



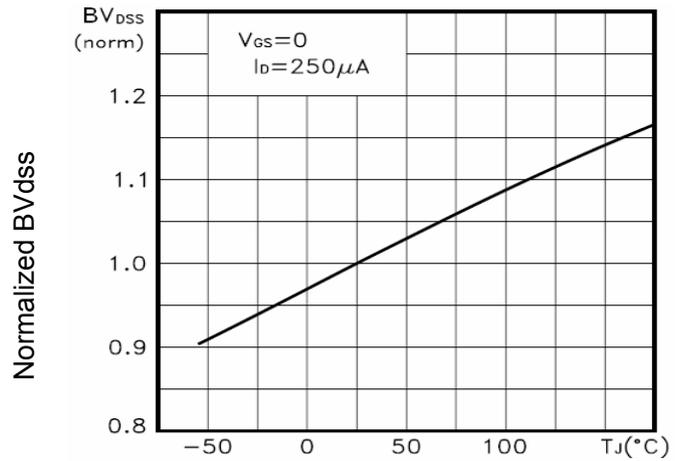
**Figure 3  $R_{dson}$ - Drain Current**



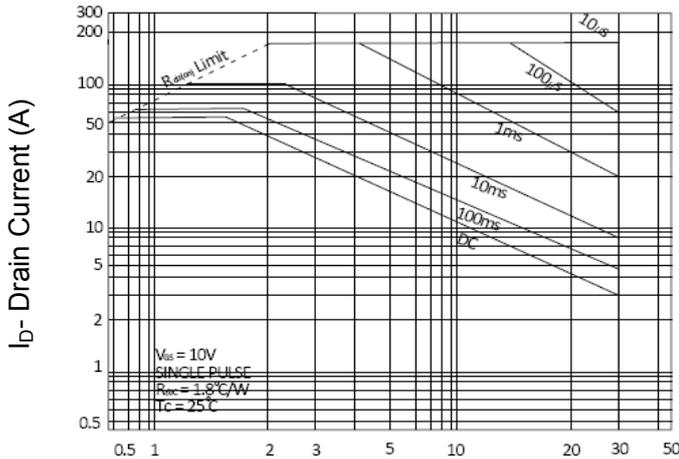
**Figure 6 Source- Drain Diode Forward**



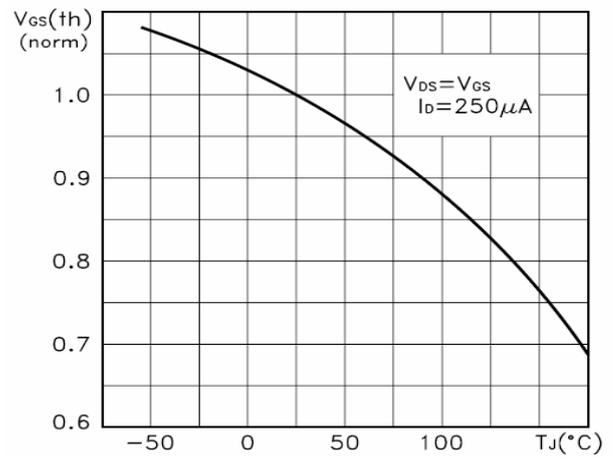
Vds Drain-Source Voltage (V)  
**Figure 7 Capacitance vs Vds**



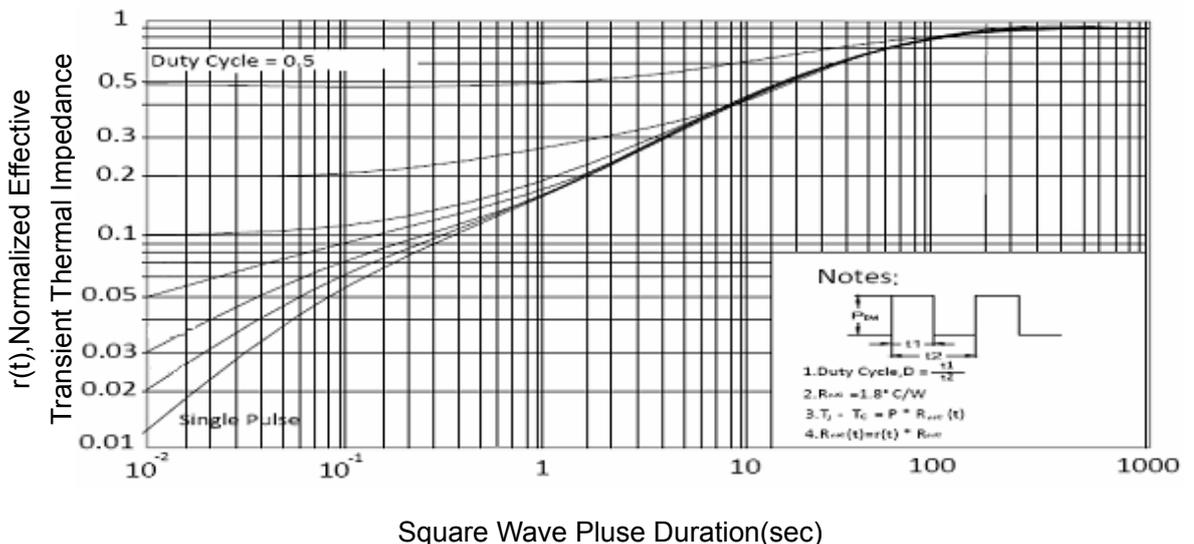
T<sub>J</sub>-Junction Temperature(°C)  
**Figure 9 BV<sub>DSS</sub> vs Junction Temperature**



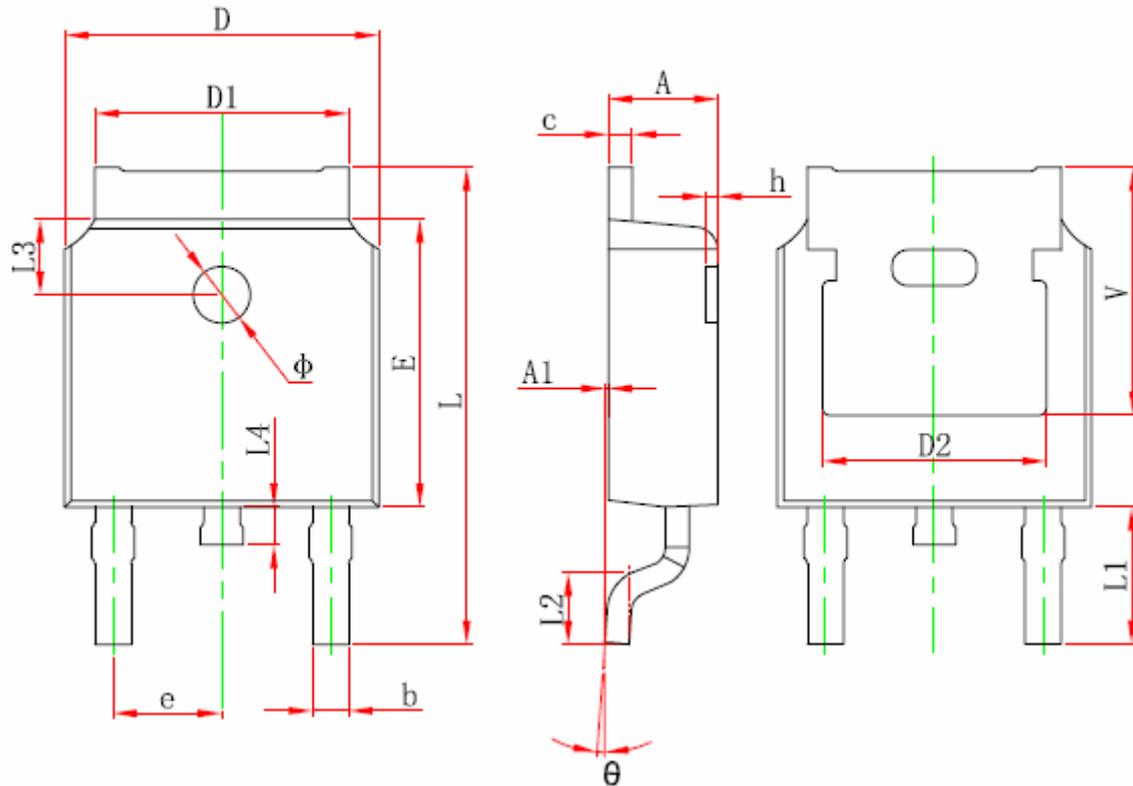
Vds Drain-Source Voltage (V)  
**Figure 8 Safe Operation Area**



T<sub>J</sub>-Junction Temperature(°C)  
**Figure 10 V<sub>GS(th)</sub> vs Junction Temperature**



**Figure 11 Normalized Maximum Transient Thermal Impedance**

**TO-252-2L Package Information**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	

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