

# CDx4HC405x, CDx4HCT405x High-Speed CMOS Logic Analog Multiplexers and Demultiplexers

## 1 Features

- Wide Analog Input Voltage Range:  $\pm 5$ -V Maximum
- Low ON-Resistance
  - 7- $\Omega$  Typical ( $V_{CC} - V_{EE} = 4.5$  V)
  - 40- $\Omega$  Typical ( $V_{CC} - V_{EE} = 9$  V)
- Low Crosstalk Between Switches
- Fast Switching and Propagation Speeds
- Break-Before-Make Switching
- Wide Operating Temperature Range:  
 $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- CD54HC and CD74HC Types
  - Operation Control Voltage: 2 V to 6 V
  - Switch Voltage: 0 V to 10 V
- CD54HCT and CD74HCT Types
  - Operation Control Voltage: 4.5 V to 5.5 V
  - Switch Voltage: 0 V to 10 V
  - Direct LSTTL Input Logic Compatibility  
 $V_{IL} = 0.8$ -V Max,  $V_{IH} = 2$ -V Min
  - CMOS Input Compatibility  
 $I_I \leq 1 \mu\text{A}$  at  $V_{OL}, V_{OH}$
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

## 2 Applications

- Digital Radio
- Signal Gating
- Factory Automation
- Televisions
- Appliances
- Programmable Logic Circuits
- Sensors

### 3 Description

The CDx4HC405x and CDx4HCT405x devices are digitally controlled analog switches that use silicon gate CMOS technology to achieve operating speeds similar to LSTTL with the low-power consumption of standard CMOS integrated circuits.

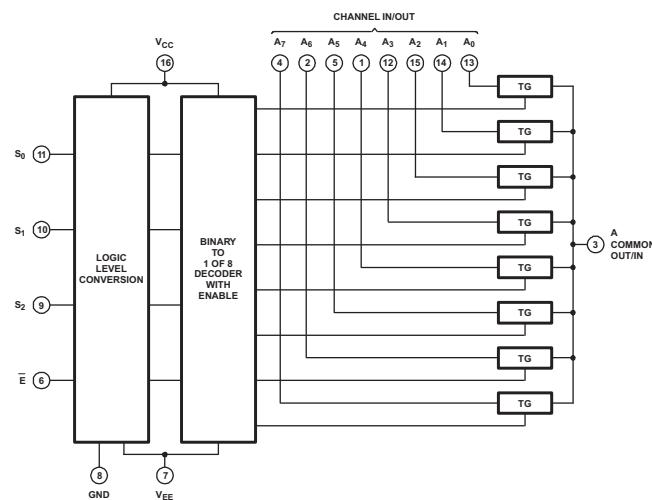
These analog multiplexers and demultiplexers control analog voltages that may vary across the voltage supply range (for example,  $V_{CC}$  to  $V_{EE}$ ). They are bidirectional switches that allow any analog input to be used as an output and vice versa. The switches have low ON resistance and low OFF leakages. In addition, all these devices have an enable control that, when high, disables all switches to their OFF state.

## Device Information<sup>(1)</sup>

DEVICE INFORMATION		
PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD54HCx405xF	CDIP (16)	19.56 mm x 6.92 mm
CD74HCx405xE	PDIP (16)	19.30 mm x 6.35 mm
CD74HCx405xM	SOIC (16)	9.90 mm x 3.91 mm
CD74HCx405xNS	SOP (16)	10.30 mm x 5.30 mm
CD74HCx405xPW	TSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## Functional Diagram of HC4051 and HCT4051



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## 4 Revision History

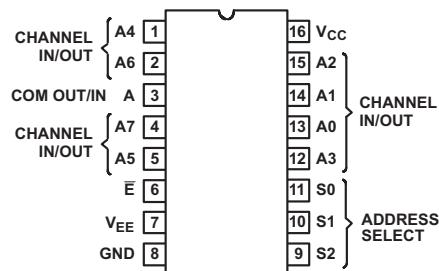
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (February 2011) to Revision K	Page
• Removed <i>Ordering Information</i> table.	1
• Added <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Detailed Description</i> section, <i>Applications and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Added Military Disclaimer to <i>Features</i> list.	1

## 5 Pin Configuration and Functions

**CD54HC4051, CD54HCT4051, CD74HC4051, CD74HCT4051 J, N, D, NS, PW Packages  
16-Pin CDIP, PDIP, SOIC, SO, TSSOP**

Top View

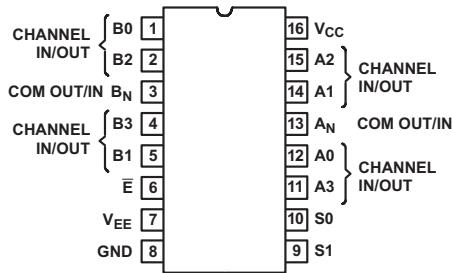


**Pin Functions for CDx4HCx4051B**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CH A4 IN/OUT	I/O	Channel 4 in/out
2	CH A6 IN/OUT	I/O	Channel 6 in/out
3	COM OUT/IN	I/O	Common out/in
4	CH A7 IN/OUT	I/O	Channel 7 in/out
5	CH A5 IN/OUT	I/O	Channel 5 in/out
6	$\bar{E}$	I	Enable Channels (Active Low). See <a href="#">Table 1</a> .
7	$V_{EE}$	—	Negative power input
8	GND	—	Ground
9	S2	I	Channel select 2. See <a href="#">Table 1</a> .
10	S1	I	Channel select 1. See <a href="#">Table 1</a> .
11	S0	I	Channel select 0. See <a href="#">Table 1</a> .
12	CH A3 IN/OUT	I/O	Channel 3 in/out
13	CH A0 IN/OUT	I/O	Channel 0 in/out
14	CH A1 IN/OUT	I/O	Channel 1 in/out
15	CH A2 IN/OUT	I/O	Channel 2 in/out
16	$V_{CC}$	—	Positive power input

CD54HC4052, CD74HC4052, CD74HCT4052 J, N, D, NS, PW Packages  
 16-Pin CDIP, PDIP, SOIC, SO, TSSOP

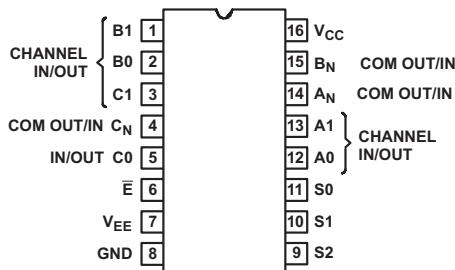
Top View



Pin Functions for CDx4HCx4052B

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CH B0 IN/OUT	I/O	Channel B0 in/out
2	CH B2 IN/OUT	I/O	Channel B2 in/out
3	COM B OUT/IN	I/O	B common out/in
4	CH B3 IN/OUT	I/O	Channel B3 in/out
5	CH B1 IN/OUT	I/O	Channel B1 in/out
6	Ē	I	Enable channels (Active Low). See <a href="#">Table 2</a> .
7	V <sub>EE</sub>	—	Negative power input
8	GND	—	Ground
9	S1	I	Channel select 1. See <a href="#">Table 2</a> .
10	S0	I	Channel select 0. See <a href="#">Table 2</a> .
11	CH A3 IN/OUT	I/O	Channel A3 in/out
12	CH A0 IN/OUT	I/O	Channel A0 in/out
13	COM A IN/OUT	I/O	A common out/in
14	CH A1 IN/OUT	I/O	Channel A1 in/out
15	CH A2 IN/OUT	I/O	Channel A2 in/out
16	V <sub>CC</sub>	—	Positive power input

**CD54HC4053 CD74HC4053 CD74HCT4053 J, N, D, NS, PW Packages  
16-Pin CDIP, PDIP, SOIC, SOP, TSSOP  
TOP VIEW**



**Pin Functions CDx4HCx4053B**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	B1 IN/OUT	I/O	B channel Y in/out
2	B0 IN/OUT	I/O	B channel X in/out
3	C1 IN/OUT	I/O	C channel Y in/out
4	COM C OUT/IN	I/O	C common out/in
5	C0 IN/OUT	I/O	C channel X in/out
6	$\bar{E}$	I	Enable channels (Active Low). See <a href="#">Table 3</a> .
7	$V_{EE}$	—	Negative power input
8	GND	—	Ground
9	S2	I	Channel select 2. See <a href="#">Table 3</a> .
10	S1	I	Channel select 1. See <a href="#">Table 3</a> .
11	S0	I	Channel select 0. See <a href="#">Table 3</a> .
12	A0 IN/OUT	I/O	A channel X in/out
13	A1 IN/OUT	I/O	A channel Y in/out
14	COM A OUT/IN	I/O	A common out/in
15	COM B OUT/IN	I/O	B common out/in
16	$V_{CC}$	—	Positive power input

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC} - V_{EE}$	DC supply voltage		-0.5	10.5	V
$V_{CC}$	DC supply voltage		-0.5	7	V
$V_{EE}$	DC supply voltage		0.5	-7	V
$I_{IK}$	DC input diode current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$		$\pm 20$	mA
$I_{OK}$	DC switch diode current	$V_I < V_{EE} - 0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$		$\pm 20$	mA
	DC switch current <sup>(2)</sup>	$V_I > V_{EE} - 0.5 \text{ V}$ or $V_I < V_{CC} + 0.5 \text{ V}$		$\pm 25$	mA
$I_{CC}$	DC $V_{CC}$ or ground current			$\pm 50$	mA
$I_{EE}$	DC $V_{EE}$ current			-20	mA
$T_{JMAX}$	Maximum junction temperature			150	°C
$T_{LMAX}$	Maximum lead temperature	Soldering 10 s		300	°C
$T_{stg}$	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to GND unless otherwise specified.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	$\pm 500$	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	$\pm 1000$	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage range ( $T_A$ = full package temperature range) <sup>(2)</sup>	CD54 and 74HC types	2	6	V
		CD54 and 74HCT types	4.5	5.5	
$V_{CC} - V_{EE}$	Supply voltage range ( $T_A$ = full package temperature range)	CD54 and 74HC types, CD54 and 74HCT types (see Figure 1)	2	10	V
$V_{EE}$	Supply voltage range ( $T_A$ = full package temperature range) <sup>(3)</sup>	CD54 and 74HC types, CD54 and 74HCT types (see Figure 2)	0	-6	V
$V_I$	DC input control voltage		GND	$V_{CC}$	V
$V_{IS}$	Analog switch I/O voltage		$V_{EE}$	$V_{CC}$	V
$T_A$	Operating temperature		-55	125	°C
$t_r, t_f$	Input rise and fall times	2 V	0	1000	ns
		4.5 V	0	500	
		6 V	0	400	

(1) For maximum reliability, nominal operating conditions must be selected so that operation is always within the ranges specified in the *Recommended Operating Conditions* table.

(2) All voltages referenced to GND unless otherwise specified.

(3) In certain applications, the external load resistor current may include both  $V_{CC}$  and signal line components. To avoid drawing  $V_{CC}$  current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 V (calculated from  $r_{ON}$  values shown in Electrical Specifications table). No  $V_{CC}$  current will flow through  $R_L$  if the switch current flows into terminal 3 on the HC and HCT4051; terminals 3 and 13 on the HC and HCT4052; terminals 4, 14, and 15 on the HC and HCT4053.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		CD74HC4051			UNIT
		N (PDIP)	NS (SO)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	49.0	83.0	107.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	36.3	41.2	42.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	29.0	43.3	52.8	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	21.2	9.2	4.2	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	28.9	43.0	52.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics: HC Devices

PARAMETERS	TEST CONDITIONS					MIN	TYP	MAX	UNIT
	V <sub>IS</sub> (V)	V <sub>I</sub> (V)	V <sub>EE</sub> (V)	V <sub>CC</sub> (V)	T <sub>A</sub>				
V <sub>IH</sub> High-level input voltage				2	25°C	1.5			V
					–40°C to 85°C	1.5			
					–55°C to 125°C	1.5			
				4.5	25°C	3.15			
					–40°C to 85°C	3.15			
					–55°C to 125°C	3.15			
				6	25°C	4.2			
					–40°C to 85°C	4.2			
					–55°C to 125°C	4.2			
V <sub>IL</sub> Low-level input voltage				2	25°C	0.5			V
					–40°C to 85°C	0.5			
					–55°C to 125°C	0.5			
				4.5	25°C	1.35			
					–40°C to 85°C	1.35			
					–55°C to 125°C	1.35			
				6	25°C	1.8			
					–40°C to 85°C	1.8			
					–55°C to 125°C	1.8			

## Electrical Characteristics: HC Devices (continued)

PARAMETERS		TEST CONDITIONS					MIN	TYP	MAX	UNIT
		$V_{IS}$ (V)	$V_I$ (V)	$V_{EE}$ (V)	$V_{CC}$ (V)	$T_A$				
$r_{ON}$	ON resistance  $I_O = 1 \text{ mA}$ See Figure 21	$V_{CC}$ or $V_{EE}$	$V_{IL}$ or $V_{IH}$	0	4.5	25°C	70	160		$\Omega$
						–40°C to 85°C		200		
						–55°C to 125°C		240		
				0	6	25°C	60	140		
						–40°C to 85°C		175		
						–55°C to 125°C		210		
				–4.5	4.5	25°C	40	120		
						–40°C to 85°C		150		
		$V_{CC}$ to $V_{EE}$	$V_{IL}$ or $V_{IH}$			–55°C to 125°C		180		
			0	4.5	25°C	90	180			
					–40°C to 85°C		225			
					–55°C to 125°C		270			
			0	6	25°C	80	160			
					–40°C to 85°C		200			
					–55°C to 125°C		240			
			–4.5	4.5	25°C	45	130			
					–40°C to 85°C		162			
					–55°C to 125°C		195			
$\Delta r_{ON}$	Maximum ON resistance between any two channels			0	4.5	25°C	10			$\Omega$
				0	6	25°C	8.5			
				–4.5	4.5	25°C	5			

## Electrical Characteristics: HC Devices (continued)

PARAMETERS		TEST CONDITIONS					MIN	TYP	MAX	UNIT							
		$V_{IS}$ (V)	$V_I$ (V)	$V_{EE}$ (V)	$V_{CC}$ (V)	$T_A$											
$I_Z$ Switch ON/OFF leakage current	1 and 2 channels	For switch OFF: When $V_{IS} = V_{CC}$ , $V_{OS} = V_{EE}$ ; When $V_{IS} = V_{EE}$ , $V_{OS} = V_{CC}$ . For switch ON: All applicable combinations of $V_{IS}$ and $V_{OS}$ voltage levels	$V_{IL}$ or $V_{IH}$	0	6	25°C	$\pm 0.1$										
						-40°C to 85°C	$\pm 1$										
						-55°C to 125°C	$\pm 1$										
	4053			-5	5	25°C	$\pm 0.1$										
						-40°C to 85°C	$\pm 1$										
						-55°C to 125°C	$\pm 1$										
	4 channels			0	6	25°C	$\pm 0.1$										
						-40°C to 85°C	$\pm 1$										
						-55°C to 125°C	$\pm 1$										
	4052			-5	5	25°C	$\pm 0.2$										
						-40°C to 85°C	$\pm 2$										
						-55°C to 125°C	$\pm 2$										
	8 channels			0	6	25°C	$\pm 0.2$										
						-40°C to 85°C	$\pm 2$										
						-55°C to 125°C	$\pm 2$										
	4051			-5	5	25°C	$\pm 0.4$										
						-40°C to 85°C	$\pm 4$										
						-55°C to 125°C	$\pm 4$										
$I_{IL}$ Control input leakage current			$V_{CC}$ or GND	0	6	25°C	$\pm 0.1$										
						-40°C to 85°C	$\pm 1$										
						-55°C to 125°C	$\pm 1$										
$I_{CC}$ Quiescent device current	$I_O = 0$	When $V_{IS} = V_{EE}$ , $V_{OS} = V_{CC}$	$V_{CC}$ or GND	0	6	25°C	8										
						-40°C to 85°C	80										
						-55°C to 125°C	160										
		When $V_{IS} = V_{CC}$ , $V_{OS} = V_{EE}$		-5	5	25°C	16										
						-40°C to 85°C	160										
						-55°C to 125°C	320										

## 6.6 Electrical Characteristics: HCT Devices

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
		$V_{IS}$ (V)	$V_I$ (V)	$V_{EE}$ (V)	$V_{CC}$ (V)	$T_A$				
$V_{IH}$	High-level input voltage				4.5 to 5.5	25°C	2			V
						–40°C to 85°C	2			
						–55°C to 125°C	2			
$V_{IL}$	Low-level input voltage				4.5 to 5.5	25°C		0.8		V
						–40°C to 85°C		0.8		
						–55°C to 125°C		0.8		
$r_{ON}$	$I_O = 1 \text{ mA}$ See Figure 6	$V_{CC}$ or $V_{EE}$	$V_{IL}$ or $V_{IH}$	0	4.5	25°C	70	160		$\Omega$
						–40°C to 85°C		200		
						–55°C to 125°C		240		
				–4.5	4.5	25°C	40	120		
						–40°C to 85°C		150		
						–55°C to 125°C		180		
		$V_{CC}$ to $V_{EE}$	$V_{IL}$ or $V_{IH}$	0	4.5	25°C	90	180		
						–40°C to 85°C		225		
						–55°C to 125°C		270		
				–4.5	4.5	25°C	45	130		
						–40°C to 85°C		162		
						–55°C to 125°C		195		
$\Delta r_{ON}$	Maximum ON resistance between any two channels			0	4.5	25°C	10			$\Omega$
				–4.5	4.5	25°C	5			

## Electrical Characteristics: HCT Devices (continued)

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT		
		$V_{IS}$ (V)	$V_I$ (V)	$V_{EE}$ (V)	$V_{CC}$ (V)	$T_A$						
$I_Z$ Switch ON/OFF leakage current	1 and 2 channels	For switch OFF: When $V_{IS} = V_{CC}$ , $V_{OS} = V_{EE}$ ; When $V_{IS} = V_{EE}$ , $V_{OS} = V_{CC}$ For switch ON: All applicable combinations of $V_{IS}$ and $V_{OS}$ voltage levels	$V_{IL}$ or $V_{IH}$	0	6	25°C			±0.1	µA		
						–40°C to 85°C			±1			
	4053					–55°C to 125°C			±1			
	–5			5	25°C			±0.1				
					–40°C to 85°C			±1				
					4 channels						–55°C to 125°C	
	0			6	25°C			±0.1				
					–40°C to 85°C			±1				
					4052						–55°C to 125°C	
	–5			5	25°C			±0.2				
					–40°C to 85°C			±2				
					8 channels						–55°C to 125°C	
	0			6	25°C			±0.2				
					–40°C to 85°C			±2				
					4051						–55°C to 125°C	
	–5			5	25°C			±0.4				
					–40°C to 85°C			±4				
					–55°C to 125°C			±4				
$I_{IL}$ Control input leakage current		See <sup>(1)</sup>	5.5	25°C			±0.1			µA		
				–40°C to 85°C				±1				
				–55°C to 125°C				±1				
$I_{CC}$ Quiescent device current	$I_O = 0$	When $V_{IS} = V_{EE}$ , $V_{OS} = V_{CC}$	$V_{CC}$ or GND	0	5.5	25°C			8	µA		
						–40°C to 85°C			80			
						–55°C to 125°C			160			
		When $V_{IS} = V_{CC}$ , $V_{OS} = V_{EE}$		–4.5	5.5	25°C			16			
						–40°C to 85°C			160			
						–55°C to 125°C			320			
$\Delta I_{CC}$ Additional quiescent device current per input pin: 1 unit load <sup>(2)</sup>	$\Delta I_{CC}$ <sup>(2)</sup>	$V_{CC} - 2.1$	4.5 to 5.5	25°C			100	360		µA		
				–40°C to 85°C				450				
				–55°C to 125°C				490				

(1) Any voltage between  $V_{CC}$  and GND.

(2) For dual-supply systems, theoretical worst-case ( $V_I = 2.4$  V,  $V_{CC} = 5.5$  V) specification is 1.8 mA.

## 6.7 Switching Characteristics, $V_{CC} = 5$ V

$V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ , input  $t_r, t_f = 6$  ns

PARAMETER	TEST CONDITIONS	$C_L$ (pF)	MIN	TYP	MAX	UNIT
$t_{PHL}, t_{PLH}$	Switch IN to OUT	15	CDx4HC4051	4	4	ns
			CDx4HCT4051	4	4	
			CDx4HC4052	4	4	
			CDx4HCT4052	4	4	
			CDx4HC4053	4	4	
			CDx4HCT4053	4	4	
$t_{PHZ}, t_{PLZ}$	Propagation delay	15	CDx4HC4051	19	19	ns
			CDx4HCT4051	19	19	
			CDx4HC4052	21	21	
			CDx4HCT4052	21	21	
			CDx4HC4053	18	18	
			CDx4HCT4053	18	18	
$t_{PZH}, t_{PZL}$	Switch turn-on (S or $\bar{E}$ )	15	CDx4HC4051	19	19	ns
			CDx4HCT4051	23	23	
			CDx4HC4052	27	27	
			CDx4HCT4052	29	29	
			CDx4HC4053	18	18	
			CDx4HCT4053	20	20	
$C_{PD}$	Power dissipation capacitance <sup>(1)</sup>		CDx4HC4051	50	50	pF
			CDx4HCT4051	52	52	
			CDx4HC4052	74	74	
			CDx4HCT4052	76	76	
			CDx4HC4053	38	38	
			CDx4HCT4053	42	42	

(1)  $C_{PD}$  is used to determine the dynamic power consumption, per package.  $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L + C_S) V_{CC}^2 f_O$ ,  $f_O$  = output frequency,  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $C_S$  = switch capacitance,  $V_{CC}$  = supply voltage

## 6.8 Switching Characteristics, $C_L = 50 \text{ pF}$

 $C_L = 50 \text{ pF}$ , input  $t_r, t_f = 6 \text{ ns}$ 

PARAMETER		$V_{EE}$ (V)	$V_{CC}$ (V)	TEST CONDITIONS		MIN	MAX	UNIT
$t_{PLH}, t_{PHL}$	Propagation delay, switch in to out	0	2	$T_A = 25^\circ\text{C}$	HC	60		ns
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	75		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	90		
		0	4.5	$T_A = 25^\circ\text{C}$	HC, HCT	12		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC, HCT	15		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC, HCT	18		
		0	6	$T_A = 25^\circ\text{C}$	HC	10		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	13		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	15		
		-4.5	4.5	$T_A = 25^\circ\text{C}$	HC, HCT	8		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC, HCT	10		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC, HCT	12		
$t_{PHZ}, t_{PLZ}$	Maximum switch turn OFF delay from S or E to switch output	0	2	$T_A = 25^\circ\text{C}$	HC	225		ns
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	280		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	340		
		0	4.5	$T_A = 25^\circ\text{C}$	HC, HCT	45		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC, HCT	56		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC, HCT	68		
		0	6	$T_A = 25^\circ\text{C}$	HC	38		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	48		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	57		
		-4.5	4.5	$T_A = 25^\circ\text{C}$	HC, HCT	32		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC, HCT	40		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC, HCT	48		
$t_{PHZ}, t_{PLZ}$	Maximum switch turn OFF delay from S or E to switch output	0	2	$T_A = 25^\circ\text{C}$	HC	250		ns
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	315		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	375		
		0	4.5	$T_A = 25^\circ\text{C}$	HC, HCT	50		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC, HCT	63		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC, HCT	75		
		0	6	$T_A = 25^\circ\text{C}$	HC	43		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	54		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	65		
		-4.5	4.5	$T_A = 25^\circ\text{C}$	HC	38		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HCT	38		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	48		
				$T_A = 25^\circ\text{C}$	HCT	48		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	57		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HCT	57		

## Switching Characteristics, $C_L = 50 \text{ pF}$ (continued)

$C_L = 50 \text{ pF}$ , input  $t_r, t_f = 6 \text{ ns}$

PARAMETER		$V_{EE}$ (V)	$V_{CC}$ (V)	TEST CONDITIONS		MIN	MAX	UNIT
$t_{PHZ}, t_{PLZ}$ Maximum switch turn OFF delay from S or $\bar{E}$ to switch output	4053	0	2	$T_A = 25^\circ\text{C}$	HC	210		ns
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	265		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	315		
		0	4.5	$T_A = 25^\circ\text{C}$	HC	42		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HCT	44		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	53		
				$T_A = 25^\circ\text{C}$	HCT	53		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	63		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HCT	66		
		0	6	$T_A = 25^\circ\text{C}$	HC	36		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	45		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	54		
		-4.5	4.5	$T_A = 25^\circ\text{C}$	HC	29		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HCT	31		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	36		
				$T_A = 25^\circ\text{C}$	HCT	39		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	44		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HCT	47		
$t_{PZL}, t_{PZH}$ Maximum switch turn ON delay from S or $\bar{E}$ to switch output	4051	0	2	$T_A = 25^\circ\text{C}$	HC	225		ns
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	280		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	340		
		0	4.5	$T_A = 25^\circ\text{C}$	HC	45		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HCT	55		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	56		
				$T_A = 25^\circ\text{C}$	HCT	69		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	68		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HCT	83		
		0	6	$T_A = 25^\circ\text{C}$	HC	38		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	48		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	57		
		-4.5	4.5	$T_A = 25^\circ\text{C}$	HC	32		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HCT	39		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	40		
				$T_A = 25^\circ\text{C}$	HCT	49		
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	48		
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HCT	59		

## Switching Characteristics, $C_L = 50 \text{ pF}$ (continued)

 $C_L = 50 \text{ pF}$ , input  $t_r, t_f = 6 \text{ ns}$ 

PARAMETER		$V_{EE}$ (V)	$V_{CC}$ (V)	TEST CONDITIONS		MIN	MAX	UNIT	
$t_{PZL}, t_{PZH}$ Maximum switch turn ON delay from S or $\bar{E}$ to switch output	4052	0	2	$T_A = 25^\circ\text{C}$	HC	325		ns	
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	405			
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	490			
		0	4.5	$T_A = 25^\circ\text{C}$	HC	65			
					HCT	70			
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	81			
					HCT	68			
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	98			
					HCT	105			
		0	6	$T_A = 25^\circ\text{C}$	HC	55			
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	69			
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	83			
		-4.5	4.5	$T_A = 25^\circ\text{C}$	HC	46			
					HCT	48			
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	58			
					HCT	60			
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	69			
					HCT	72			
$t_{PZL}, t_{PZH}$ Maximum switch turn ON delay from S or $\bar{E}$ to switch output	4053	0	2	$T_A = 25^\circ\text{C}$	HC	220		ns	
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	275			
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	330			
		0	4.5	$T_A = 25^\circ\text{C}$	HC	44			
					HCT	48			
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	55			
					HCT	60			
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	66			
					HCT	72			
		0	6	$T_A = 25^\circ\text{C}$	HC	37			
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	47			
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	56			
		-4.5	4.5	$T_A = 25^\circ\text{C}$	HC	31			
					HCT	34			
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC	39			
					HCT	43			
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC	47			
					HCT	51			
$C_I$ Input (control) capacitance				$T_A = 25^\circ\text{C}$	HC, HCT	10		pF	
				$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$	HC, HCT	10			
				$T_A = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$	HC, HCT	10			

## 6.9 Analog Channel Specifications

Typical values at  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	HC, HCT TYPES	$V_{EE}$ (V)	$V_{CC}$ (V)	TYP	UNIT
$C_I$	Switch input capacitance	All			5	pF
$C_{COM}$	Common output capacitance	4051			25	pF
		4052			12	
		4053			8	
$f_{MAX}$	Minimum switch frequency response at $-3\text{ dB}$ (see Figure 3, Figure 5, and Figure 7)	4051	-2.25	2.25	145	MHz
		4052			165	
		4053			200	
		4051	-4.5	4.5	180	
		4052			185	
		4053			200	
Sine-wave distortion	See Figure 12	All	-2.25%	2.25%	0.035%	
		All	-4.5%	4.5%	0.018%	
Switch OFF signal feedthrough (see Figure 4, Figure 6, and Figure 8)	See Figure 14 <sup>(2)(3)</sup>	4051	-2.25	2.25	-73	dB
		4052			-65	
		4053			-64	
		4051	-4.5	4.5	-75	
		4052			-67	
		4053			-66	

(1) Adjust input voltage to obtain 0 dBm at  $V_{OS}$  for  $f_{IN} = 1\text{ MHz}$ .

(2)  $V_{IS}$  is centered at  $(V_{CC} - V_{EE}) / 2$ .

(3) Adjust input for 0 dBm.

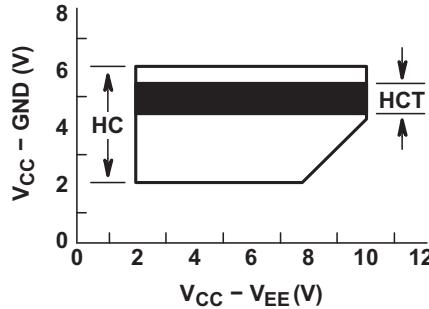


Figure 1. Recommended Operating Area as a Function of  $(V_{CC} - V_{EE})$

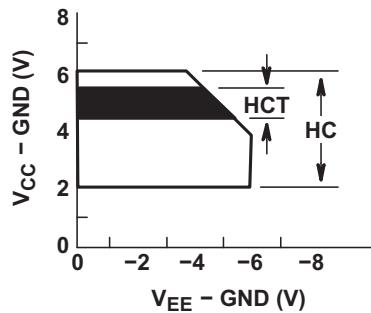


Figure 2. Recommended Operating Area as a Function of  $(V_{EE} - GND)$

## 6.10 Typical Characteristics

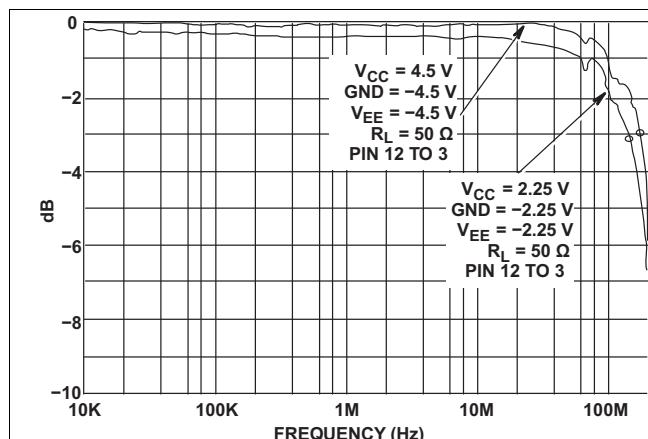


Figure 3. Channel ON Bandwidth  
(HC and HCT4051)

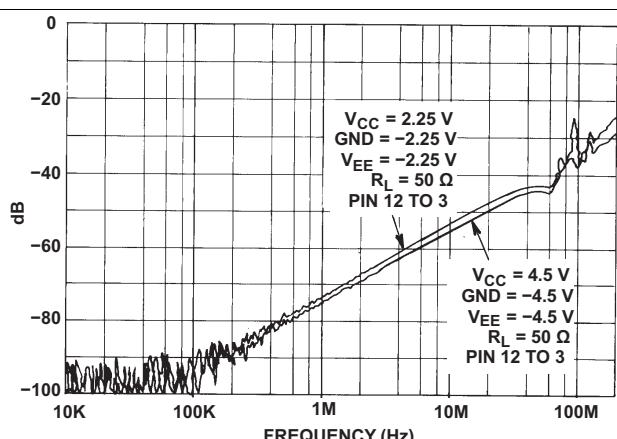


Figure 4. Channel OFF Feedthrough  
(HC and HCT4051)

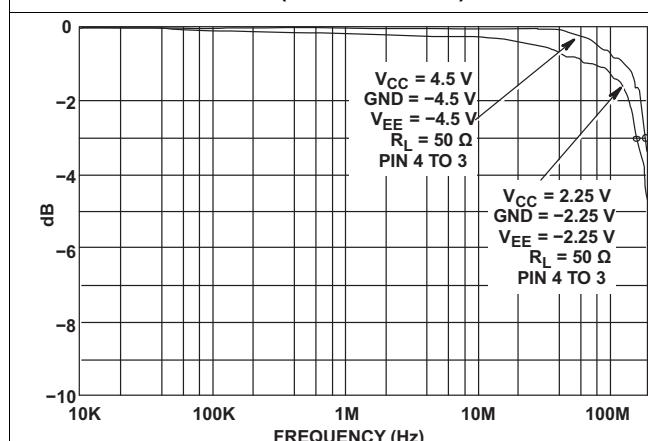


Figure 5. Channel ON Bandwidth  
(HC and HCT4052)

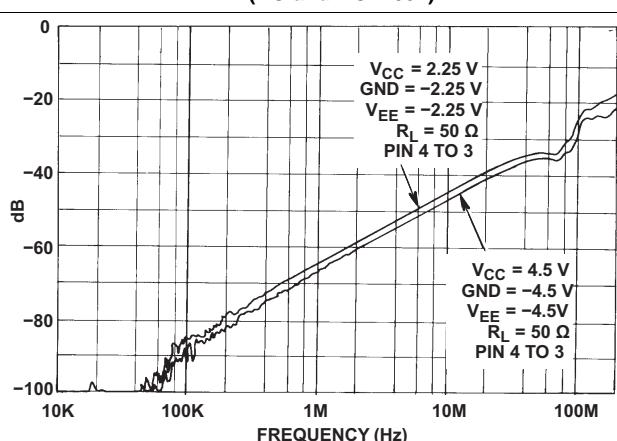


Figure 6. Channel OFF Feedthrough  
(HC and HCT4052)

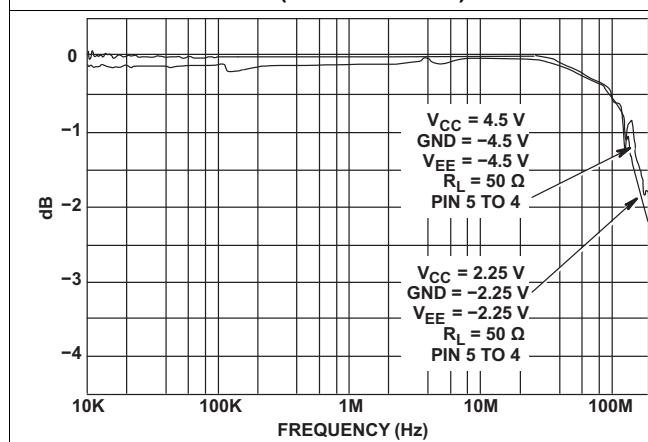


Figure 7. Channel ON Bandwidth  
(HC and HCT4053)

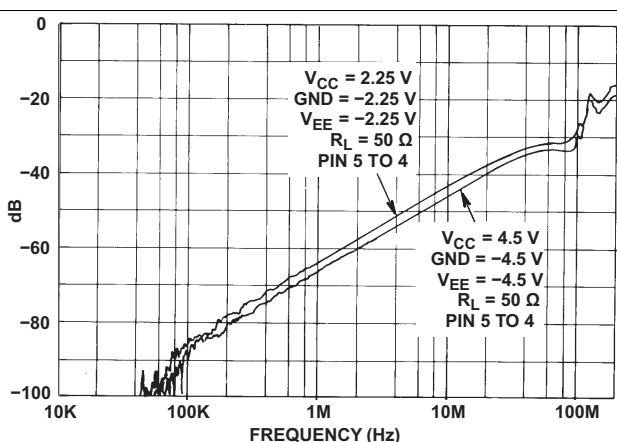
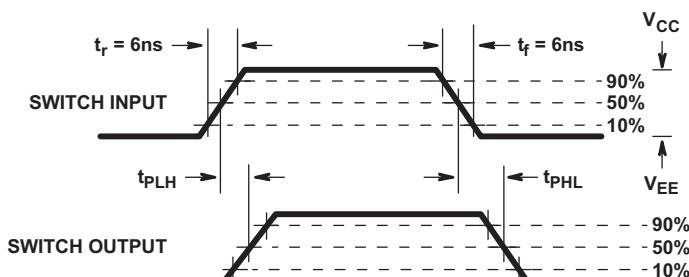
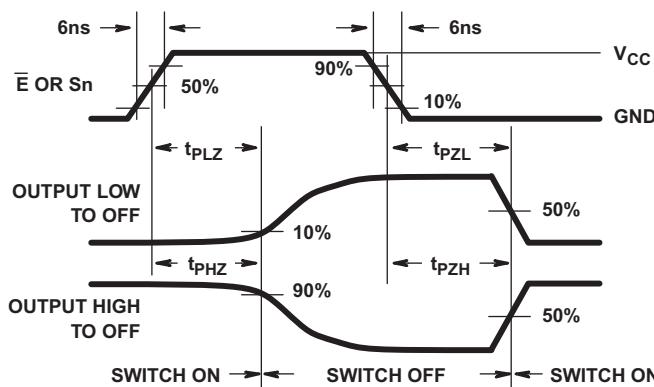


Figure 8. Channel OFF Feedthrough  
(HC and HCT4053)

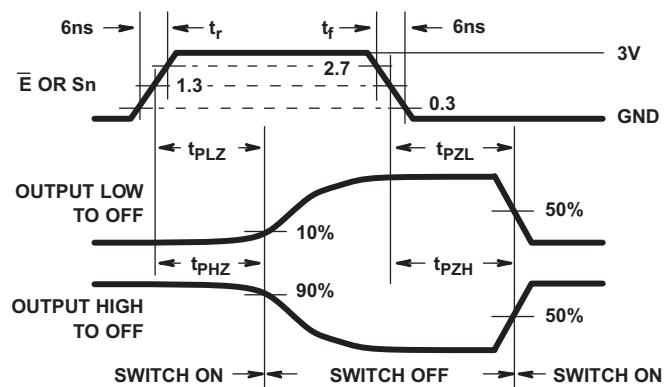
## 7 Parameter Measurement Information



(FIGURE A)



(FIGURE B) HC TYPES



(FIGURE C) HCT TYPES

Figure 9. Switch Propagation Delay, Turn-On, Turn-Off Times

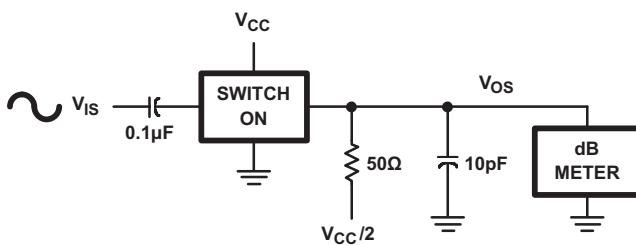


Figure 10. Frequency Response Test Circuit

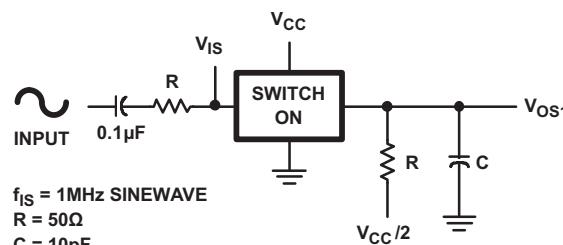


Figure 11. Crosstalk Between Two Switches Test Circuit

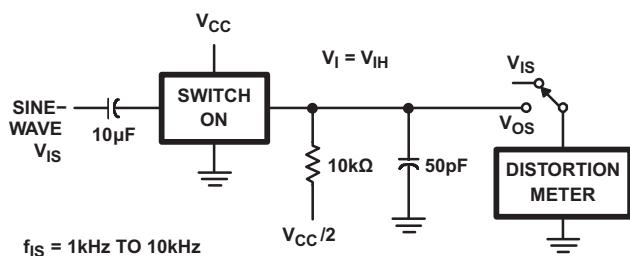


Figure 12. 1/4Sine-Wave Distortion Test Circuit

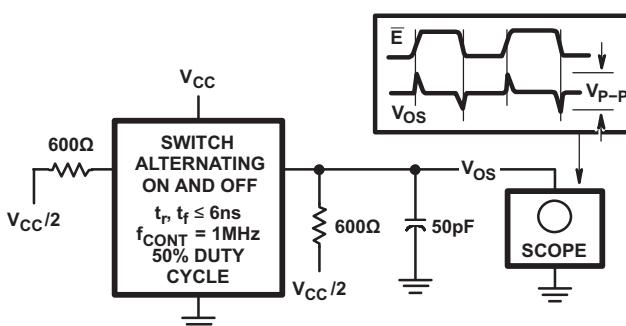


Figure 13. Control to Switch Feedthrough Noise Test Circuit

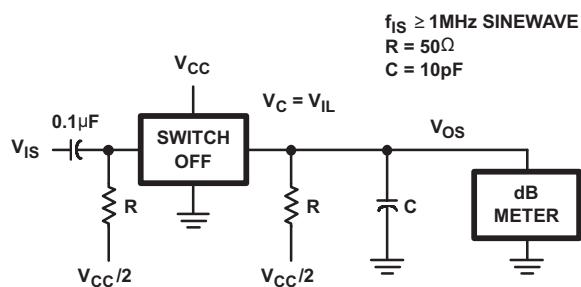


Figure 14. Switch OFF Signal Feedthrough

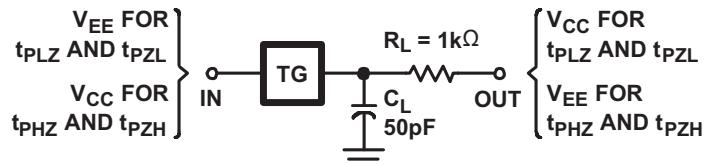


Figure 15. Switch ON/OFF Propagation Delay Test Circuit

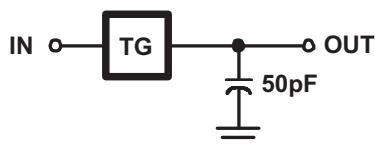


Figure 16. Switch In to Switch Out Propagation Delay Test Circuit

## 8 Detailed Description

### 8.1 Overview

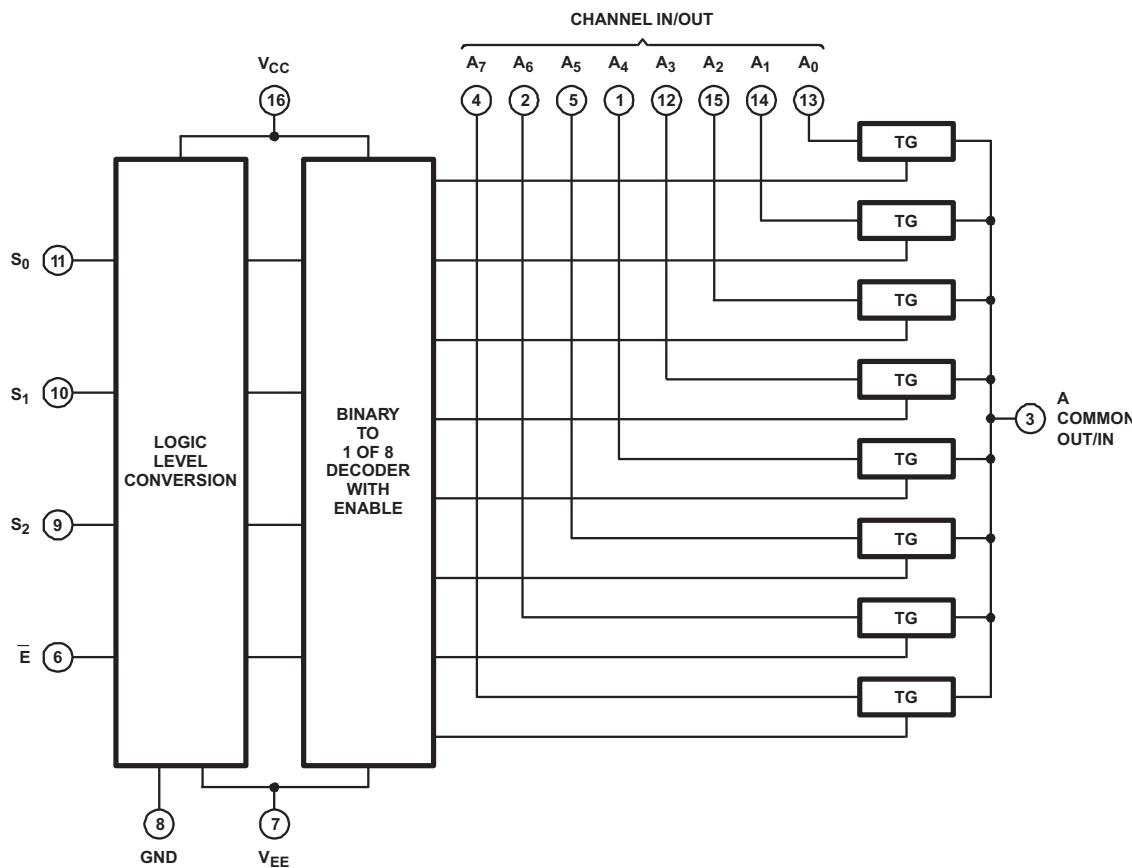
The CDx4HCx4051 devices are a single 8-channel multiplexer having three binary control inputs,  $S_0$ ,  $S_1$ , and  $S_2$  and an ENABLE input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CDx4HCx4052 devices are a differential 4-channel multiplexer having two binary control inputs,  $S_0$  and  $S_1$ , and an ENABLE input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CDx4HCx4053 devices are a triple 2-channel multiplexer having three separate digital control inputs,  $S_0$ ,  $S_1$ , and  $S_2$  and an ENABLE input. Each control input selects one of a pair of channels that are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the CHANNEL IN/OUT terminals are the outputs and the COMMON OUT/IN terminals are the inputs.

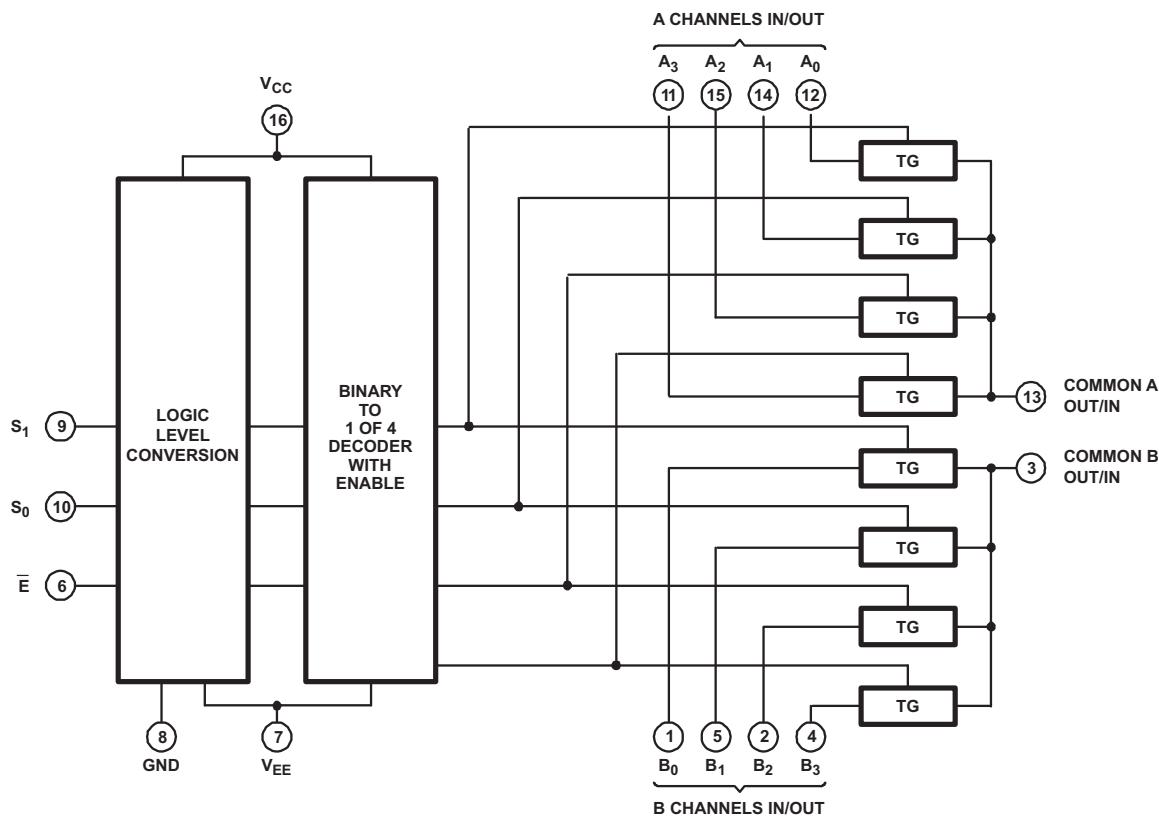
### 8.2 Functional Block Diagrams



All inputs are protected by standard CMOS protection network.

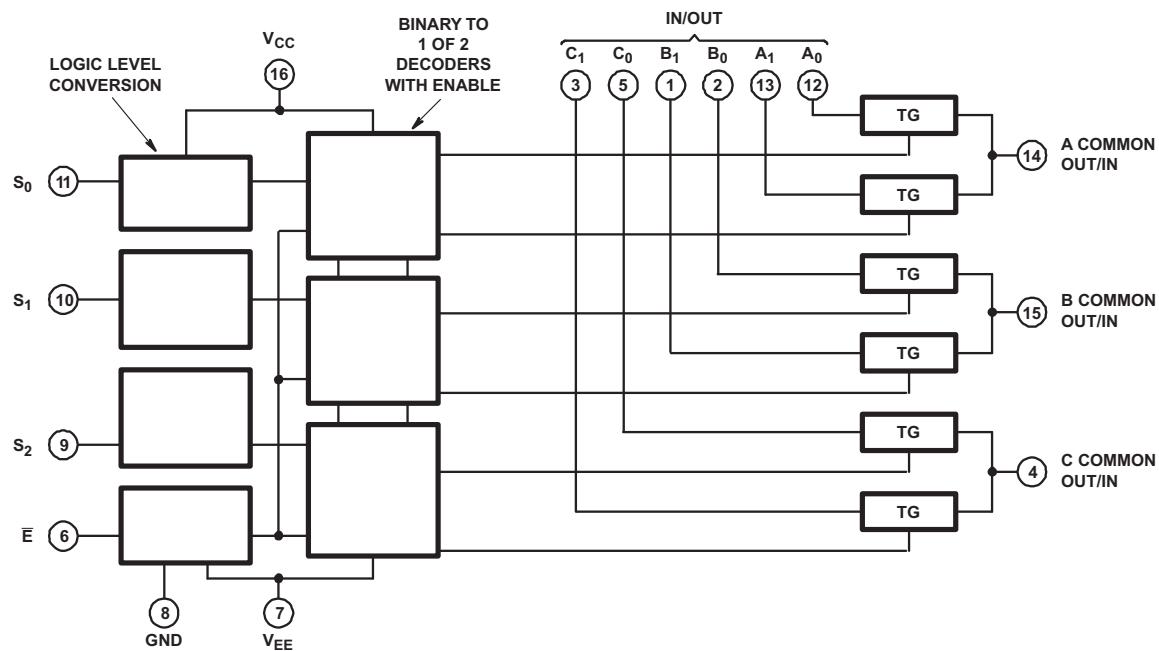
Figure 17. CDx4HCx4051 Functional Block Diagram

## Functional Block Diagrams (continued)



All inputs are protected by standard CMOS protection network.

**Figure 18. CDx4HCx4052 Functional Block Diagram**



All inputs are protected by standard CMOS protection network.

**Figure 19. CDx4HCx4053 Functional Block Diagram**

## 8.3 Feature Description

The CDx4HCx405x line of multiplexers and demultiplexers can accept a wide range of analog signal levels from  $-5$  to  $+5$  V. They have low ON resistance, typically  $70\text{-}\Omega$  for  $V_{CC} - V_{EE} = 4.5$  V and  $40\text{-}\Omega$  for  $V_C - V_{EE} = 4.5$  V, which allows for very little signal loss through the switch.

Binary address decoding on chip makes channel selection easy. When channels are changed, a break-before-make system eliminates channel overlap.

## 8.4 Device Functional Modes

**Table 1. CD54HC4051, CD74HC4051, CD54HCT4051, CD74HCT4051 Function Table<sup>(1)</sup>**

ENABLE	INPUT STATES			ON CHANNEL
	$S_2$	$S_1$	$S_0$	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

(1) X = Don't care

**Table 2. CD54HC4052, CD74HC4052, CD54HCT4052, CD74HCT4052 Function Table<sup>(1)</sup>**

ENABLE	INPUT STATES		ON CHANNELS
	$S_1$	$S_0$	
L	L	L	A0, B0
L	L	H	A1, B1
L	H	L	A2, B2
L	H	H	A3, B3
H	X	X	None

(1) X = Don't care

**Table 3. CD54HC4053, CD74HC4053, CD54HCT4053, CD74HCT4053 Function Table<sup>(1)</sup>**

ENABLE	INPUT STATES			ON CHANNELS
	$S_2$	$S_1$	$S_0$	
L	L	L	L	C0, B0, A0
L	L	L	H	C0, B0, A1
L	L	H	L	C0, B1, A0
L	L	H	H	C0, B1, A1
L	H	L	L	C1, B0, A0
L	H	L	H	C1, B0, A1
L	H	H	L	C1, B1, A0
L	H	H	H	C1, B1, A1
H	X	X	X	None

(1) X = Don't care

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The CDx4HCx405x line of multiplexers and demultiplexers can be used for a wide variety of applications.

### 9.2 Typical Application

One application of the CD74HC4051 device is use in conjunction with a microcontroller to poll a keypad. Figure 20 shows the basic schematic for such a polling system. The microcontroller uses the channel-select pins to cycle through the different channels while reading the input to see if a user is pressing any of the keys. This is a very robust setup that allows for simultaneous key presses with very little power consumption. It also uses very few pins on the microcontroller. The down side of polling is that the microcontroller must frequently scan the keys for a press.

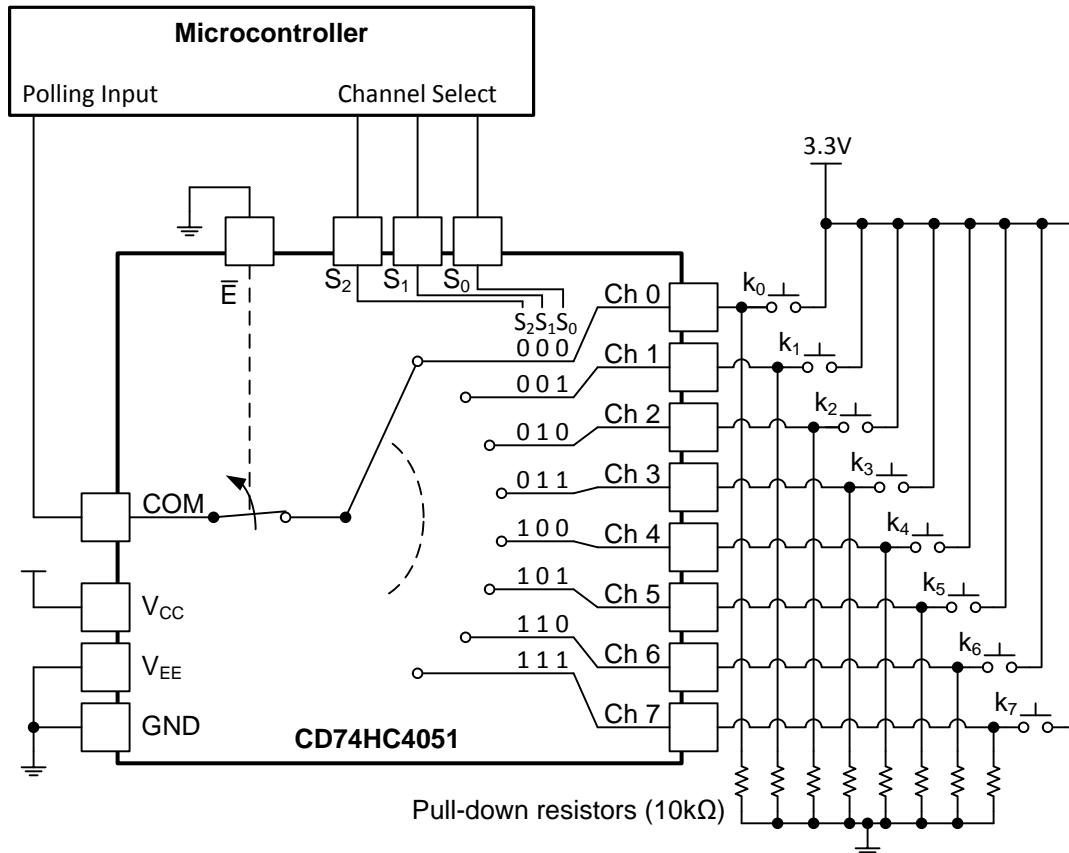


Figure 20. CD74HC4051 Being Used to Help Read Button Presses on a Keypad

#### 9.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

## Typical Application (continued)

See [Table 4](#) for the input loading details.

**Table 4. HCT Input Loading Table**

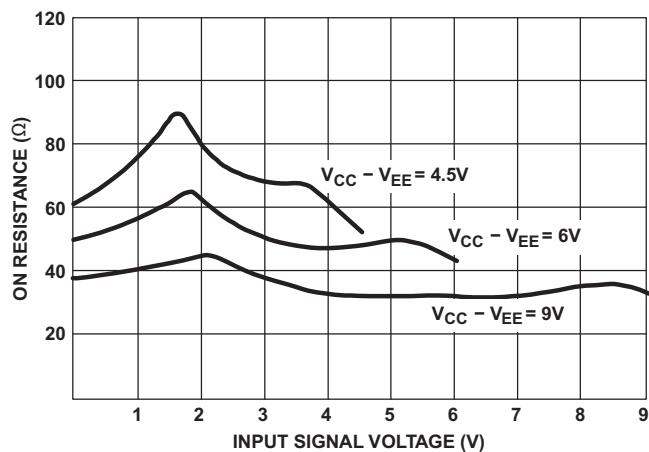
TYPE	INPUT	UNIT LOADS <sup>(1)</sup>
4051, 4053	All	0.5
4052	All	0.4

(1) Unit load is  $\Delta I_{CC}$  limit specified in [Specifications](#), for example, 360-mA MAX at 25°C.

### 9.2.2 Detailed Design Procedure

1. Recommended input conditions:
  - For switch time specifications, see propagation delay times in [Electrical Characteristics: HC Devices](#).
  - Inputs must not be pushed more than 0.5 V above  $V_{DD}$  or below  $V_{EE}$ .
  - For input voltage level specifications for control inputs, see  $V_{IH}$  and  $V_{IL}$  in [Electrical Characteristics: HC Devices](#).
2. Recommended output conditions:
  - Outputs must not be pulled above  $V_{DD}$  or below  $V_{EE}$ .
3. Input and output current consideration:
  - The CDx4HCx405x series of parts do not have internal current-drive circuitry, and thus cannot sink or source current. Any current will be passed through the device.

### 9.2.3 Application Curve



**Figure 21. Typical ON Resistance vs Input Signal Voltage**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Electrical Characteristics: HC Devices](#).

Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F bypass capacitor is recommended. If there are multiple pins labeled  $V_{CC}$ , then a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu$ F bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1- $\mu$ F and a 1- $\mu$ F capacitor are commonly used in parallel. For best results, the bypass capacitor or capacitors must be installed as close as possible to the power terminal.

## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they will have to turn corners. [Figure 22](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

### 11.2 Layout Example

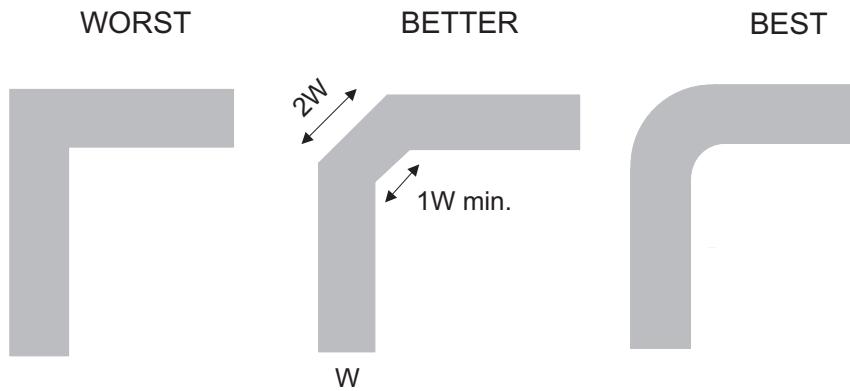


Figure 22. Trace Example

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

*Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54HC4051	<a href="#">Click here</a>				
CD74HC4051	<a href="#">Click here</a>				
CD54HCT4051	<a href="#">Click here</a>				
CD74HCT4051	<a href="#">Click here</a>				
CD54HC4052	<a href="#">Click here</a>				
CD74HC4052	<a href="#">Click here</a>				
CD54HCT4052	<a href="#">Click here</a>				
CD74HCT4052	<a href="#">Click here</a>				
CD54HC4053	<a href="#">Click here</a>				
CD74HC4053	<a href="#">Click here</a>				
CD54HCT4053	<a href="#">Click here</a>				
CD74HCT4053	<a href="#">Click here</a>				

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8775401EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8775401EA CD54HC4053F3A	<a href="#">Samples</a>
5962-8855601EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8855601EA CD54HC4052F3A	<a href="#">Samples</a>
5962-9065401MEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9065401ME A CD54HCT4051F3A	<a href="#">Samples</a>
CD54HC4051F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4051F	<a href="#">Samples</a>
CD54HC4051F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4051F3A	<a href="#">Samples</a>
CD54HC4052F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4052F	<a href="#">Samples</a>
CD54HC4052F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8855601EA CD54HC4052F3A	<a href="#">Samples</a>
CD54HC4053F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4053F	<a href="#">Samples</a>
CD54HC4053F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8775401EA CD54HC4053F3A	<a href="#">Samples</a>
CD54HCT4051F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9065401ME A CD54HCT4051F3A	<a href="#">Samples</a>
CD74HC4051E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4051E	<a href="#">Samples</a>
CD74HC4051EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4051E	<a href="#">Samples</a>
CD74HC4051M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	<a href="#">Samples</a>
CD74HC4051M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	HC4051M	<a href="#">Samples</a>
CD74HC4051M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	<a href="#">Samples</a>
CD74HC4051M96G3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	HC4051M	<a href="#">Samples</a>
CD74HC4051M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4051ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	<a href="#">Samples</a>
CD74HC4051MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	<a href="#">Samples</a>
CD74HC4051MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	<a href="#">Samples</a>
CD74HC4051NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	<a href="#">Samples</a>
CD74HC4051NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	<a href="#">Samples</a>
CD74HC4051PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	HJ4051	<a href="#">Samples</a>
CD74HC4051PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4051	<a href="#">Samples</a>
CD74HC4051PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4051	<a href="#">Samples</a>
CD74HC4051PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4051	<a href="#">Samples</a>
CD74HC4052E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4052E	<a href="#">Samples</a>
CD74HC4052EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4052E	<a href="#">Samples</a>
CD74HC4052M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	<a href="#">Samples</a>
CD74HC4052M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	HC4052M	<a href="#">Samples</a>
CD74HC4052M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	<a href="#">Samples</a>
CD74HC4052M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	<a href="#">Samples</a>
CD74HC4052ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	<a href="#">Samples</a>
CD74HC4052MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	<a href="#">Samples</a>
CD74HC4052MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4052MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4052NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4052NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4052PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4052PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4052PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	HJ4052	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4052PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4052PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4052PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4053E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4053E	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4053EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4053E	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4053M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4053M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	HC4053M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4053M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4053M96G3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	HC4053M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4053M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4053ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC4053MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4053MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	<a href="#">Samples</a>
CD74HC4053NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	<a href="#">Samples</a>
CD74HC4053PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053	<a href="#">Samples</a>
CD74HC4053PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053	<a href="#">Samples</a>
CD74HC4053PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	HJ4053	<a href="#">Samples</a>
CD74HC4053PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053	<a href="#">Samples</a>
CD74HC4053PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053	<a href="#">Samples</a>
CD74HCT4051E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4051E	<a href="#">Samples</a>
CD74HCT4051M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	<a href="#">Samples</a>
CD74HCT4051M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	<a href="#">Samples</a>
CD74HCT4051M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	<a href="#">Samples</a>
CD74HCT4051M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	<a href="#">Samples</a>
CD74HCT4051ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	<a href="#">Samples</a>
CD74HCT4051MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	<a href="#">Samples</a>
CD74HCT4051MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	<a href="#">Samples</a>
CD74HCT4051MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	<a href="#">Samples</a>
CD74HCT4052E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4052E	<a href="#">Samples</a>
CD74HCT4052EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4052E	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT4052M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	<a href="#">Samples</a>
CD74HCT4052M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	<a href="#">Samples</a>
CD74HCT4052M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	<a href="#">Samples</a>
CD74HCT4052ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	<a href="#">Samples</a>
CD74HCT4052MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	<a href="#">Samples</a>
CD74HCT4052MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	<a href="#">Samples</a>
CD74HCT4053E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4053E	<a href="#">Samples</a>
CD74HCT4053EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4053E	<a href="#">Samples</a>
CD74HCT4053M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	<a href="#">Samples</a>
CD74HCT4053M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	<a href="#">Samples</a>
CD74HCT4053M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	<a href="#">Samples</a>
CD74HCT4053M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	<a href="#">Samples</a>
CD74HCT4053ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	<a href="#">Samples</a>
CD74HCT4053MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	<a href="#">Samples</a>
CD74HCT4053MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	<a href="#">Samples</a>
CD74HCT4053PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 125	HK4053	<a href="#">Samples</a>
CD74HCT4053PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK4053	<a href="#">Samples</a>
CD74HCT4053PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK4053	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT4053PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK4053	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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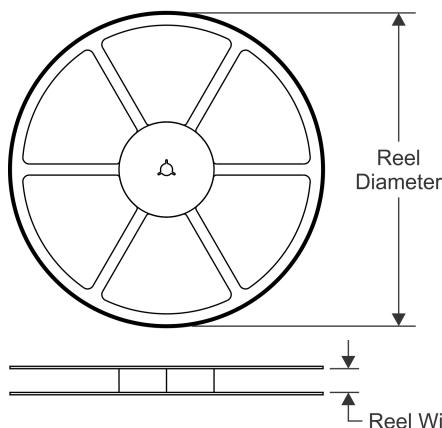
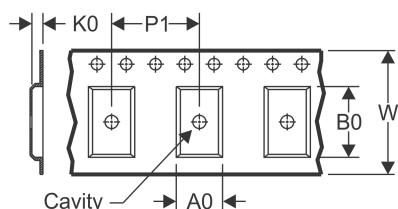
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC4051, CD54HC4052, CD54HC4053, CD54HCT4051, CD74HC4051, CD74HC4052, CD74HC4053, CD74HCT4051 :**

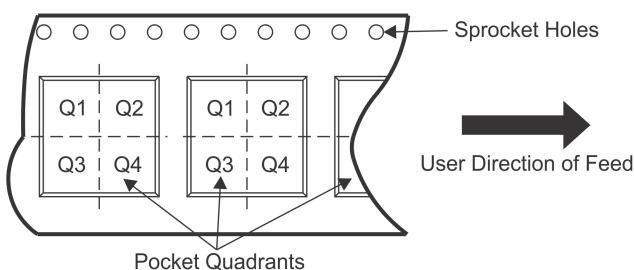
- Catalog: [CD74HC4051](#), [CD74HC4052](#), [CD74HC4053](#), [CD74HCT4051](#)
- Automotive: [CD74HC4051-Q1](#), [CD74HCT4051-Q1](#), [CD74HC4051-Q1](#), [CD74HCT4051-Q1](#)
- Enhanced Product: [CD74HC4051-EP](#), [CD74HC4051-EP](#)
- Military: [CD54HC4051](#), [CD54HC4052](#), [CD54HC4053](#), [CD54HCT4051](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


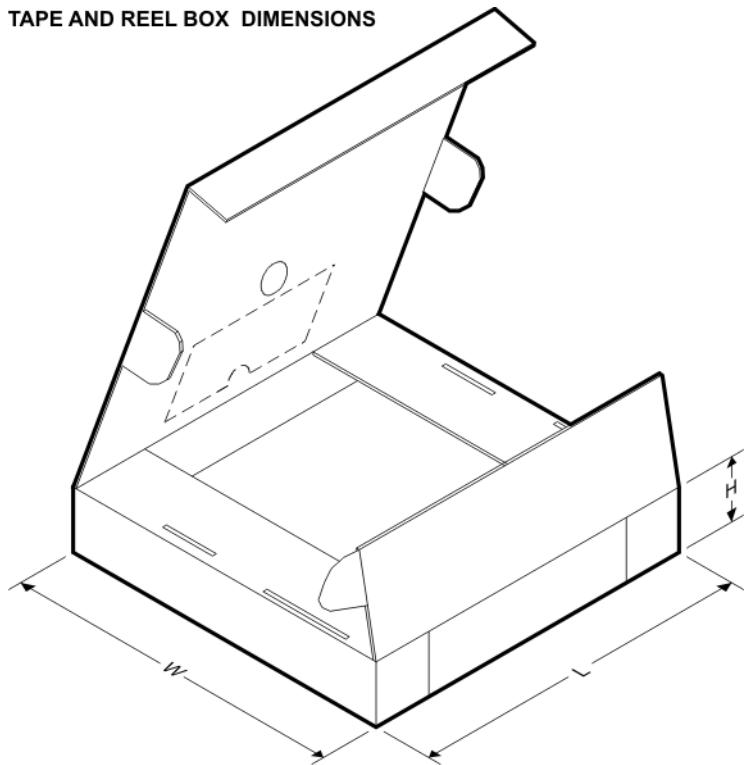
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4051M96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4051M96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4051M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4051PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4051PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052M96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4052M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4052NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC4052PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4053M96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4053M96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4053M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4053PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4053PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4051M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4052M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4053M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4053PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4053PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

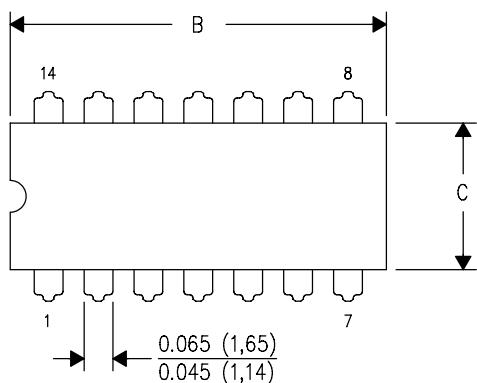
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4051M96	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4051M96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4051M96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4051PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4051PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HC4051PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4051PWT	TSSOP	PW	16	250	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4052M96	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4052M96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4052NSR	SO	NS	16	2000	367.0	367.0	38.0
CD74HC4052PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4052PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HC4052PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4052PWT	TSSOP	PW	16	250	367.0	367.0	35.0
CD74HC4053M96	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4053M96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4053M96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4053PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4053PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HC4053PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4053PWT	TSSOP	PW	16	250	367.0	367.0	35.0
CD74HCT4051M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT4052M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT4053M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT4053PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HCT4053PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HCT4053PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HCT4053PWT	TSSOP	PW	16	250	367.0	367.0	35.0

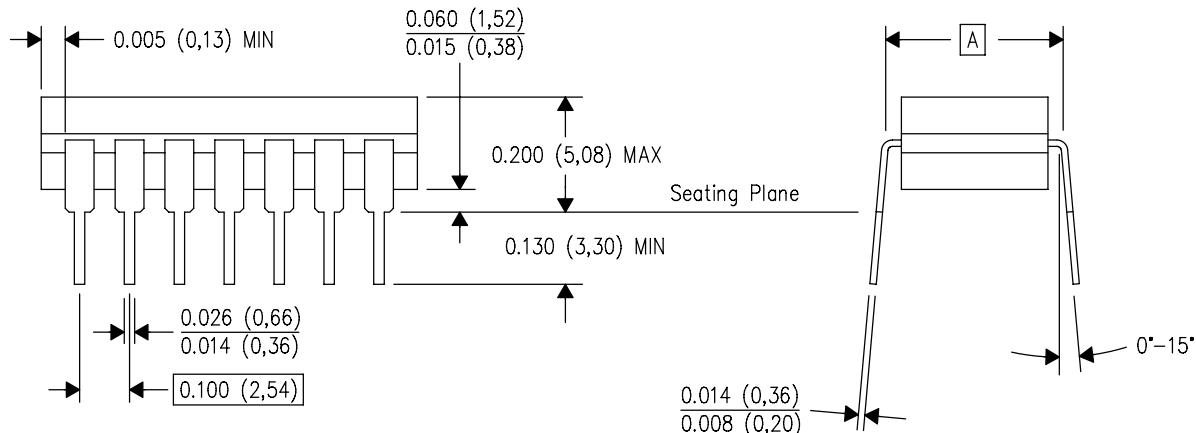
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



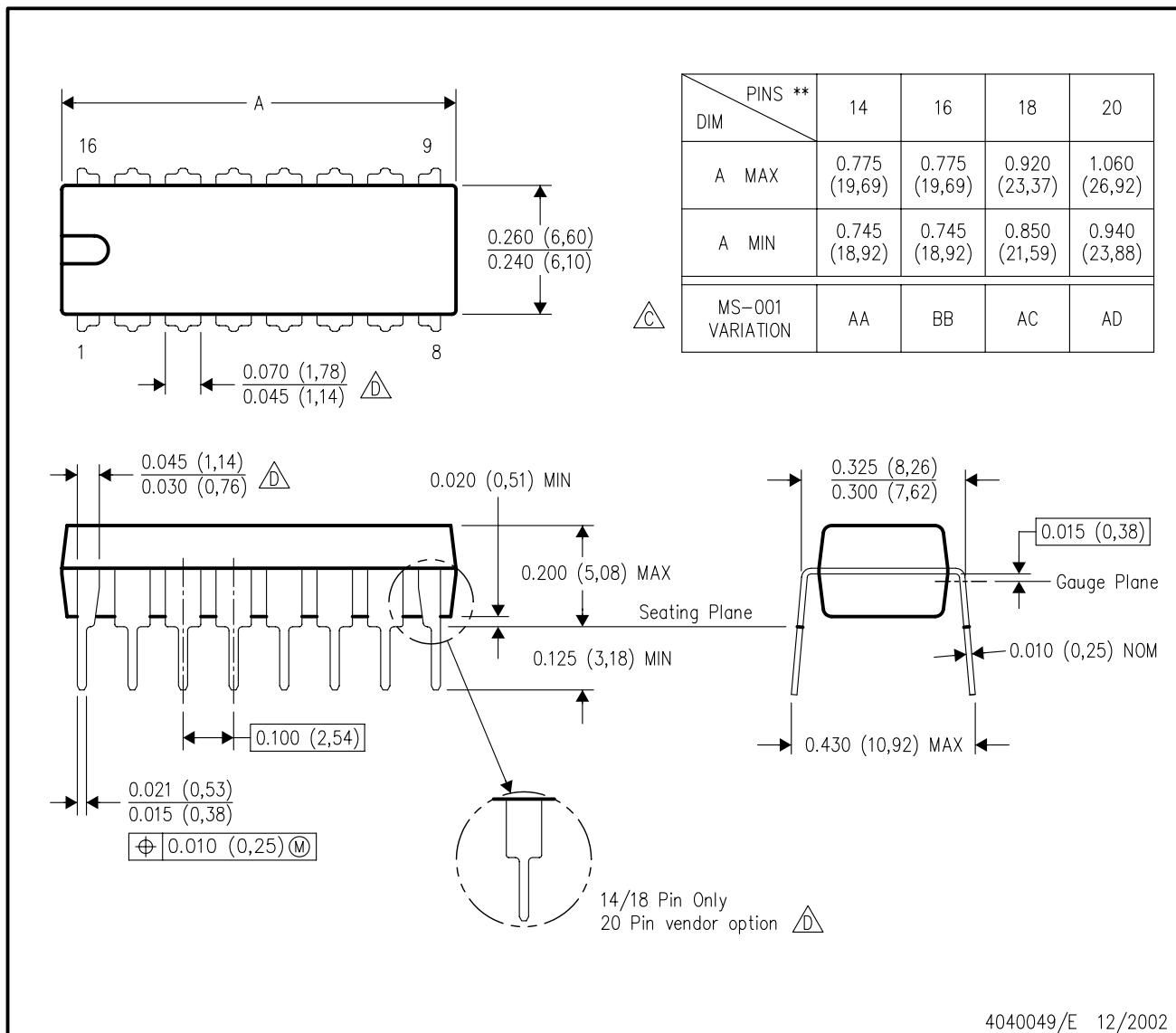
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

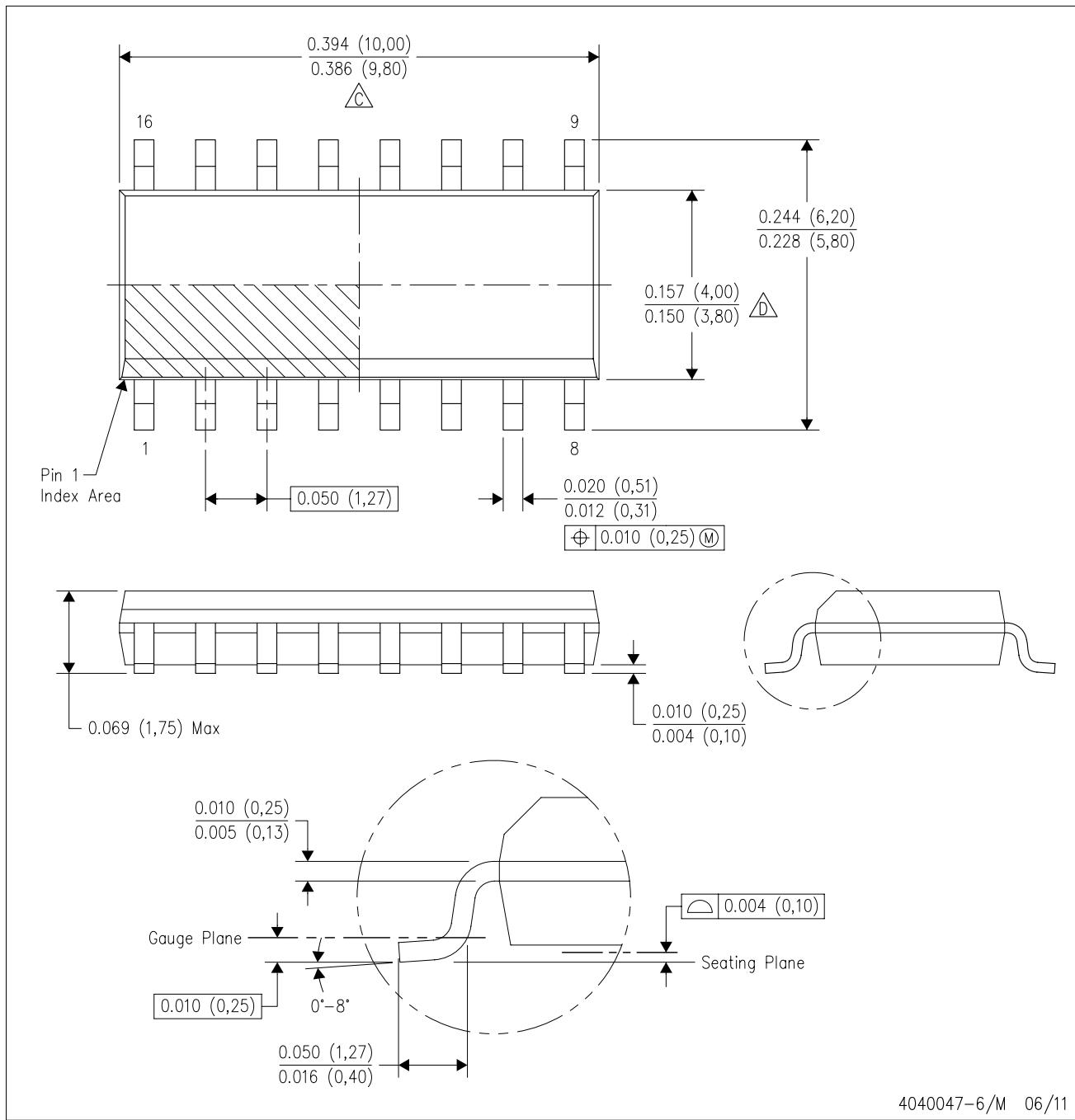
16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

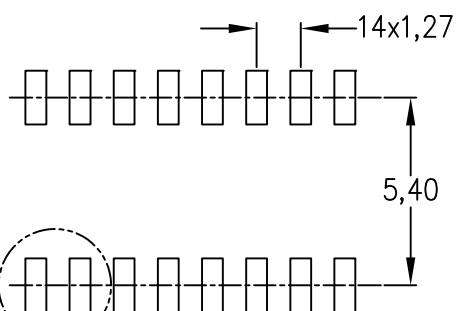
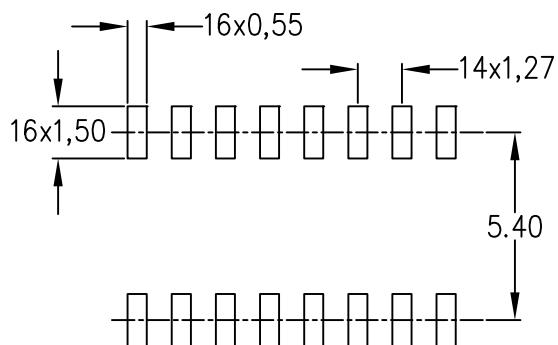
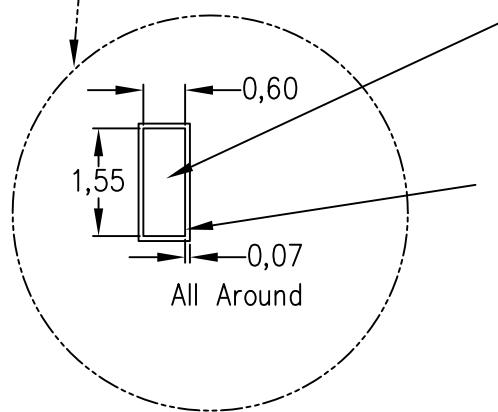
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

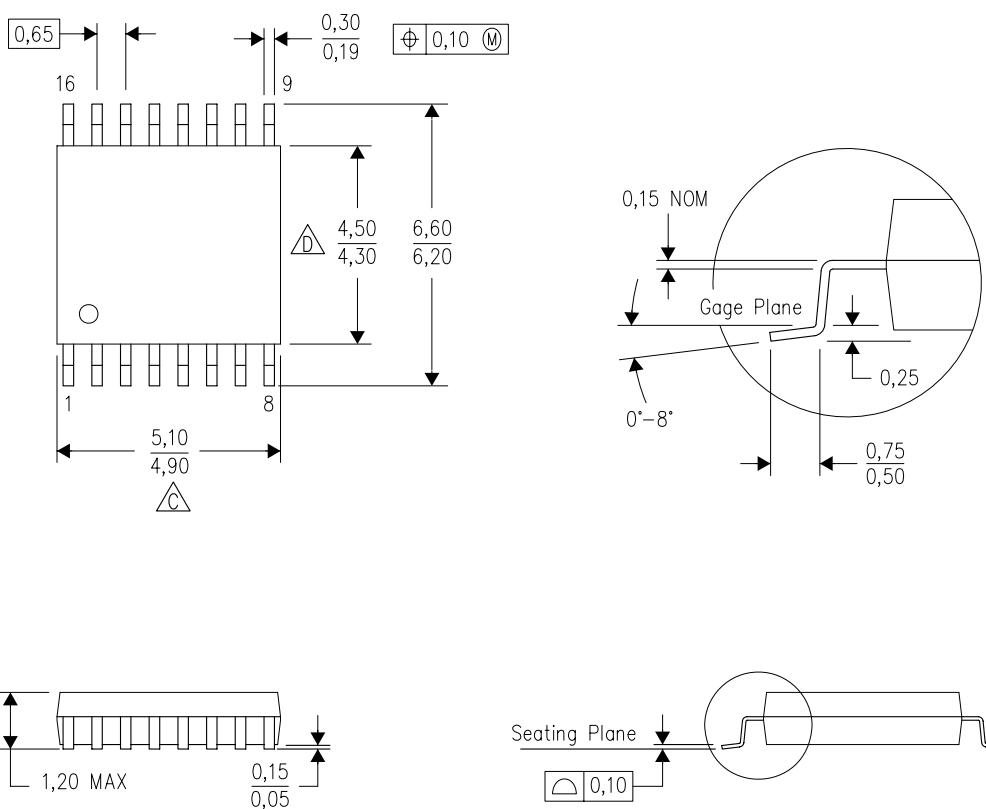
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

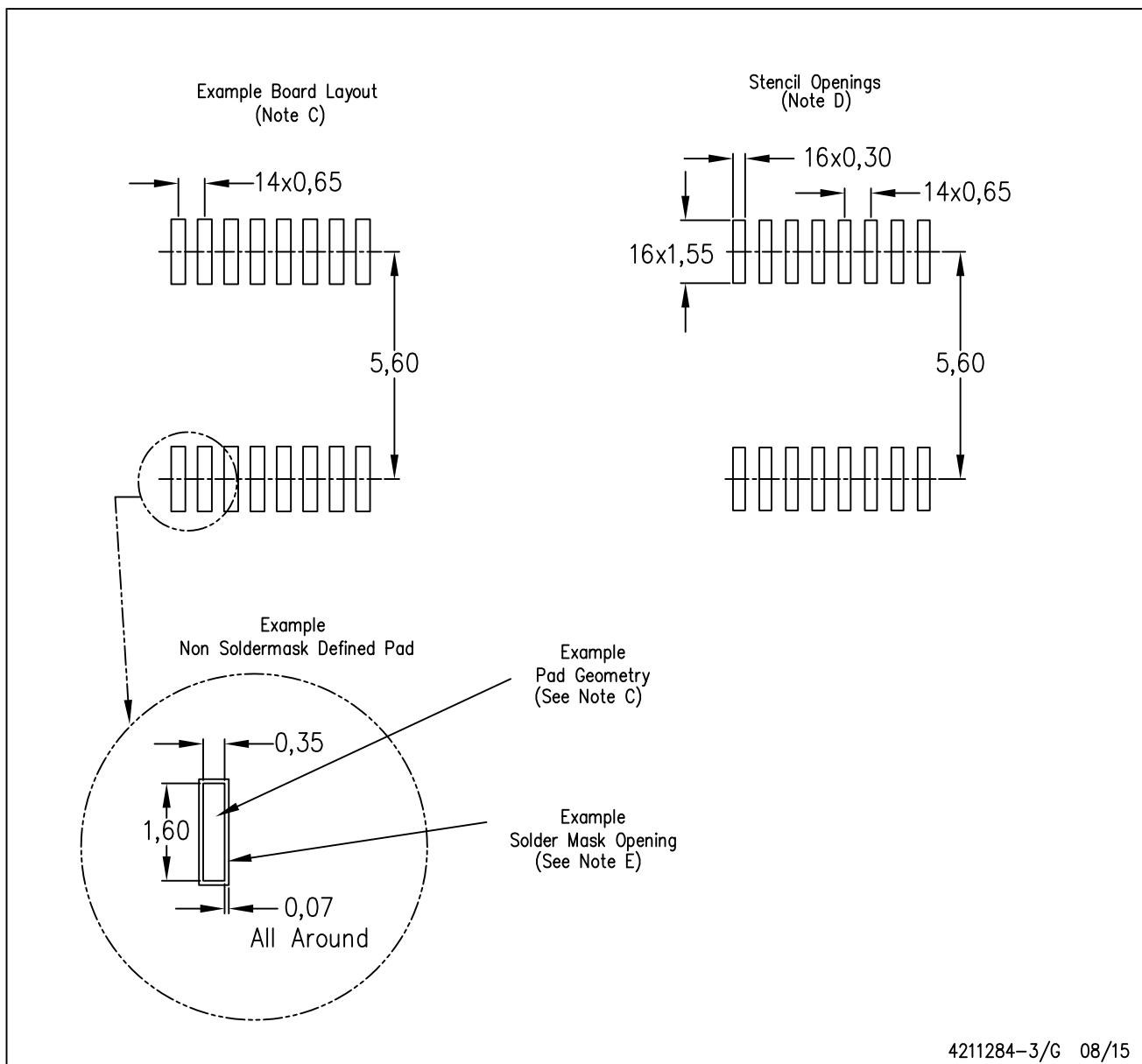
 C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

 D Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/G 08/15

NOTES:

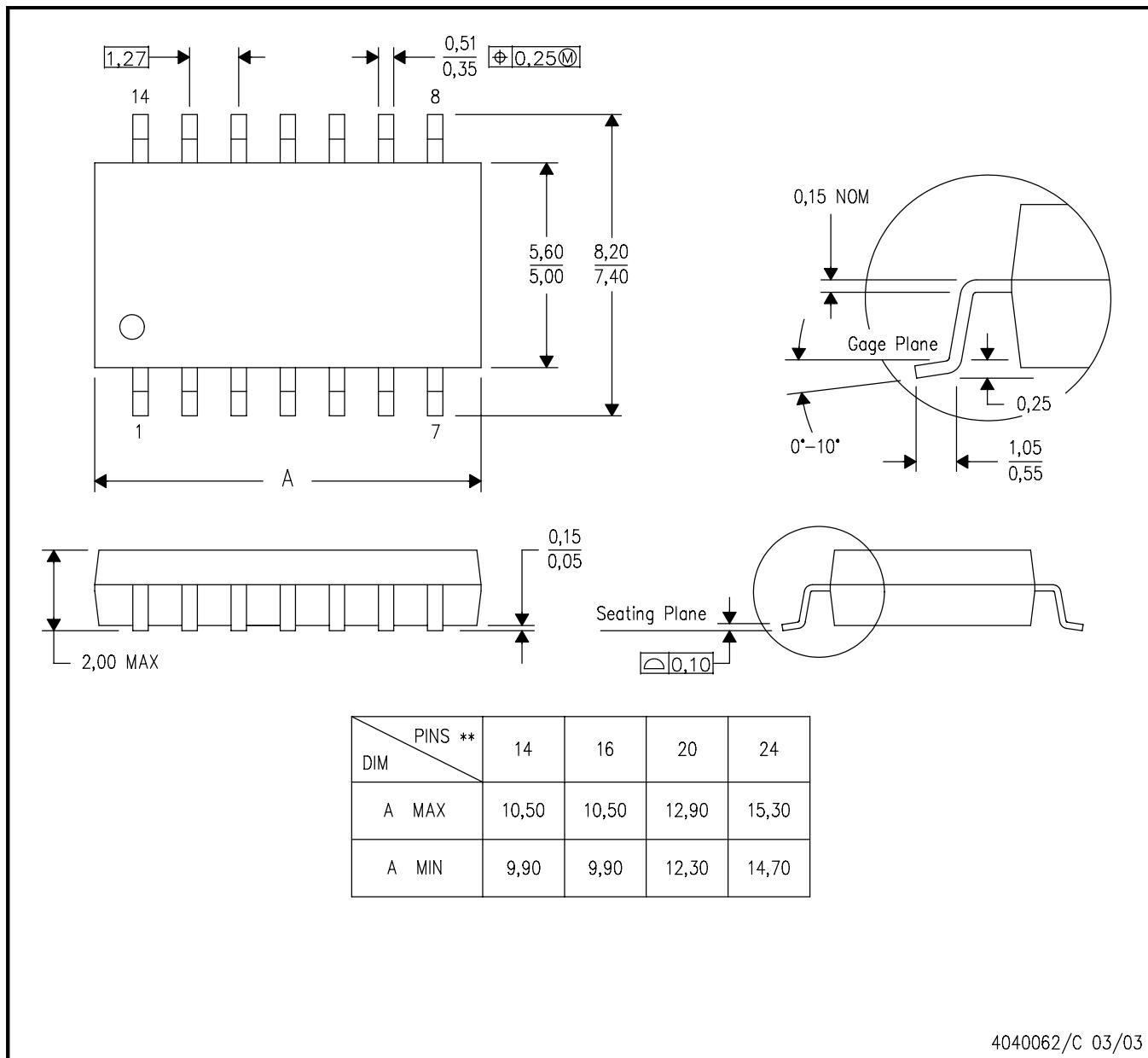
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

## NS (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>
	<b>TI E2E Community</b>
	<a href="http://e2e.ti.com">e2e.ti.com</a>