19-2129; Rev 1; 2/05

MAXIM

Low-Voltage, Dual DPDT/Quad SPDT Analog Switches in QFN

General Description

The MAX4699/MAX4701/MAX4702 are low-voltage, single-supply CMOS analog switches. The MAX4699/MAX4701 are dual double-pole/double-throw (DPDT) switches with two control inputs that control two single-pole/double-throw (SPDT) switches each. The MAX4702 is a quad SPDT switch with one control input and one low-voltage digital logic power supply.

These devices operate from a single +1.8V to +5.5V power supply. When powered from a +2.7V supply the MAX4699/MAX4701/MAX4702 offer a 75Ω on-resistance (R_{ON}), with 12Ω max R_{ON} flatness and 4Ω max matching between channels. Each switch has rail-to-rail signal handling, fast switching speeds of t_{ON} = 35ns, t_{OFF} = 20ns, and a maximum 1nA of leakage current.

The MAX4699/MAX4701 digital inputs are 1.8V-logic compatible when operated from a +3V supply. The MAX4702's digital inputs feature a 1.0V threshold when powered with a 1.5V logic supply.

The MAX4699 is available in a space-saving 16-lead 4mm x 4mm TQFN package. The MAX4701/MAX4702 are available in space-saving 16-lead 3mm x 3mm TQFN 16-pin TSSOP packages.

Applications

Audio and Video Signal Routing

Cellular Phones

Battery-Operated Equipment

Communications Circuits

Modems

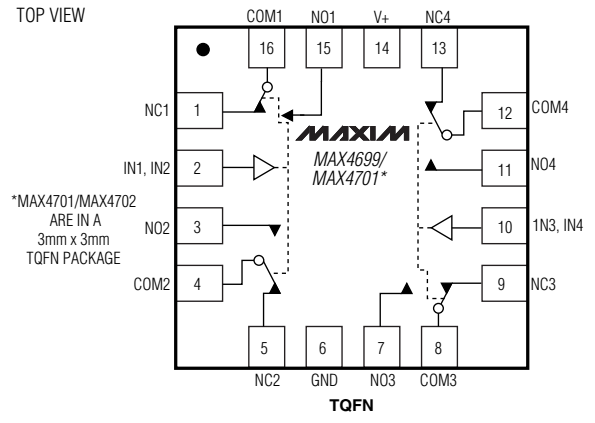
Features

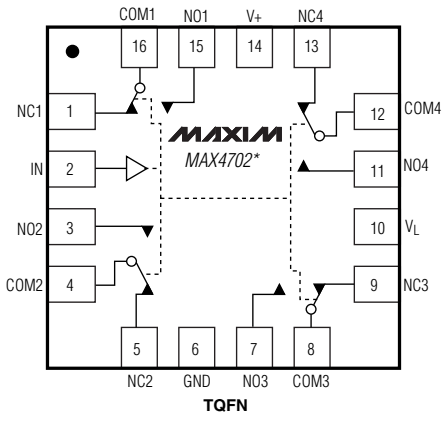
- **3mm x 3mm and 4mm x 4mm 16-Pin TQFN Packages**
- **Guaranteed On-Resistance:**
  75Ω (max) (+3V Supply)
  40Ω (max) (+5V Supply)
- **Guaranteed Match Between Channels:**
  4Ω max
- **Guaranteed Flatness Over Signal Range:**
  12Ω max
- **Low Leakage Currents Over Temperature:**
  1nA Max at +85°C
- **Fast Switching: t_{ON} = 35ns, t_{OFF} = 20ns**
- **Guaranteed Break-Before-Make**
- **Single-Supply Operation from +1.8V to +5.5V**
- **Rail-to-Rail Signal Handling**
- **-3dB Bandwidth: 250MHz**
- **Low Crosstalk: -79dB (1MHz)**
- **High Off-Isolation: -76dB (1MHz)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4699ETE	-40°C to +85°C	16 TQFN (4mm x 4mm)
MAX4701EUE	-40°C to +85°C	16 TSSOP
MAX4701ETE	-40°C to +85°C	16 TQFN (3mm x 3mm)
MAX4702EUE	-40°C to +85°C	16 TSSOP
MAX4702ETE	-40°C to +85°C	16 TQFN (3mm x 3mm)

Pin Configurations





Pin Configurations continued at end of data sheet.

Low-Voltage, Dual DPDT/Quad SPDT Analog Switches in QFN

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V+ .....-0.3V to +6V
V_L, IN_, COM_, NO_, NC_ (Note1)..... -0.3V to (V+ + 0.3V)
Continuous Current COM_, NO_, NC_ ..... ±20mA
Peak Current COM_, NO_, NC_ (pulsed at 1ms, 10% duty cycle).....±40mA
ESD per Method 3015.7.....>2.5kV

Continuous Power Dissipation (T_A = +70°C)
TSSOP (derate 5.6mW/°C above +70°C) 444mW
16-Pin Thin QFN (derate 20.8mW/°C above +70°C).....1666.7mW
16-Pin Thin QFN (derate 25mW/°C above +70°C).....2000mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: Signals on IN_, COM_, NO_, and NC_ exceeding 0 or V+ are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.3V, GND = 0, V_{IH} = +1.4V, V_{IL} = +0.5V, (V_L = +1.5V, V_{IH} = +1.0V, V_{IL} = +0.4V for MAX4702 only), T_A = -40°C to +85°C. Typical values are at V+ = +3V and T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = +2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = +1.5V	+25°C		60	75	Ω
			T_{MIN} to T_{MAX}			85	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = +2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = +1.5V	+25°C		2	4	Ω
			T_{MIN} to T_{MAX}			5	
On-Resistance Flatness (Note 5)	$R_{FLAT (ON)}$	V+ = +2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = +1V, +1.5V, +2V	+25°C		8	12	Ω
			T_{MIN} to T_{MAX}			14	
NO_, NC_ Off-Leakage Current (Note 6)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = +3.3V, $V_{COM\_}$ = +1V, +3V; $V_{NO\_}$ or $V_{NC\_}$ = +3V, +1V	+25°C	-0.5		+0.5	nA
			T_{MIN} to T_{MAX}	-1		1	
COM_ On-Leakage Current (Note 6)	$I_{COM\_ (ON)}$	V+ = +3.3V, $V_{COM\_}$ = +1V, +3V; $V_{NO\_}$ or $V_{NC\_}$ = +1V, +3V, or floating	+25°C	-0.5		+0.5	nA
			T_{MIN} to T_{MAX}	-1		1	
DYNAMIC							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = +2V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		27	35	ns
			T_{MIN} to T_{MAX}			45	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = +2V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		15	20	ns
			T_{MIN} to T_{MAX}			25	
Break-Before-Make (Note 6)	t_{BBM}	$V_{NO\_}$ or $V_{NC\_}$ = +2V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		15		ns
			T_{MIN} to T_{MAX}	1			
On-Channel -3dB Bandwidth	BW	Signal = 0, 50Ω in and out, Figure 5			250		MHz
Off-Isolation (Note 7)	V_{ISO}	f = 1MHz, R_L = 50Ω, C_L = 5pF, Figure 5	+25°C		-76		dB

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.3V, GND = 0, V_{IH} = +1.4V, V_{IL} = +0.5V, (V_L = +1.5V, V_{IH} = +1.0V, V_{IL} = +0.4V for MAX4702 only), T_A = -40°C to +85°C. Typical values are at V+ = +3V and T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Crosstalk (Note 8)	V_{CT}	f = 1MHz, R_L = 50Ω, C_L = 5pF, Figure 5	+25°C		-79		dB
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0Ω, C_L = 1.0nF, Figure 4	+25°C		0.5		pC
NO_, NC_, Off-Capacitance	$C_{NO\_(OFF)}$, $C_{NC\_(OFF)}$	f = 1MHz, $V_{NO\_}$, $V_{NC\_}$ = GND, Figure 6	+25°C		8		pF
Switch On-Capacitance	$C_{(ON)}$	f = 1MHz, Figure 6	+25°C		20		pF
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, 2.5Vp-p, R_L = 600Ω	+25°C		0.02		%
DIGITAL I/O							
Input Logic High	V_{IH}	MAX4699/MAX4701		1.4			V
		MAX4702 (V_L = +1.5V)		1.0			
Input Logic Low	V_{IL}	MAX4699/MAX4701				0.8	V
		MAX4702 (V_L = +1.5V)				0.4	
Input Leakage Current	I_{IH}, I_{IL}	V_{IN} = 0 to V+		-1		1	µA
SUPPLY							
Power-Supply Range	V+			1.8		5.5	V
Logic Power-Supply Input	V_L			1.5		V+	V
Positive Supply Current	I+	V+ = +3.3V, V_{IN} = 0 or V+	T_{MIN} to T_{MAX}	-1		1	µA

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, GND = 0, V_{IH} = +2.4V, V_{IL} = +0.8V, (V_L = +1.5V, V_{IH} = +1.0V, V_{IL} = +0.4V for MAX4702 only), T_A = -40°C to +85°C. Typical values are at V+ = +5V and T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = +4.5V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = +3.5V	+25°C		30	40	Ω
			T_{MIN} to T_{MAX}			50	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = +4.5V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = +3.5V	+25°C		1	3	Ω
			T_{MIN} to T_{MAX}			5	
On-Resistance Flatness (Note 5)	$R_{FLAT (ON)}$	V+ = +4.5V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = +2.0V, +2.25V, +3.5V	+25°C		5	8	Ω
			T_{MIN} to T_{MAX}			10	
DYNAMIC							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = +3V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		15	18	ns
			T_{MIN} to T_{MAX}			20	

Low-Voltage, Dual DPDT/Quad SPDT Analog Switches in QFN

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, GND = 0, V_{IH} = +2.4V, V_{IL} = +0.8V, (V_L = +1.5V, V_{IH} = +1.0V, V_{IL} = +0.4V for MAX4702 only), T_A = -40°C to +85°C. Typical values are at V+ = +5V and T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

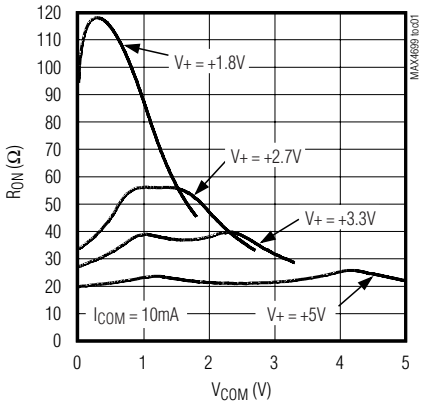
PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = +3V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		7	12	ns
			T_{MIN} to T_{MAX}			15	
Break-Before-Make (Note 6)	t_{BBM}	$V_{NO\_}$ or $V_{NC\_}$ = +3V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		10		ns
			T_{MIN} to T_{MAX}	2			
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1.0nF, Figure 4	+25°C		0.5		pC
DIGITAL I/O							
Input Logic High	V_{IH}	MAX4699/MAX4701		2.4			V
		MAX4702 (V_L = +1.5V)		1.0			
Input Logic Low	V_{IL}	MAX4699/MAX4701				0.8	V
		MAX4702 (V_L = +1.5V)				0.4	
Logic Input Current	I_{IH}, I_{IL}	V_{IN} = 0 to V+		-1		1	µA

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
Note 3: -40°C specifications are guaranteed by design.
Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
Note 6: Guaranteed by design.
Note 7: Off-Isolation = 20log10 ($V_{COM\_}$ / V_{NO}), V_{COM} = output, V_{NO} = input to off switch.
Note 8: Between any two switches.

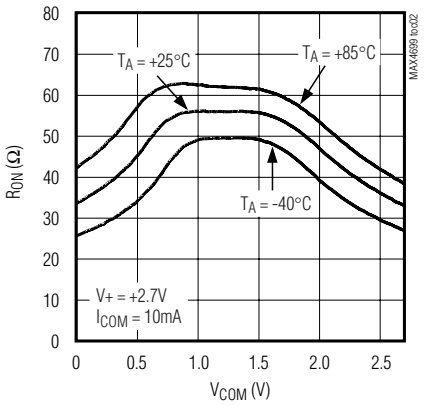
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted. V_L = +1.5V for MAX4702 only)

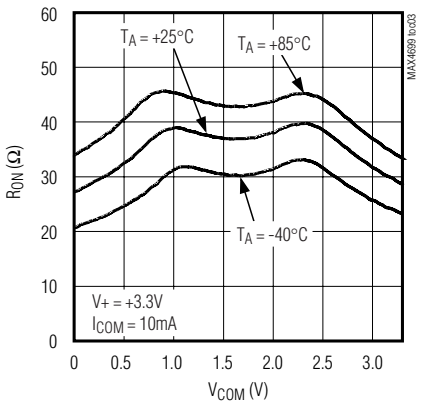
ON-RESISTANCE vs. COM VOLTAGE OVER SUPPLY VOLTAGE



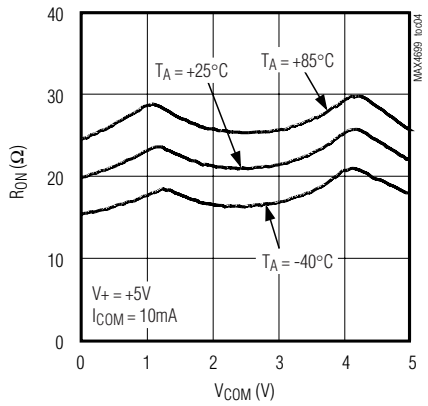
ON-RESISTANCE vs. COM VOLTAGE OVER TEMPERATURE (V+ = +2.7V)



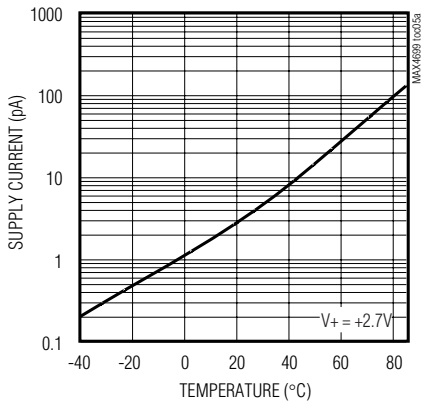
ON-RESISTANCE vs. COM VOLTAGE OVER TEMPERATURE (V+ = +3.3V)



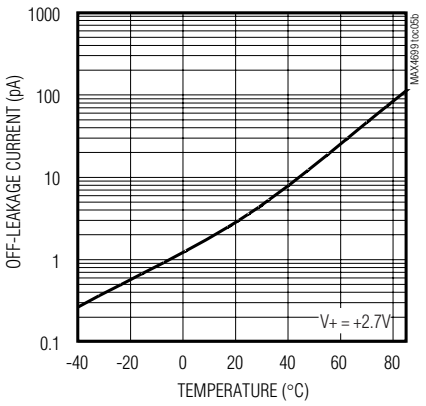
ON-RESISTANCE vs. COM VOLTAGE OVER TEMPERATURE (V+ = +5V)



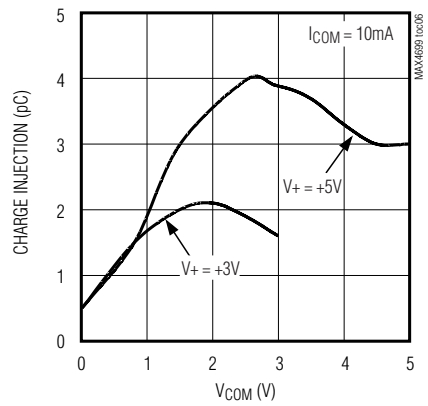
ON-LEAKAGE CURRENT vs. TEMPERATURE



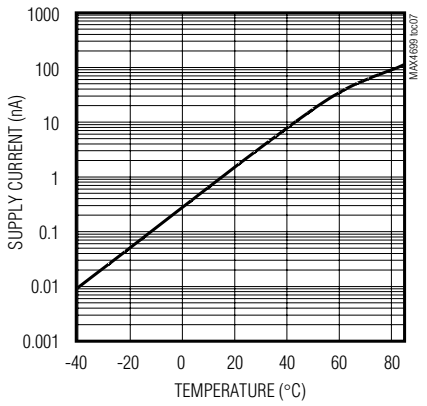
OFF-LEAKAGE CURRENT vs. TEMPERATURE



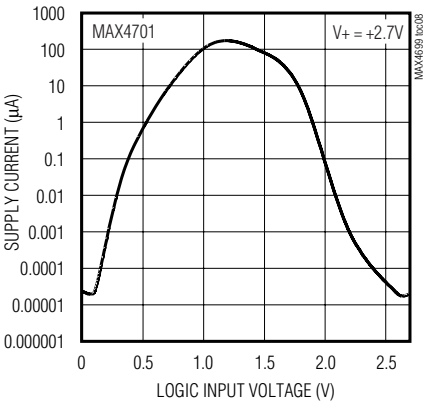
CHARGE INJECTION vs. COM VOLTAGE OVER SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE

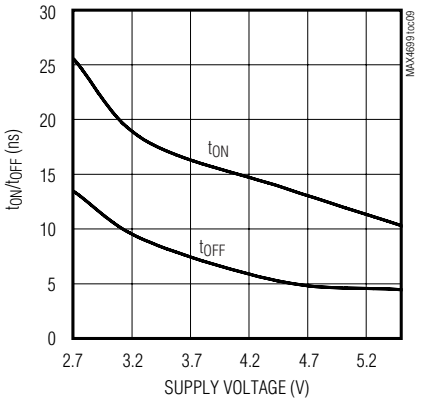


Low-Voltage, Dual DPDT/Quad SPDT Analog Switches in QFN

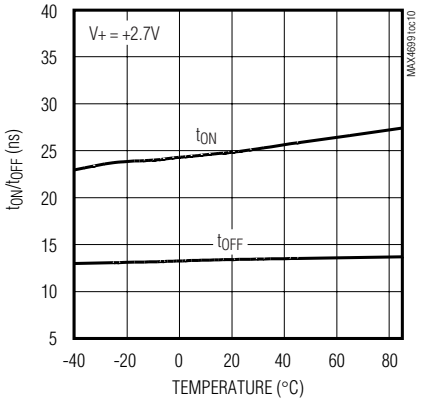
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted. V_L = +1.5V for MAX4702 only)

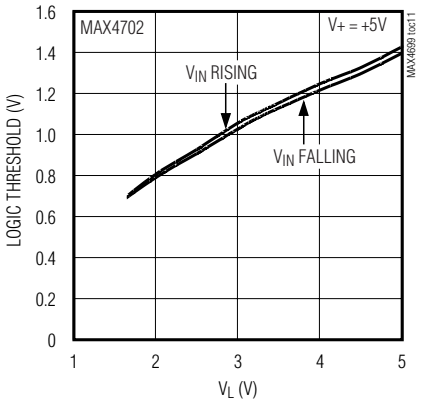
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



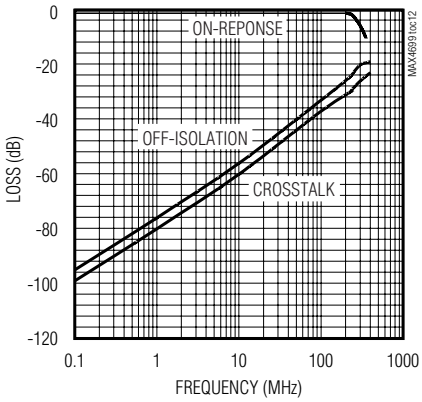
TURN-ON/OFF TIME vs. TEMPERATURE



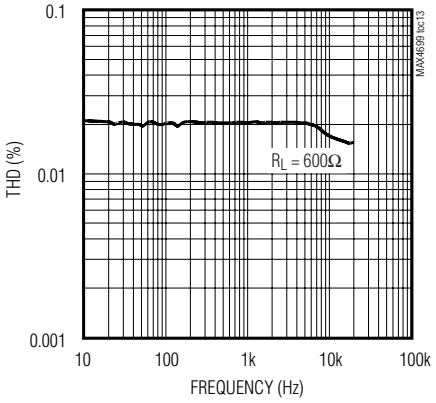
LOGIC THRESHOLD vs. V_L



FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Description

QFN PIN		TSSOP PIN		NAME	FUNCTION
MAX4699/ MAX4701	MAX4702	MAX4701	MAX4702		
1	1	3	3	NC1	Analog Switch 1—Normally Closed Terminal
—	2	—	4	IN	Digital Control Input Switch 1, 2, 3, and 4
2	—	4	—	IN1, IN2	Digital Control Input Switch 1 and 2
3	3	5	5	NO2	Analog Switch 2—Normally Open Terminal
4	4	6	6	COM2	Analog Switch 2—Common Terminal
5	5	7	7	NC2	Analog Switch 2—Normally Closed Terminal
6	6	8	8	GND	Ground
7	7	9	9	NO3	Analog Switch 3—Normally Open Terminal
8	8	10	10	COM3	Analog Switch 3—Common Terminal
9	9	11	11	NC3	Analog Switch 3—Normally Closed Terminal
—	10	—	12	V_L	Logic Power-Supply Input
10	—	12	—	IN3, IN4	Digital Control Input Switch 3 and 4
11	11	13	13	NO4	Analog Switch 4—Normally Open Terminal
12	12	14	14	COM4	Analog Switch 4—Common Terminal
13	13	15	15	NC4	Analog Switch 4—Normally Closed Terminal
14	14	16	16	V+	Positive Supply Voltage Input
15	15	1	1	NO1	Analog Switch 1—Normally Open Terminal
16	16	2	2	COM1	Analog Switch 1—Common Terminal

Detailed Description

The MAX4699/MAX4701 are low-voltage CMOS analog switches that operate from a single +1.8V to +5.5V power supply. The MAX4702 requires an additional logic supply that allows for setting lower logic thresholds. The MAX4699/MAX4701 are double-pole/double-throw (DPDT) devices. The MAX4702 is a quad single-pole/double-throw (SPDT) device. These devices feature a break-before-make switching, fast switching speeds (with V+ = 5V: t_{ON} = 18ns max, t_{OFF} = 9ns max and with V+ = 3V: t_{ON} = 35ns, t_{OFF} = 20) and rail-to-rail signal handling. A logic input on the MAX4702 allows for logic thresholds as low as 1.0V.

Applications Information

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) can be passed with very little change in on-resistance (see *Typical Operating Characteristics*). The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

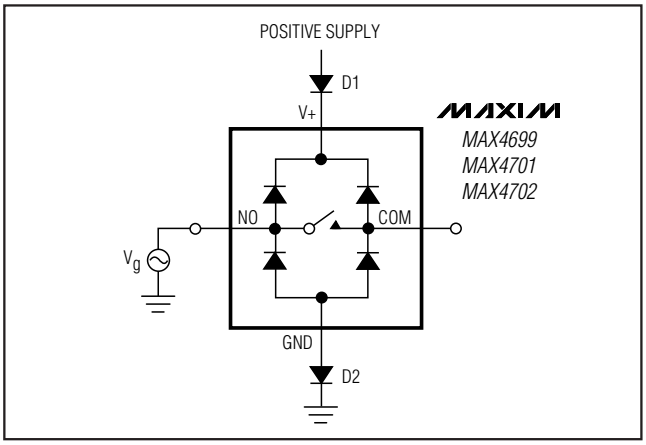


Figure 1. Overvoltage Protection Using Two External Blocking Diodes

Low-Voltage, Dual DPDT/Quad SPDT Analog Switches in QFN

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to <20mA, add a small-signal diode (D1) as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog range to a diode drop (about 0.7V) below V+ (for D1), and a diode drop above ground (for D2). On-resistance increases slightly at low supply voltages. Maximum supply voltage (V+) must not exceed +6V.

Adding protection diode D2 causes the logic threshold to be shifted relative to GND. TTL compatibility is not guaranteed when D2 is added.

Protection diodes D1 and D2 also protect against some overvoltage situations. With Figure 1's circuit, if the supply voltage is below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result.

V_L Logic Input (MAX4702)

The MAX4702 features a V_L logic input that allows for lower logic input thresholds down to 1.0V min for V_{IH} in the quad SPDT configuration. Power-up V_L after V+ has been powered with a minimum of 1.5V to ensure proper operation of the device.

Test Circuits/Timing Diagrams

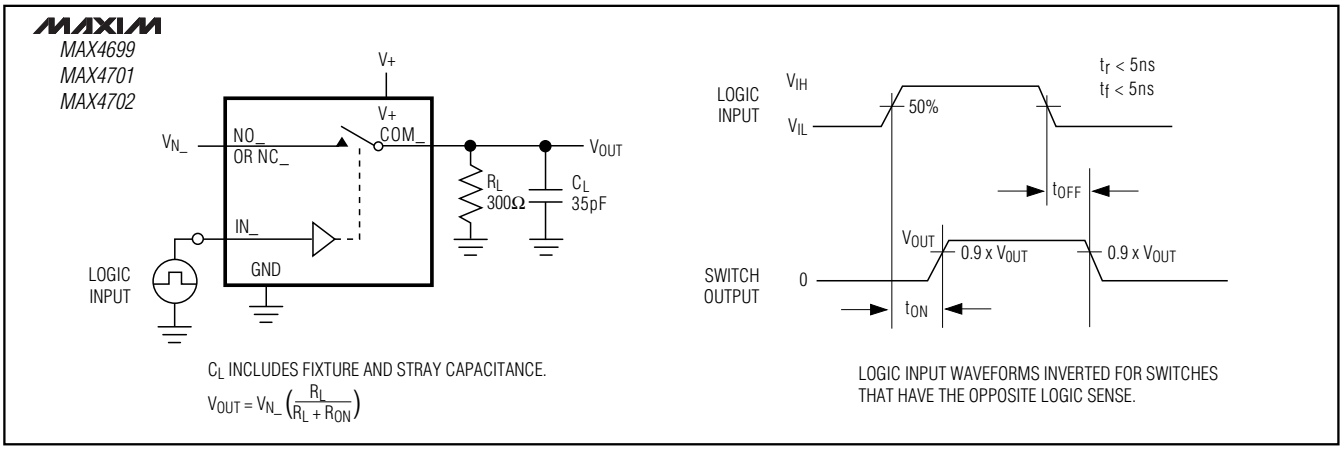


Figure 2. Switching Time

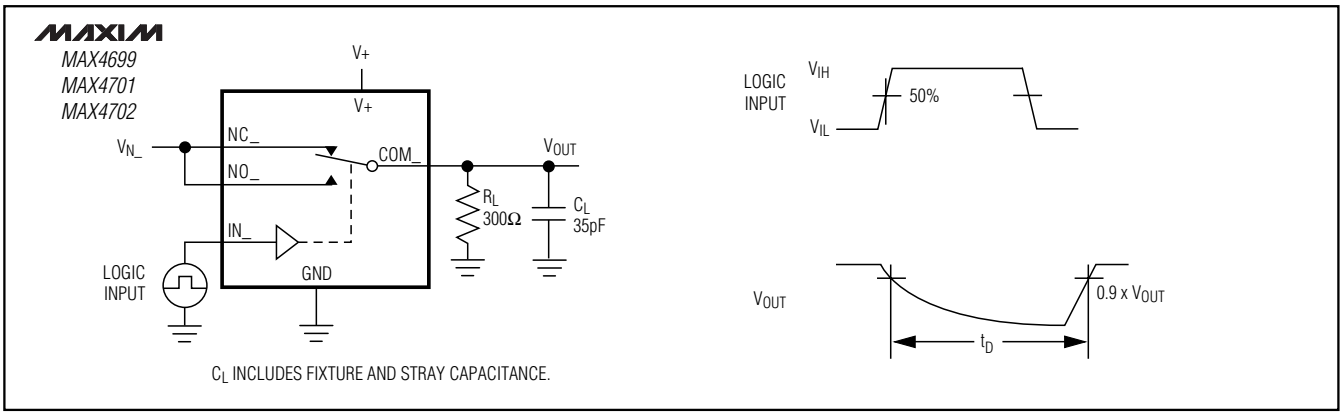


Figure 3. Break-Before-Make Interval

Test Circuits/Timing Diagrams (continued)

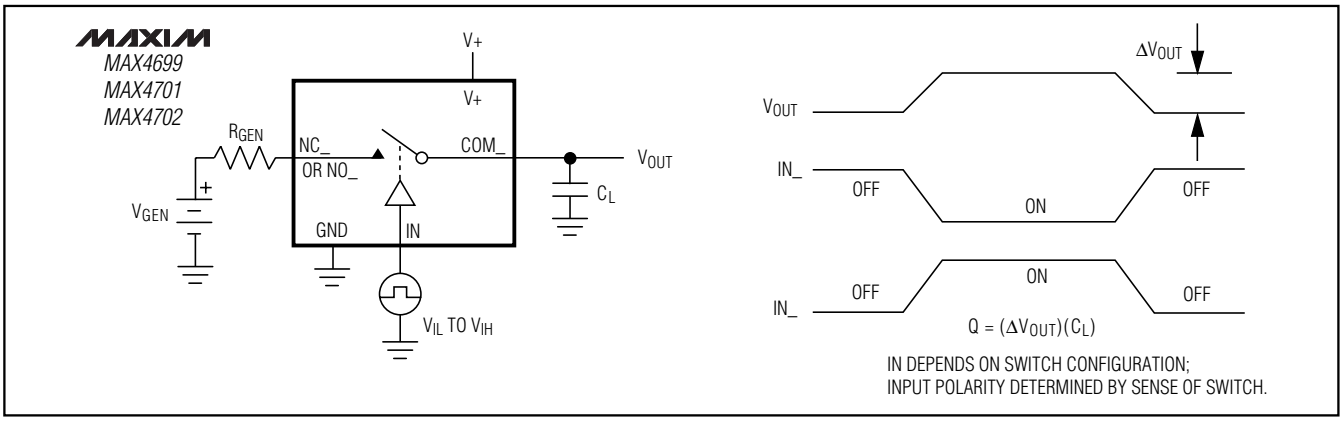


Figure 4. Charge Injection

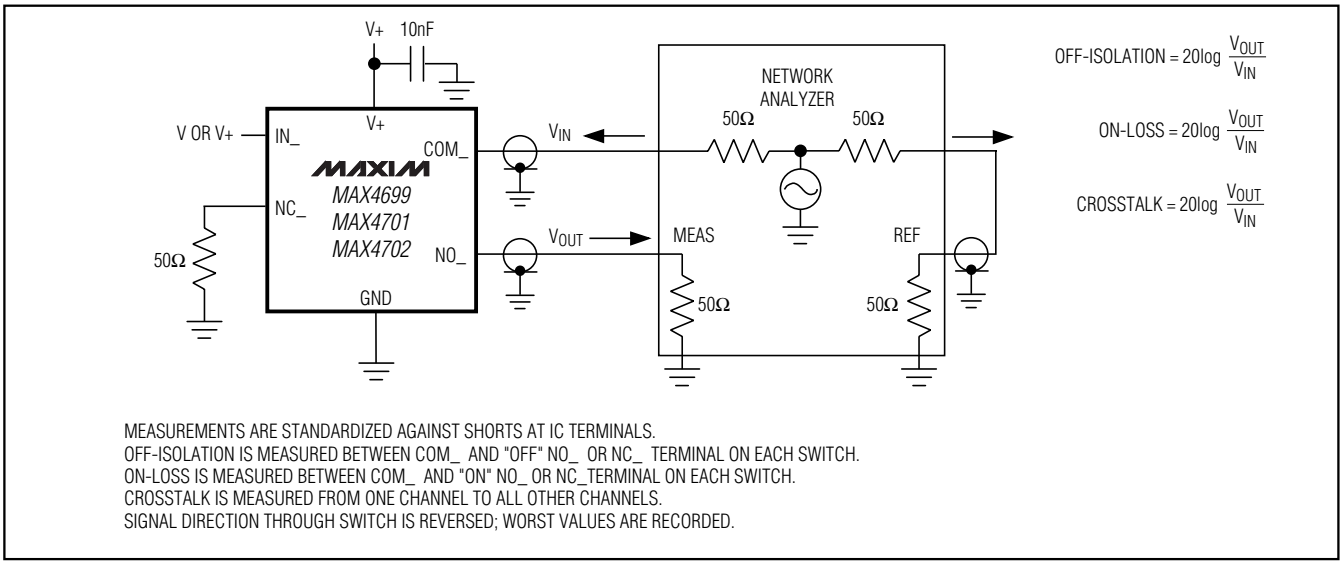


Figure 5. On-Loss, Off-Isolation, and Crosstalk

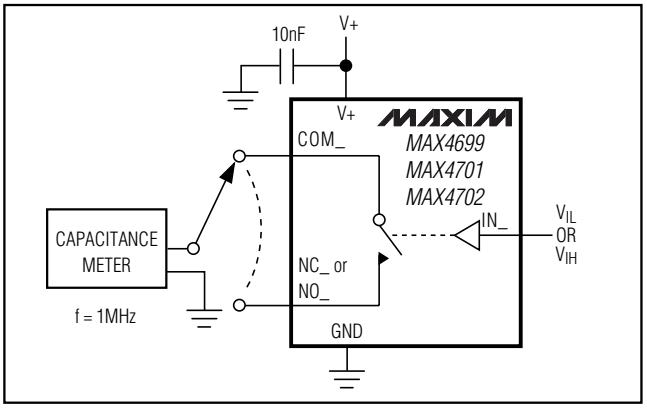


Figure 6. Channel Off/On-Capacitance

Chip Information

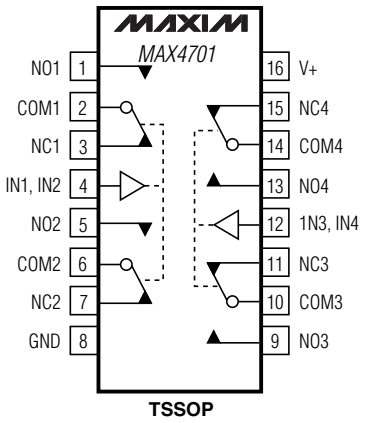
TRANSISTOR COUNT: 269

Substrate connected to GND

Low-Voltage, Dual DPDT/Quad SPDT Analog Switches in QFN

Pin Configurations (continued)

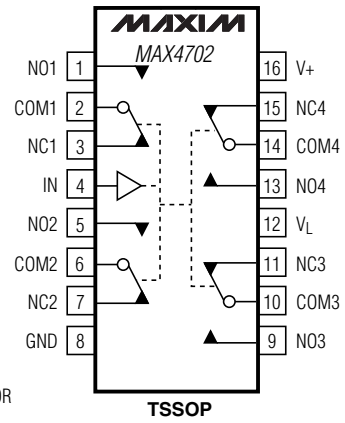
TOP VIEW



TSSOP

IN1, IN2	IN3, IN4	ON SWITCHES
L	—	NC1–COM1, NC2–COM2
H	—	NO1–COM1, NO2–COM2
—	L	NC3–COM3, NC4–COM4
—	H	NO3–COM3, NO4–COM4

SWITCHES SHOWN FOR LOGIC "0" INPUTS



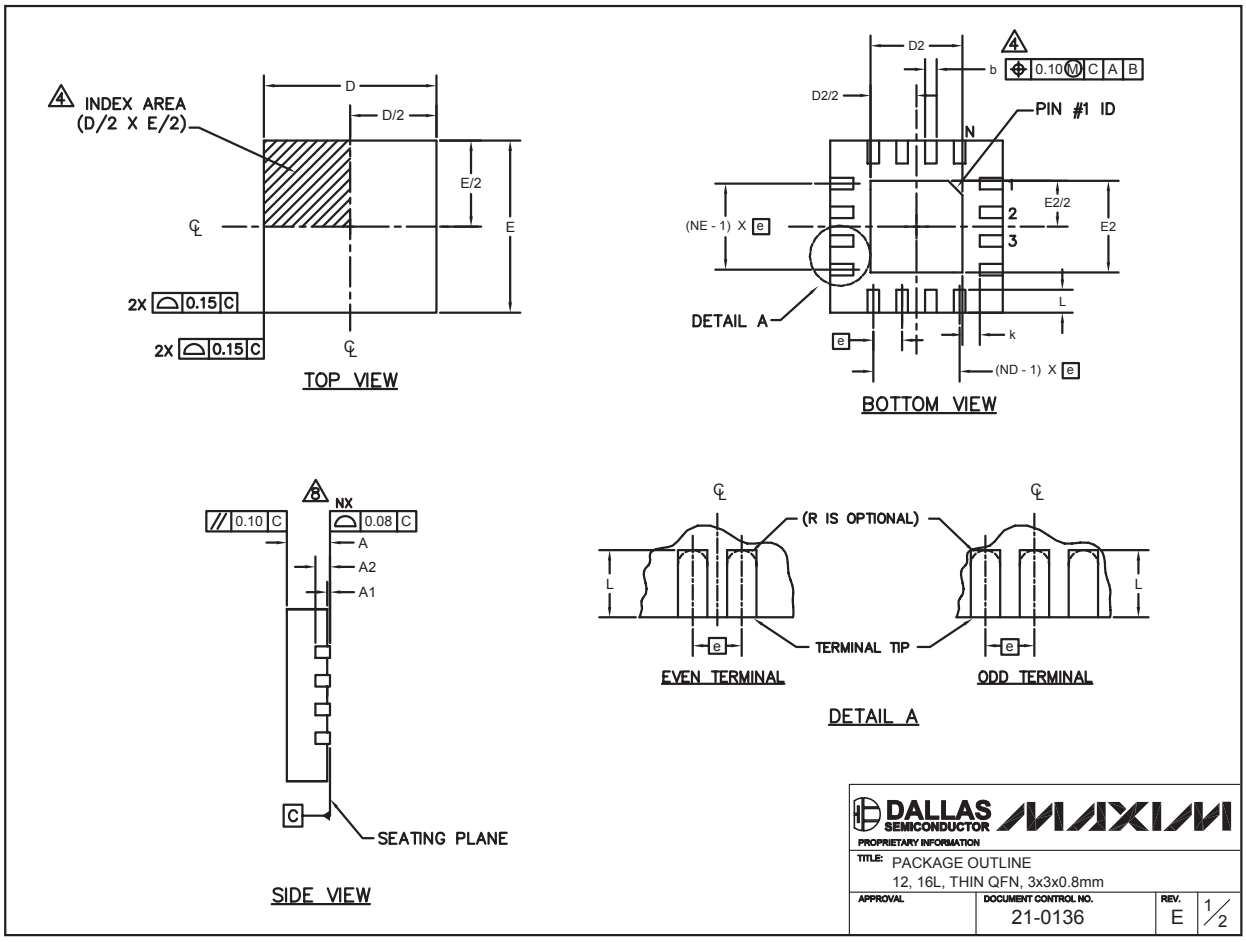
TSSOP

IN	ON SWITCHES
L	NC1–COM1, NC2–COM2 NC3–COM3, NC4–COM4
H	NO1–COM1, NO2–COM2 NO3–COM3, NO4–COM4

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



Low-Voltage, Dual DPDT/Quad SPDT Analog Switches in QFN

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45∞	WEED-1	NO
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45∞	WEED-1	YES
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45∞	WEED-2	NO
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45∞	WEED-2	YES
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45∞	WEED-2	N/A
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45∞	WEED-2	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

DALLAS SEMICONDUCTOR MAXIM

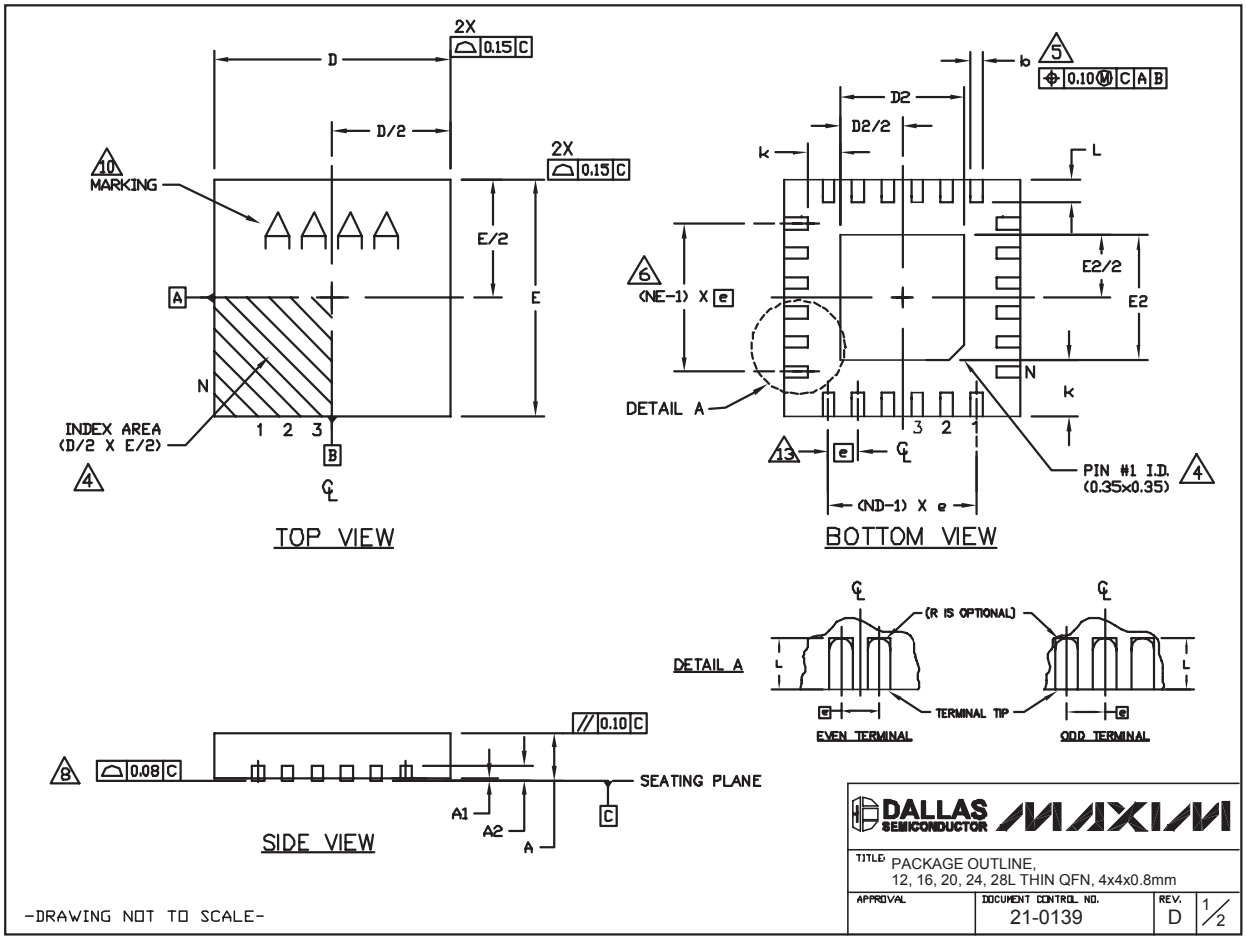
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
12, 16L, THIN QFN, 3x3x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	E	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Low-Voltage, Dual DPDT/Quad SPDT Analog Switches in QFN

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

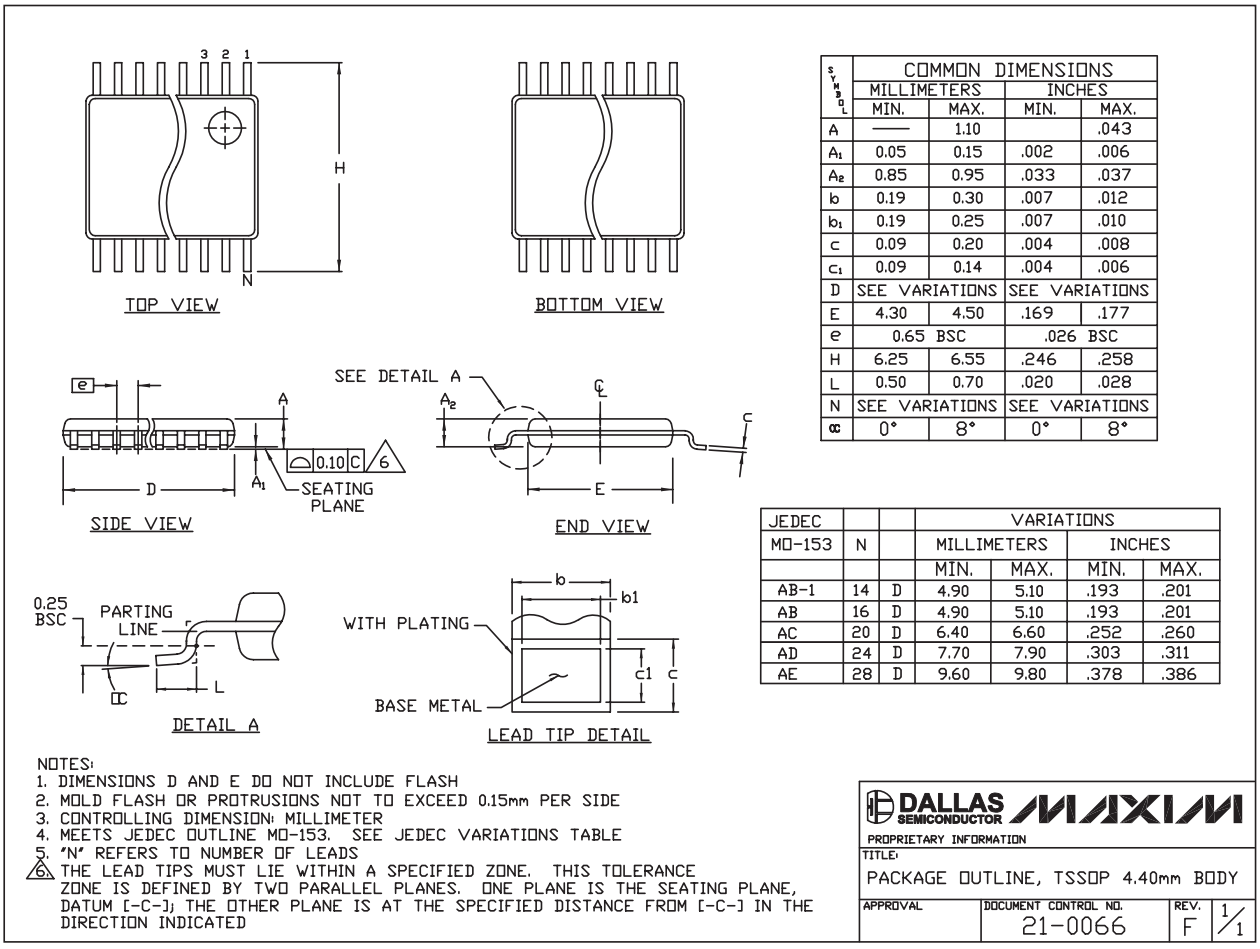
TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	D	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1