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74AHC244; 74AHCT244

Octal buffer/line driver; 3-state

Rev. 05 — 20 December 2007 Product data sheet

1. General description

The 74AHC244; 74AHCT244 is a high-speed Si-gate CMOS device.

The 74AHC244; 74AHCT244 has octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs (n$\overline{OE}$). A HIGH on n$\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

2. Features

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accepts voltages higher than V_{CC}
- For 74AHC244 only: operates with CMOS input levels
- For 74AHCT244 only: operates with TTL input levels
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC244D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHCT244D				
74AHC244PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74AHCT244PW				
74AHC244BQ	–40 °C to +125 °C	DHVQFN20	plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74AHCT244BQ				

founded by Philips

4. Functional diagram

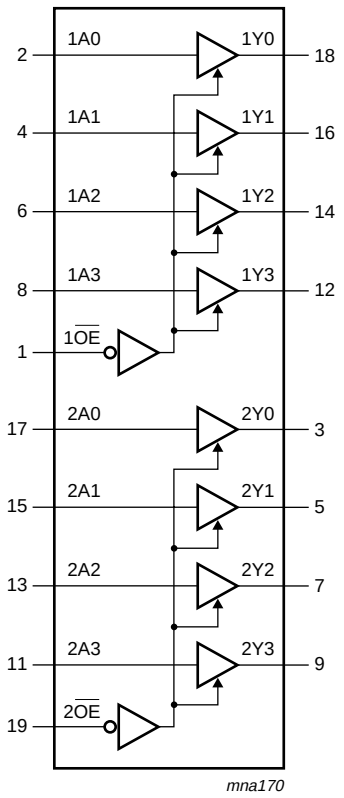

Fig 1. Functional diagram

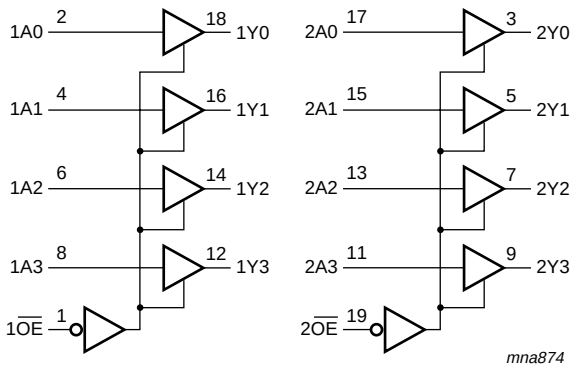

Fig 2. Logic symbol

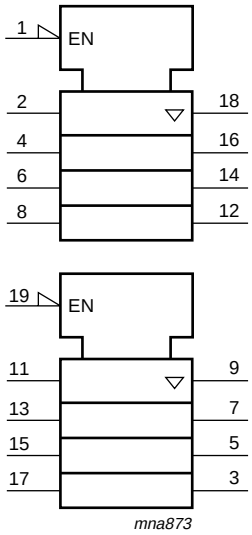

Fig 3. IEC logic symbol

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5. Pinning information

5.1 Pinning

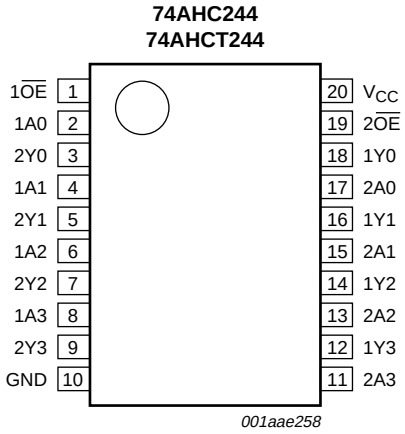
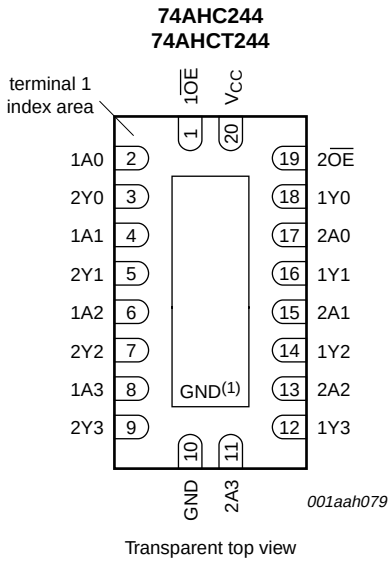


Fig 4. Pin configuration SO20, TSSOP20



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 5. Pin configuration DHVQFN20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	output enable input (active LOW)
1A[0:3]	2, 4, 6, 8	data input
2A[0:3]	17, 15, 13, 11	data input
1Y[0:3]	18, 16, 14, 12	data output
2Y[0:3]	3, 5, 7, 9	data output
GND	10	ground (0 V)
$2\overline{OE}$	19	output enable input (active LOW)
V_{CC}	20	supply voltage

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6. Functional description

Table 3. Function table[1]

Control	Input	Output
n$\overline{OE}$	**nAn**	**nYn**
L	L	L
	H	H
H	X	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage			–0.5	+7.0	V
I_{IK}	input clamping current	V_I < –0.5 V	[1]	–20	-	mA
I_{OK}	output clamping current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V	[1]	-	±20	mA
I_O	output current	V_O = –0.5 V to (V_{CC} + 0.5 V)		-	±25	mA
I_{CC}	supply current			-	75	mA
I_{GND}	ground current			–75	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
	SO20 package		[2]	-	500	mW
	TSSOP20 package		[3]	-	500	mW
	DHVQFN20 package		[4]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC244			74AHCT244			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V_{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
For type 74AHC244										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = –50 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –50 μA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I_O = –50 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 50 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 μA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	μA
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA

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Table 6. Static characteristics *...continued*

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	3.0	10	-	10	-	10	pF
C_O	output capacitance		-	4.0	-	-	-	-	-	pF
For type 74AHCT244										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = –50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I_{OZ}	OFF-state output current	per input pin; $V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V; I_O = 0 A $V_O = V_{CC}$ or GND; other pins at V_{CC} or GND	-	-	±0.25	-	±2.5	-	±10.0	μA
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; I_O = 0 A; other pins at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4.0	-	-	-	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. For test circuit see Figure 8.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
For type 74AHC244											
t_{pd}	propagation delay	nAn to nYn; see Figure 6	[2]								
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		-	5.0	8.4	1.0	10.0	1.0	10.5	ns
		C_L = 50 pF		-	7.0	11.9	1.0	13.5	1.0	15.0	ns
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	3.4	5.5	1.0	6.5	1.0	7.0	ns
		C_L = 50 pF			5.0	7.5	1.0	8.5	1.0	9.5	ns
t_{en}	enable time	$n\overline{OE}$ to nYn; see Figure 7	[2]								
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		-	6.5	10.6	1.0	12.5	1.0	13.5	ns
		C_L = 50 pF		-	7.5	14.1	1.0	16.0	1.0	18.0	ns
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	4.0	7.3	1.0	8.5	1.0	9.5	ns
		C_L = 50 pF		-	5.5	9.3	1.0	10.5	1.0	12.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nYn; see Figure 7	[2]								
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		-	5.5	9.7	1.0	11.0	1.0	12.5	ns
		C_L = 50 pF		-	10.0	14.0	1.0	16.0	1.0	17.5	ns
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	4.8	7.2	1.0	8.5	1.0	9.0	ns
		C_L = 50 pF		-	7.0	9.2	1.0	10.5	1.0	11.5	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[3]	-	10	-	-	-	-	-	pF

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Table 7. Dynamic characteristics *...continued*

GND = 0 V. For test circuit see Figure 8.

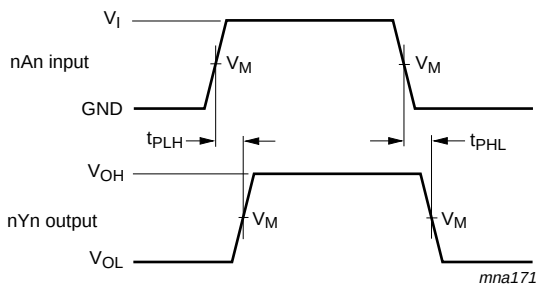
Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
For type 74AHCT244											
t_{pd}	propagation delay	nAn to nYn; see Figure 6	[2]								
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	3.5	7.4	1.0	8.5	1.0	9.5	ns
		C_L = 50 pF		-	5.0	8.4	1.0	9.5	1.0	10.5	ns
t_{en}	enable time	$n\overline{OE}$ to nYn; see Figure 7									
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	3.5	10.4	1.0	12.0	1.0	13.0	ns
		C_L = 50 pF		-	5.5	11.4	1.0	13.0	1.0	14.5	ns
t_{dis}	disable time	$n\overline{OE}$ to nYn; see Figure 7	[2]								
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	5.0	9.4	1.0	10.0	1.0	12.0	ns
		C_L = 50 pF		-	7.0	11.4	1.0	13.0	1.0	14.5	ns
C_{PD}	power dissipation capacitance	per buffer; C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC}	[3]	-	12	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts.

11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay input (nAn) to output (nYn)

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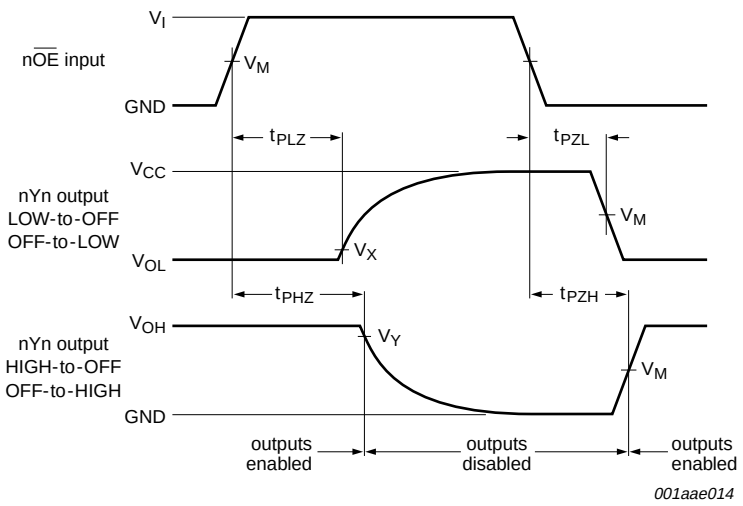

Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. enable and disable times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74AHC244	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} – 0.3 V
74AHCT244	1.5 V	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} – 0.3 V

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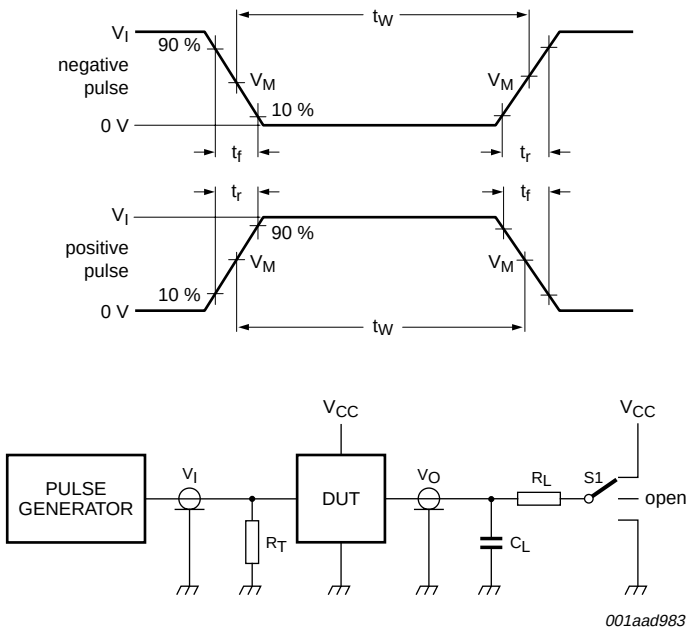

Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistor

S1 = Test selection switch

Fig 8. Load circuitry for switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC244	V_{CC}	3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74AHCT244	3.0 V	3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

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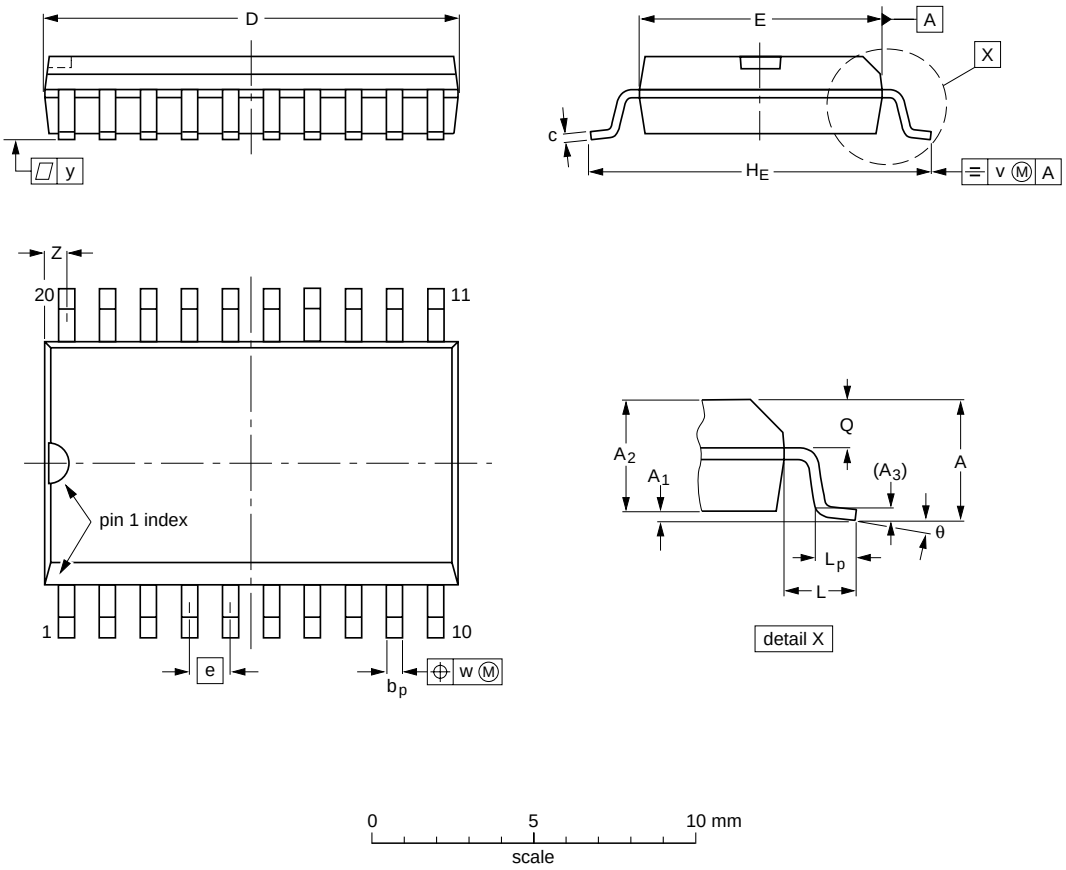
12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT163-1 (SO20)

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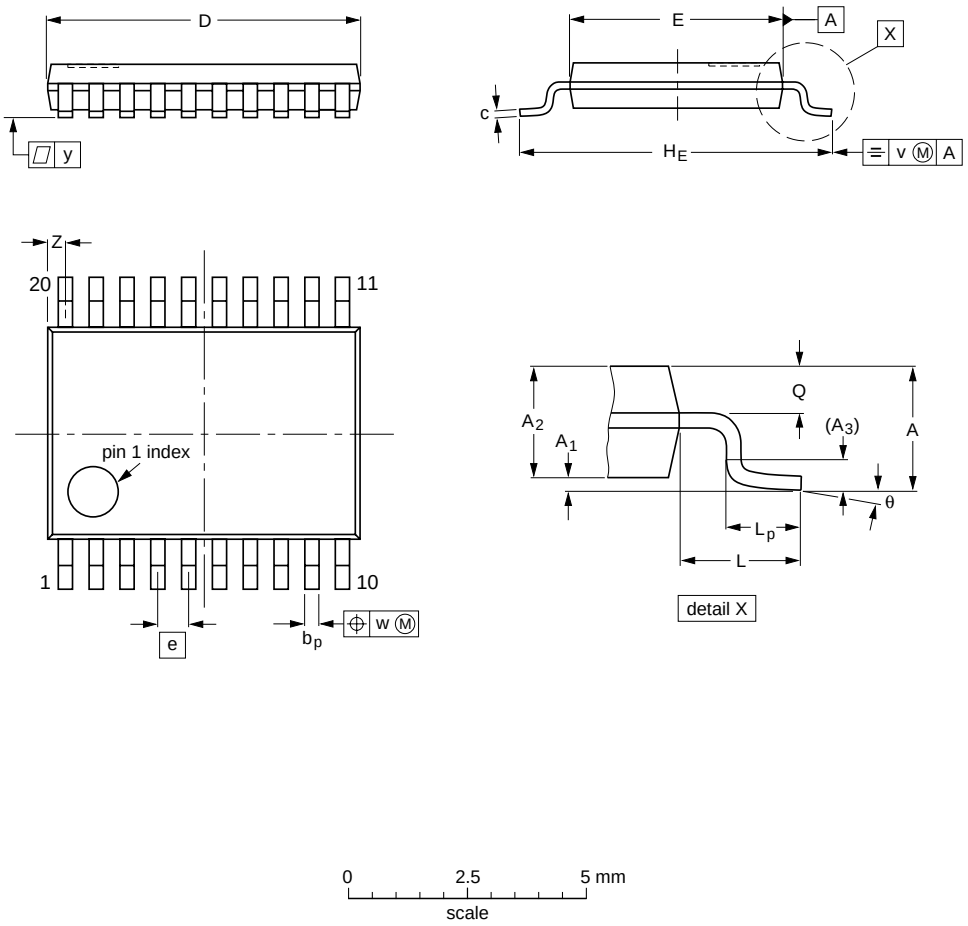
TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT360-1 (TSSOP20)

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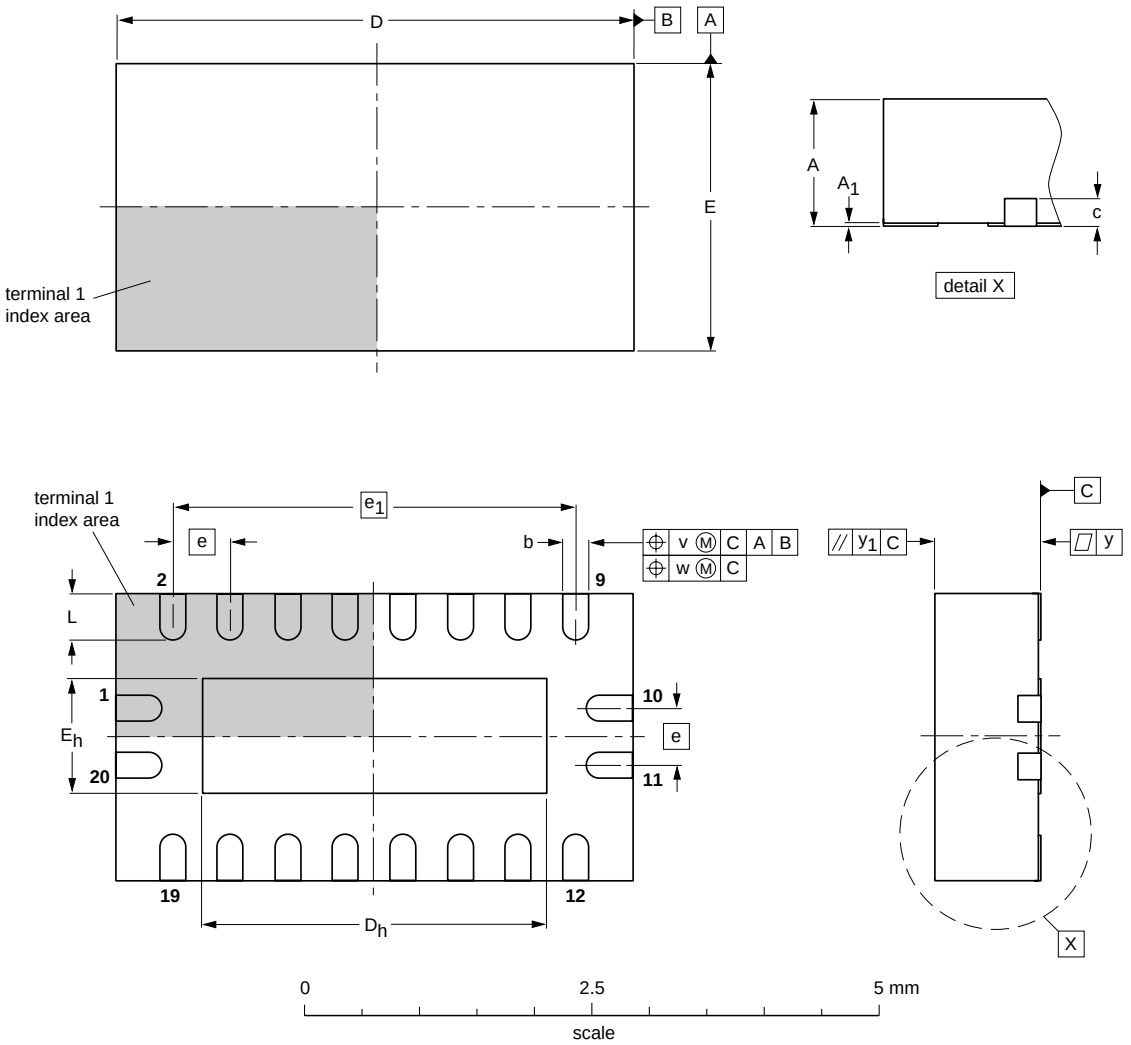
DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 11. Package outline SOT764-1 (DHVQFN20)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charge Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT244_5	20071220	Product data sheet	-	74AHC_AHCT244_4
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3: DHVQFN20 package added. • Section 7: derating values added for DHVQFN20 package. • Section 12: outline drawing added for DHVQFN20 package.			
74AHC_AHCT244_4	20060210	Product data sheet	-	74AHC_AHCT244_3
74AHC_AHCT244_3	19990928	Product specification	-	74AHC_AHCT244_2
74AHC_AHCT244_2	19990224	Product specification	-	74AHC_AHCT244_1
74AHC_AHCT244_1	19980921	Product specification	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

1 General description 1
2 Features 1
3 Ordering information 1
4 Functional diagram 2
5 Pinning information 3
5.1 Pinning 3
5.2 Pin description 3
6 Functional description 4
7 Limiting values 4
8 Recommended operating conditions 5
9 Static characteristics 5
10 Dynamic characteristics 7
11 Waveforms 8
12 Package outline 11
13 Abbreviations 14
14 Revision history 14
15 Legal information 15
15.1 Data sheet status 15
15.2 Definitions 15
15.3 Disclaimers 15
15.4 Trademarks 15
16 Contact information 15
17 Contents 16

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