

Absolute Maximum Ratings

V_{CC} to GND.....-0.3V to +6.0V
 SRT, SWT, SET0, SET1, RESET IN, WDS, MR,
 WDI, to GND.....-0.3V to (V_{CC} + 0.3V)
 RESET (Push-Pull) to GND.....-0.3V to (V_{CC} + 0.3V)
 RESET (Open-Drain) to GND.....-0.3V to +6.0V
 Input Current (All Pins).....±20mA
 Output Current (RESET)±20mA

Continuous Power Dissipation (T_A = +70°C)
 8-Pin SOT23 (derate 8.9mW/°C above +70°C).....714mW
 Operating Temperature Range-40°C to +125°C
 Storage Temperature Range-65°C to +150°C
 Junction Temperature.....+150°C
 Lead Temperature (soldering, 10s)+300°C
 Soldering Temperature (reflow)+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +1.2V to +5.5V, T_A = T_{MIN} to T_{MAX} , unless otherwise specified. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	T_A = 0°C to +125°C		1.0		5.5	V
		T_A = -40°C to 0°C		1.2		5.5	
Supply Current	I_{CC}	$V_{CC} \leq 5.5V$			5	10	μA
		$V_{CC} \leq 3.3V$			4.2	9	
		$V_{CC} \leq 2.0V$			3.7	8	
V_{CC} Reset Threshold	V_{TH}	See V_{TH} selection table	T_A = -40°C to +125°C	$V_{TH} - 2\%$		$V_{TH} + 2\%$	V
Hysteresis	V_{HYST}			0.8			%
V_{CC} Reset Threshold (MAX6752AKA32 Only)		T_A = -40°C to +125°C		3.136		3.224	V
Hysteresis (MAX6752AKA32 Only)	V_{HYST}			0.65	0.80	0.90	%
V_{CC} to Reset Delay		V_{CC} falling from $V_{TH} + 100mV$ to $V_{TH} - 100mV$ at 1mV/μs		20			μs
Reset Timeout Period	t_{RP}	$C_{SRT} = 1500pF$		5.692	7.590	9.487	ms
		$C_{SRT} = 100pF$		0.506			
SRT Ramp Current	I_{RAMP}	$V_{SRT} = 0$ to 1.23V; $V_{CC} = 1.6V$ to 5V		200	250	300	nA
SRT Ramp Threshold	V_{RAMP}	$V_{CC} = 1.6V$ to 5V (V_{RAMP} rising)		1.173	1.235	1.297	V
Normal Watchdog Timeout Period (MAX6746–MAX6751)	t_{WD}	$C_{SWT} = 1500pF$		5.692	7.590	9.487	ms
		$C_{SWT} = 100pF$		0.506			
Extended Watchdog Timeout (MAX6746–MAX6751)	t_{WD}	$C_{SWT} = 1500pF$		728.6	971.5	1214.4	ms
		$C_{SWT} = 100pF$		64.77			
Slow Watchdog Period (MAX6752/MAX6753)	t_{WD2}	$C_{SWT} = 1500pF$		728.6	971.5	1214.4	ms
		$C_{SWT} = 100pF$		64.77			
Fast Watchdog Timeout Period, SET Ratio = 8, (MAX6752/MAX6753)	t_{WD1}	$C_{SWT} = 1500pF$		91.08	121.43	151.80	ms
		$C_{SWT} = 100pF$		8.09			
Fast Watchdog Timeout Period, SET Ratio = 16, (MAX6752/MAX6753)	t_{WD1}	$C_{SWT} = 1500pF$		45.53	60.71	75.89	ms
		$C_{SWT} = 100pF$		4.05			

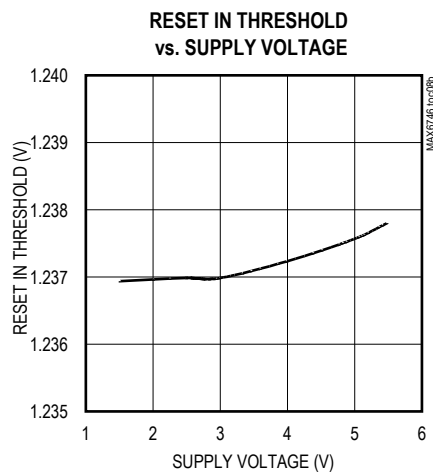
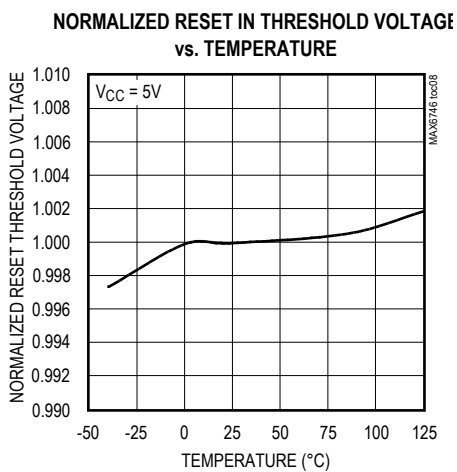
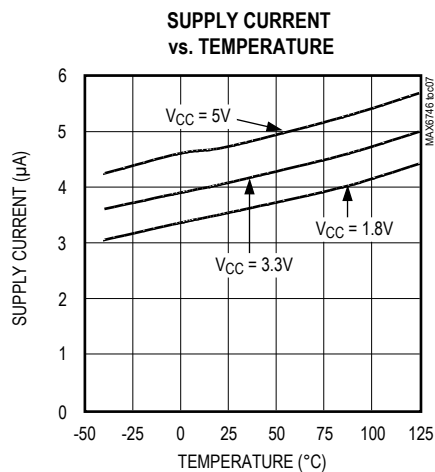
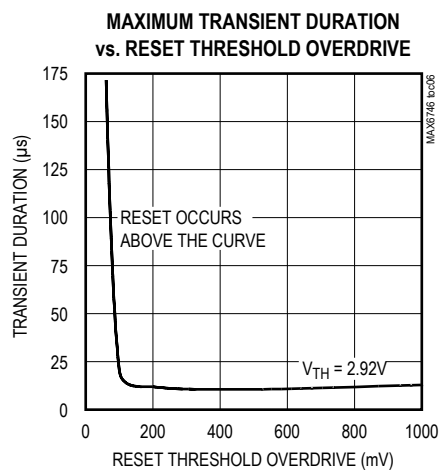
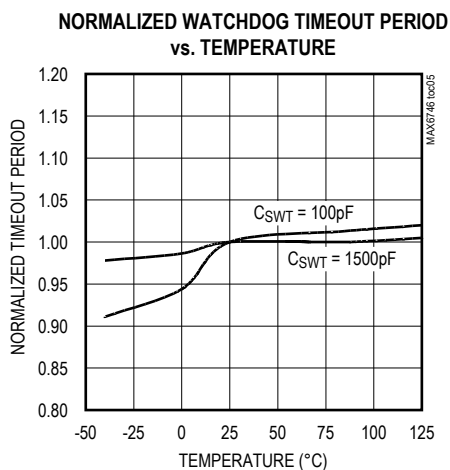
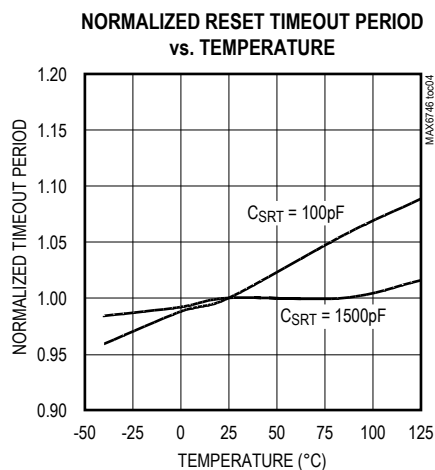
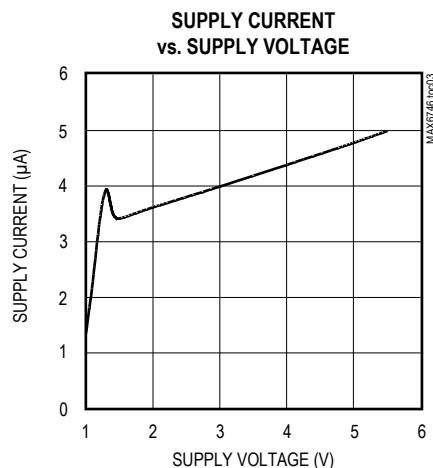
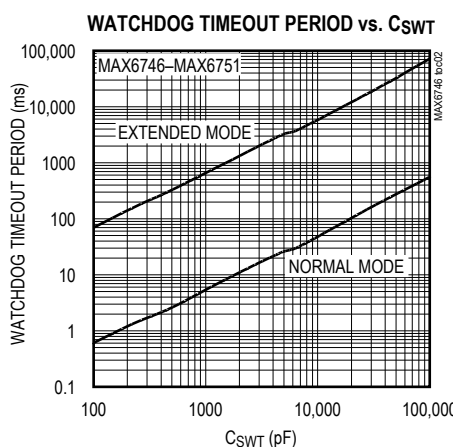
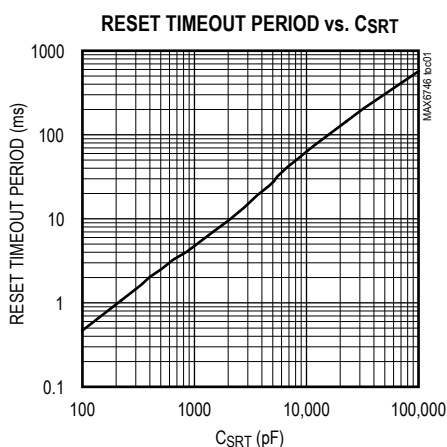
Electrical Characteristics (continued)

($V_{CC} = +1.2V$ to $+5.5V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise specified. Typical values are at $V_{CC} = +5V$ and $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Fast Watchdog Timeout Period, SET Ratio = 64, (MAX6752/MAX6753)	tWD1	CSWT = 1500pF		11.38	15.18	18.98	ms
		CSWT = 100pF		1.01			
Fast Watchdog Minimum Period (MAX6752/MAX6753)				2000			ns
SWT Ramp Current	IRAMP	VSWT = 0 to 1.23V, VCC = 1.6V to 5V		200	250	300	nA
SWT Ramp Threshold	VRAMP	VCC = 1.6V to 5V (VRAMP rising)		1.173	1.235	1.297	V
RESET Output-Voltage Low Open-Drain, Push-Pull (Asserted)	VOL	VCC ≥ 1.0V, ISINK = 50μA		0.3			V
		VCC ≥ 2.7V, ISINK = 1.2mA		0.3			
		VCC ≥ 4.5V, ISINK = 3.2mA		0.4			
RESET Output-Voltage High, Push-Pull (Not Asserted)	VOH	VCC ≥ 1.8V, ISOURCE = 200μA		0.8 x VCC			V
		VCC ≥ 2.25V, ISOURCE = 500μA		0.8 x VCC			
		VCC ≥ 4.5V, ISOURCE = 800μA		0.8 x VCC			
RESET Output Leakage Current, Open Drain	ILKG	VCC > VTH, reset not asserted, VRESET = 5.5V		1.0			μA
DIGITAL INPUTS (MR, SET0, SET1, WDI, WDS)							
Input Logic Levels	VIL	VCC ≥ 4.0V		0.8			V
	VIH			2.4			
	VIL	VCC < 4.0V		0.3 x VCC			
	VIH			0.7 x VCC			
MR Minimum Pulse Width				1			μs
MR Glitch Rejection				100			ns
MR-to-RESET Delay				200			ns
MR Pullup Resistance		Pullup to VCC		12	20	28	kΩ
WDI Minimum Pulse Width				300			ns
RESET IN							
RESET IN Threshold	VRESET IN		TA = -40°C to +125°C	1.216	1.235	1.254	V
RESET IN Leakage Current	IRESET IN			-50	±1	+50	nA
RESET IN to RESET Delay		RESET IN falling at 1mV/μs			20		μs

Note 1: Production testing done at $T_A = +25^{\circ}C$. Over temperature limits are guaranteed by design.

Typical Operating Characteristics

 $(V_{CC} = +5V, T_A = +25^\circ C, \text{ unless otherwise noted.})$ 

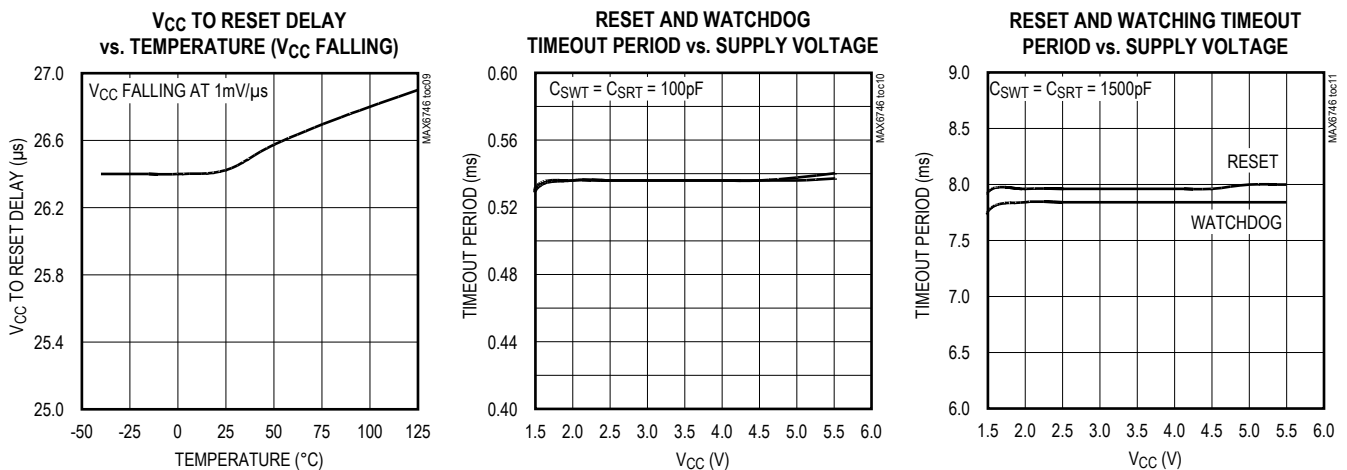
MAX6746–MAX6753

µP Reset Circuits with Capacitor-Adjustable

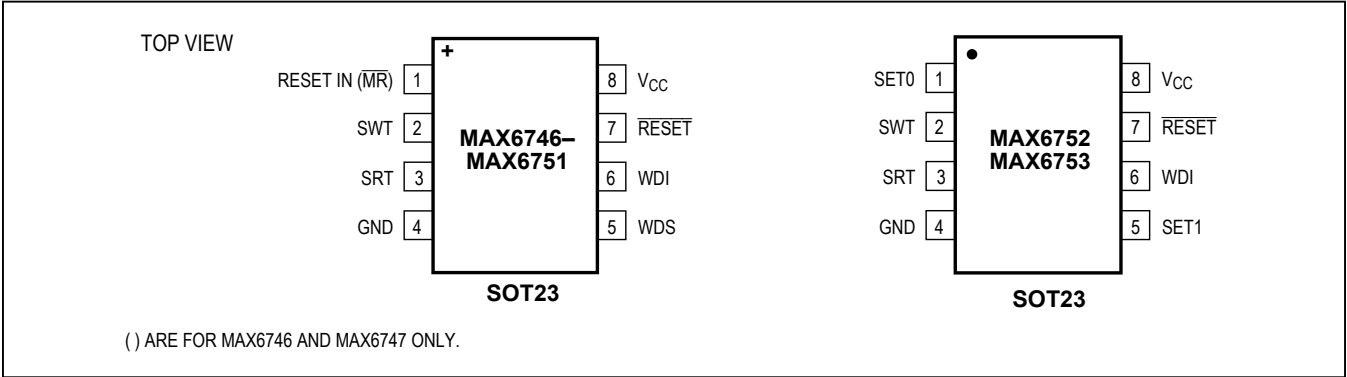
Reset/Watchdog Timeout Delay

Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)



Pin Configurations



Pin Descriptions

PIN			NAME	FUNCTION
MAX6746 MAX6747	MAX6748– MAX6751	MAX6752 MAX6753		
1	—	—	MR	Manual-Reset Input. Pull MR low to manually reset the device. Reset remains asserted for the reset timeout period after MR is released.
—	1	—	RESET IN	Reset Input. High-impedance input to the adjustable reset comparator. Connect RESET IN to the center point of an external resistor-divider to set the threshold of the externally monitored voltage.
—	—	1	SET0	Logic Input. SET0 selects watchdog window ratio or disables the watchdog timer. See Table 1.

Pin Descriptions (continued)

PIN			NAME	FUNCTION
MAX6746 MAX6747	MAX6748– MAX6751	MAX6752 MAX6753		
2	2	2	SWT	<p>Watchdog Timeout Input.</p> <p>MAX6746–MAX6751: Connect a capacitor between SWT and ground to set the basic watchdog timeout period (t_{WD}). Determine the period by the formula $t_{WD} = 4.94 \times 10^6 \times C_{SWT}$ with t_{WD} in seconds and C_{SWT} in Farads. Extend the basic watchdog timeout period by using the WDS input. Connect SWT to ground to disable the watchdog timer function.</p> <p>MAX6752/MAX6753: Connect a capacitor between SWT and ground to set the slow watchdog timeout period (t_{WD2}). Determine the slow watchdog period by the formula: $t_{WD2} = 0.65 \times 10^9 \times C_{SWT}$ with t_{WD2} in seconds and C_{SWT} in Farads. The fast watchdog timeout period is set by pin strapping SET0 and SET1 (Connect SET0 high and SET1 low to disable the watchdog timer function.) See Table 1.</p>
3	3	3	SRT	Reset Timeout Input. Connect a capacitor from SRT to GND to select the reset timeout period. Determine the period as follows: $t_{RP} = 4.94 \times 10^6 \times C_{SRT}$ with t_{RP} in seconds and C_{SRT} in Farads.
4	4	4	GND	Ground
5	5	—	WDS	Watchdog Select Input. WDS selects the watchdog mode. Connect WDS to ground to select normal mode and the watchdog timeout period. Connect WDS to V_{CC} to select extended mode, multiplying the basic timeout period by a factor of 128. A change in the state of WDS clears the watchdog timer.
—	—	5	SET1	Logic Input. SET1 selects the watchdog window ratio or disables the watchdog timer. See Table 1.
6	6	6	WDI	<p>Watchdog Input.</p> <p>MAX6746–MAX6751: A falling transition must occur on WDI within the selected watchdog timeout period or a reset pulse occurs. The watchdog timer clears when a transition occurs on WDI or whenever \overline{RESET} is asserted. Connect SWT to ground to disable the watchdog timer function.</p> <p>MAX6752/MAX6753: WDI falling transitions within periods shorter than t_{WD1} or longer than t_{WD2} force \overline{RESET} to assert low for the reset timeout period. The watchdog timer begins to count after \overline{RESET} is deasserted. The watchdog timer clears when a valid transition occurs on WDI or whenever \overline{RESET} is asserted. Connect SET0 high and SET1 low to disable the watchdog timer function. See the <i>Watchdog Timer</i> section.</p>
7	7	7	\overline{RESET}	Push/Pull or Open-Drain Reset Output. \overline{RESET} asserts whenever V_{CC} or \overline{RESET} IN drops below the selected reset threshold voltage (V_{TH} or $V_{RESET\ IN}$, respectively) or manual reset is pulled low. \overline{RESET} remains low for the reset timeout period after all reset conditions are deasserted, and then goes high. The watchdog timer triggers a reset pulse (t_{RP}) whenever a watchdog fault occurs.
8	8	8	V_{CC}	Supply Voltage. V_{CC} is the power-supply input and the input for fixed threshold V_{CC} monitor.

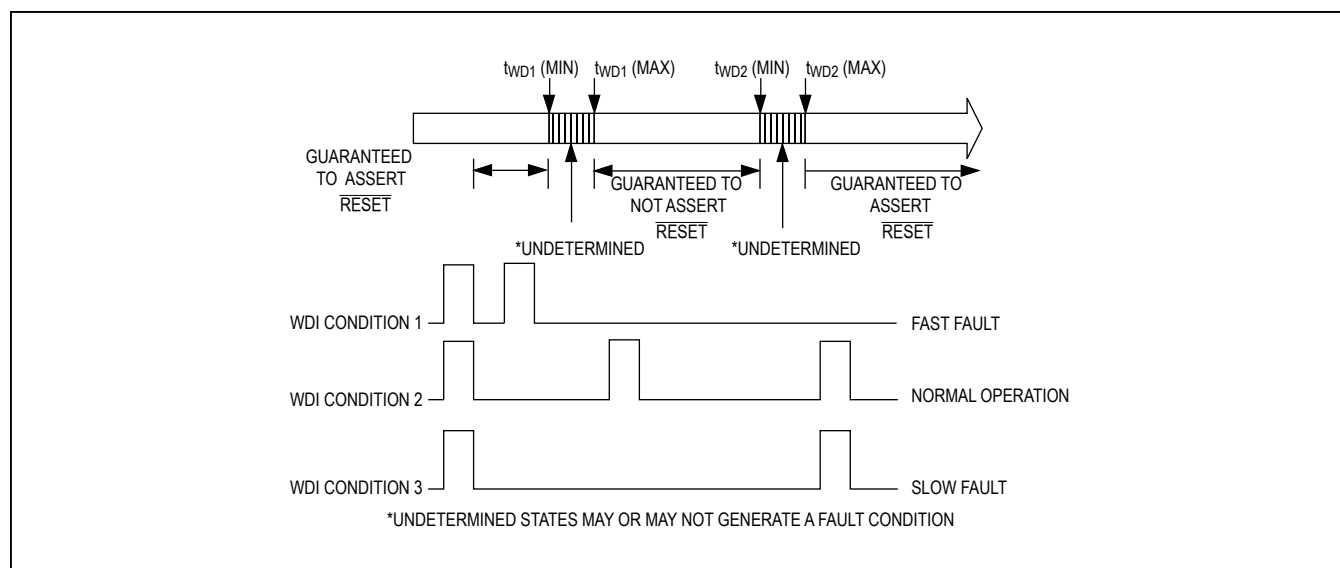


Figure 1. MAX6752/MAX6753 Detailed Watchdog Input Timing Relationship

Detailed Description

The MAX6746–MAX6753 assert a reset signal whenever the V_{CC} supply voltage or RESET IN falls below its reset threshold. The reset output remains asserted for the reset timeout period after V_{CC} and RESET IN rise above its respective reset threshold. A watchdog timer triggers a reset pulse whenever a watchdog fault occurs.

The reset and watchdog delays are adjustable with external capacitors. The MAX6746–MAX6751 contain a watchdog select input that extends the watchdog timeout period to 128x.

The MAX6752 and MAX6753 have a sophisticated watchdog timer that detects when the processor is running outside an expected window of operation. The watchdog signals a fault when the input pulses arrive too early (faster than the selected t_{WD1} timeout period) or too late (slower than the selected t_{WD2} timeout period) (see Figure 1).

Reset Output

The reset output is typically connected to the reset input of a μP. A μP's reset input starts or restarts the μP in a known state. The MAX6746–MAX6753 μP supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down, and brownout conditions (see the [Typical Operating Circuit](#)). RESET changes from high to low whenever the monitored voltage, RESET IN and/or V_{CC} drop below the reset threshold voltages. Once $V_{RESET IN}$ and/or V_{CC} exceeds its respective reset threshold voltage(s), RESET remains low for the reset timeout period, then goes high.

RESET is guaranteed to be in the correct logic state for V_{CC} greater than 1V. For applications requiring valid reset logic when V_{CC} is less than 1V, see the [Ensuring a Valid RESET Down to \$V_{CC} = 0V\$ \(Push-Pull RESET\)](#) section.

RESET IN Threshold

The MAX6748–MAX6751 monitor the voltage on RESET IN using an adjustable reset threshold ($V_{RESET IN}$) set with an external resistor voltage-divider (Figure 2). Use the following formula to calculate the externally monitored voltage (V_{MON_TH}):

$$V_{MON_TH} = V_{RESET IN} \times (R1 + R2) / R2$$

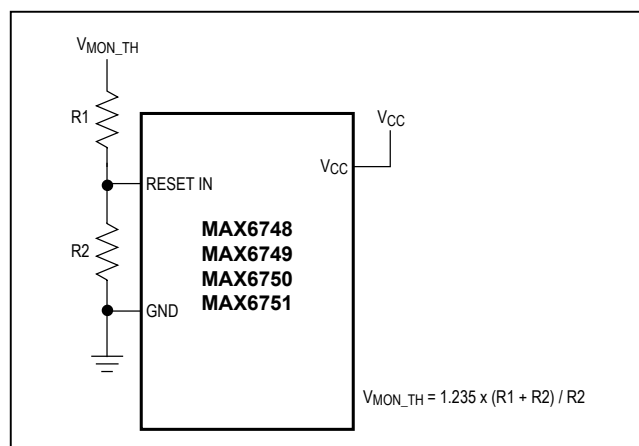


Figure 2. Calculating the Monitored Threshold Voltage (V_{MON_TH})

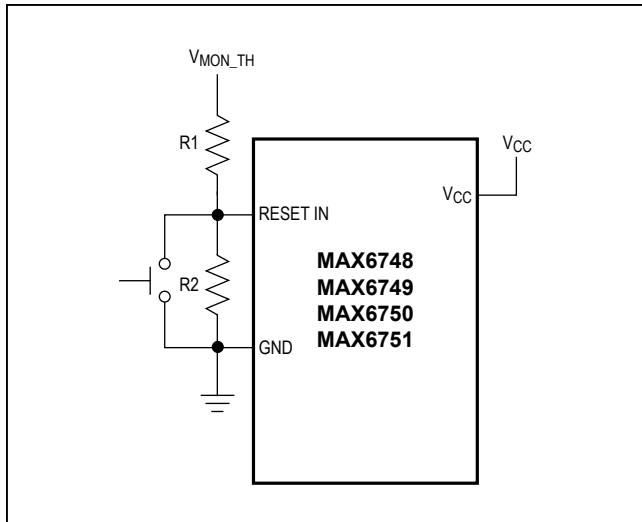


Figure 3. Adding an External Manual-Reset Function to the MAX6748–MAX6751

where V_{MON_TH} is the desired reset threshold voltage and V_{TH} is the reset input threshold (1.235V). Resistors R1 and R2 can have very high values to minimize current consumption due to low leakage currents. Set R2 to some conveniently high value (500kΩ, for example) and calculate R1 based on the desired reset threshold voltage, using the following formula:

$$R1 = R2 \times (V_{MON_TH}/V_{RESET\ IN} - 1) (\Omega)$$

The MAX6748 and MAX6749 do not monitor V_{CC} supply voltage; therefore, V_{CC} must be greater than 1.5V to guarantee RESET IN threshold accuracy and

timing performance. The MAX6748 and MAX6749 can be configured to monitor V_{CC} voltage by connecting V_{CC} to V_{MON_TH} .

Dual-Voltage Monitoring (MAX6750/MAX6751)

The MAX6750 and MAX6751 contain both factory-trimmed threshold voltages and an adjustable reset threshold input, allowing the monitoring of two voltages, V_{CC} and V_{MON_TH} (see Figure 2). RESET is asserted when either of the voltages fall below its respective threshold voltages.

Manual Reset (MAX6746/MAX6747)

Many μP-based products require manual-reset capability to allow an operator or external logic circuitry to initiate a reset. The manual-reset input (\overline{MR}) can connect directly to a switch without an external pullup resistor or debouncing network. \overline{MR} is internally pulled up to V_{CC} and, therefore, can be left unconnected if unused.

\overline{MR} is designed to reject fast, falling transients (typically 100ns pulses) and must be held low for a minimum of 1μs to assert the reset output. A 0.1μF capacitor from \overline{MR} to ground provides additional noise immunity. After \overline{MR} transitions from low to high, reset remains asserted for the duration of the reset timeout period.

A manual-reset option can easily be implemented with the MAX6748–MAX6751 by connecting a normally open momentary switch in parallel with R2 (Figure 3). When the switch is closed, the voltage on RESET IN goes to zero, initiating a reset. Similar to the MAX6746/MAX6747 manual reset, reset remains asserted while the voltage at RESET IN is zero and for the reset timeout period after the switch is opened.

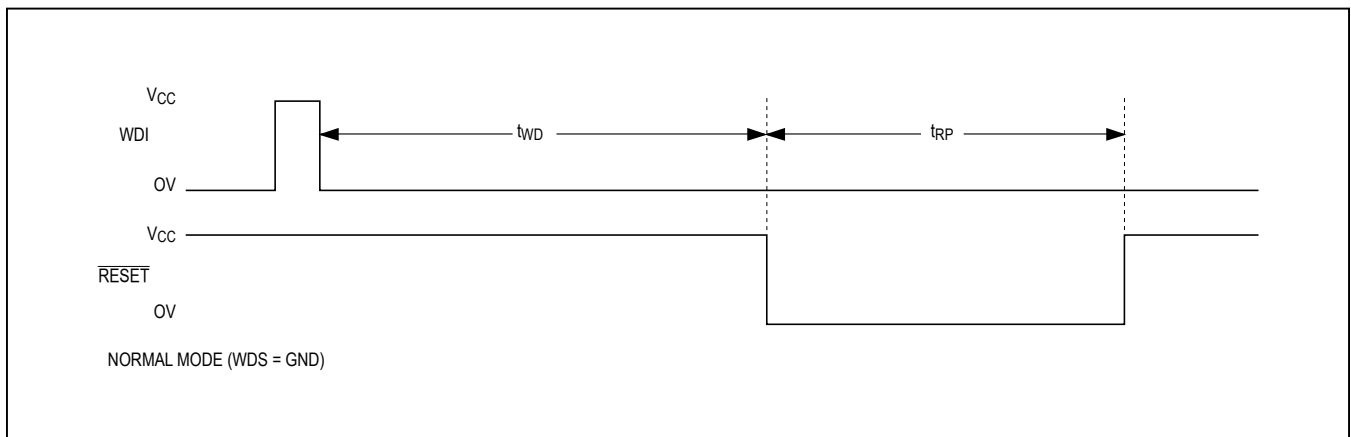


Figure 4a. Watchdog Timing Diagram, WDS = GND

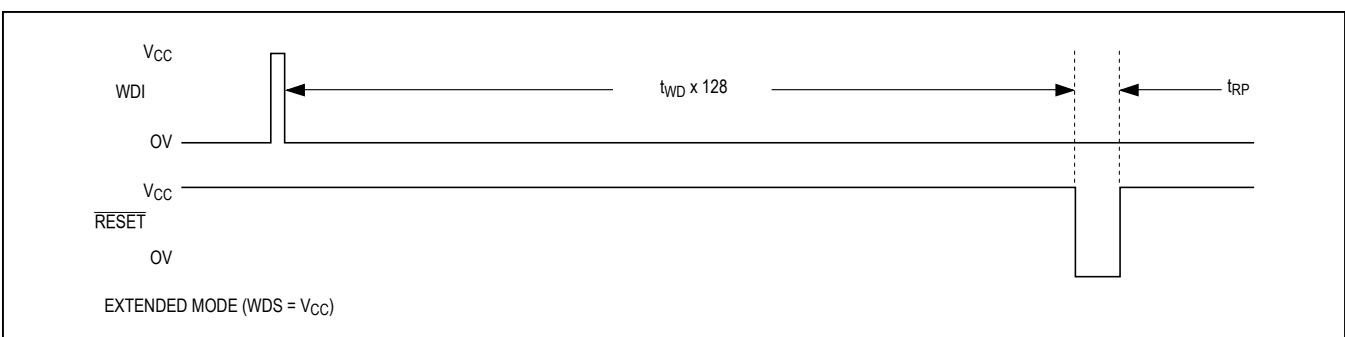


Figure 4b. Watchdog Timing Diagram, WDS = V_{CC}

Watchdog Timer

MAX6746–MAX6751

The watchdog's circuit monitors the μP's activity. If the μP does not toggle the watchdog input (WDI) within t_{WD} (user-selected), \overline{RESET} asserts for the reset timeout period. The internal watchdog timer is cleared by any event that asserts \overline{RESET} , by a falling transition at WDI (which can detect pulses as short as 300ns), or by a transition at WDS. The watchdog timer remains cleared while reset is asserted; as soon as reset is released, the timer starts counting.

The MAX6746–MAX6751 feature two modes of watchdog operation: normal mode and extended mode. In normal mode (Figure 4a), the watchdog timeout period is determined by the value of the capacitor connected between SWT and ground. In extended mode (Figure 4b), the watchdog timeout period is multiplied by 128. For example, in extended mode, a 0.1μF capacitor gives a watchdog timeout period of 65s (see the Extended-Mode Watchdog Timeout Period vs. C_{SWT} graph in the [Typical Operating Circuit](#)). To disable the watchdog timer function, connect SWT to ground.

MAX6752/MAX6753

The MAX6752 and MAX6753 have a windowed watchdog timer that asserts \overline{RESET} for the adjusted reset timeout period when the watchdog recognizes a fast watchdog fault ($t_{WDI} < t_{WD1}$), or a slow watchdog fault (period $> t_{WD2}$). The reset timeout period is adjusted independently of the watchdog timeout period.

The slow watchdog period (t_{WD2}) is calculated as follows:

$$t_{WD2} = 0.65 \times 10^9 \times C_{SWT}$$

with t_{WD2} in seconds and C_{SWT} in Farads.

The fast watchdog period (t_{WD1}) is selectable as a ratio from the slow watchdog fault period (t_{WD2}). Select the fast watchdog period by pin strapping SET0 and SET1, where high is V_{CC} and low is GND. Table 1 illustrates

Table 1. Min/Max Watchdog Setting

SET0	SET1	RATIO
Low	Low	8
Low	High	16
High	Low	Watchdog Disabled
High	High	64

the SET0 and SET1 configuration for the 8, 16, and 64 window ratio (t_{WD2}/t_{WD1}).

For example, if C_{SWT} is 1500pF, and SET0 and SET1 are low, then t_{WD2} is 975ms (typ) and t_{WD1} is 122ms (typ).

\overline{RESET} asserts if the watchdog input has two falling edges too close to each other (faster than t_{WD1}) (Figure 5a) or falling edges that are too far apart (slower than t_{WD2}) (Figure 5b). Normal watchdog operation is displayed in Figure 5c. The internal watchdog timer is cleared when a WDI falling edge is detected within the valid watchdog window or when \overline{RESET} is deasserted. All WDI inputs are ignored while \overline{RESET} is asserted.

The watchdog timer begins to count after \overline{RESET} is deasserted. The watchdog timer clears and begins to count after a valid WDI falling logic input. WDI falling transitions within periods shorter than t_{WD1} or longer than t_{WD2} force \overline{RESET} to assert low for the reset timeout period. WDI falling transitions within the t_{WD1} and t_{WD2} window do not assert \overline{RESET} . WDI transitions between $t_{WD1}(\min)$ and $t_{WD1}(\max)$ or $t_{WD2}(\min)$ and $t_{WD2}(\max)$ are not guaranteed to assert or deassert \overline{RESET} . To guarantee that the window watchdog does not assert \overline{RESET} , strobe WDI between $t_{WD1}(\max)$ and $t_{WD2}(\min)$. The watchdog timer is cleared when \overline{RESET} is asserted or after a falling transition on WDI, or after a state change on SET0 or SET1. Disable the watchdog timer by connecting SET0 high and SET1 low.

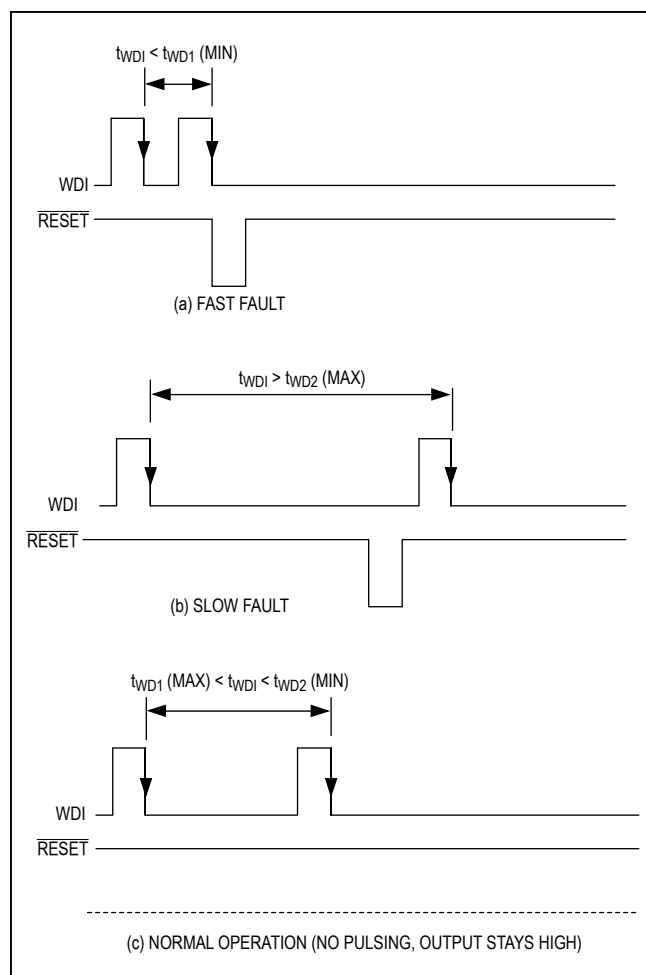


Figure 5. MAX6752/MAX6753 Window Watchdog Diagram

Applications Information

Selecting Reset/Watchdog Timeout Capacitor

The reset timeout period is adjustable to accommodate a variety of μP applications. Adjust the reset timeout period (t_{RP}) by connecting a capacitor (C_{SRT}) between SRT and ground. Calculate the reset timeout capacitor as follows:

$$C_{SRT} = t_{RP} / (4.94 \times 10^6)$$

with t_{RP} in seconds and C_{SRT} in Farads.

The watchdog timeout period is adjustable to accommodate a variety of μP applications. With this feature, the watchdog timeout can be optimized for software execution. The programmer can determine how often the watchdog timer should be serviced. Adjust the watchdog timeout period (t_{WD}) by connecting a specific value capacitor (C_{SWT}) between SWT and GND.

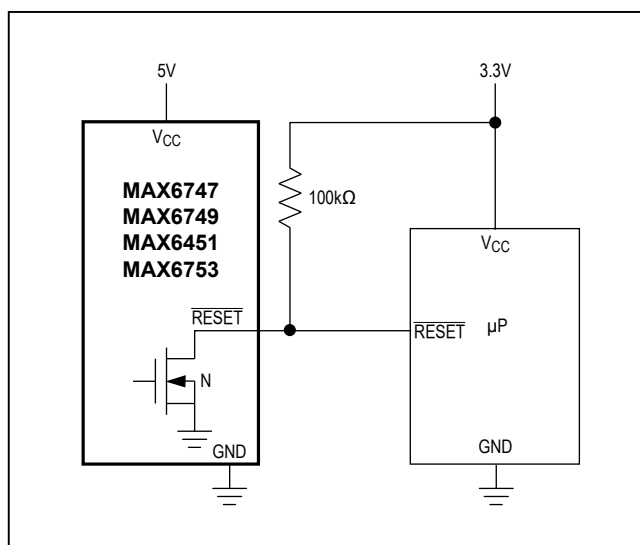


Figure 6. Interfacing to Other Voltage Levels

For normal mode operation, calculate the watchdog timeout capacitor as follows:

$$C_{SWT} = t_{WD} / (4.94 \times 10^6)$$

with t_{WD} in seconds and C_{SWT} in Farads.

For the MAX6752 and MAX6753 windowed watchdog function, calculate the slow watchdog period, t_{WD2} as follows:

$$t_{WD2} = 0.65 \times 10^9 \times C_{SWT}$$

C_{SRT} and C_{SWT} must be a low-leakage ($< 10\text{nA}$) type capacitor. Ceramic capacitors are recommended.

Transient Immunity

In addition to issuing a reset to the μP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration supply transients (glitches). The Maximum Transient Duration vs. Reset Threshold Overdrive graph in the [Typical Operating Characteristics](#) shows this relationship.

The area below the curves of the graph is the region in which these devices typically do not generate a reset pulse. This graph was generated using a falling pulse applied to V_{CC} , starting above the actual reset threshold (V_{TH}) and ending below it by the magnitude indicated (reset threshold overdrive). As the magnitude of the transient increases (farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 50μs or less does not cause a reset pulse to be issued.

Interfacing to Other Voltages for Logic Compatibility

The open-drain $\overline{\text{RESET}}$ output can be used to interface to a μP with other logic levels. As shown in [Figure 6](#), the open-drain output can be connected to voltages from 0 to 6V.

Generally, the pullup resistor connected to $\overline{\text{RESET}}$ connects to the supply voltage that is being monitored at the IC's V_{CC} pin. However, some systems can use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply. Keep in mind that as the supervisor's V_{CC} decreases towards 1V, so does the IC's ability to sink current at $\overline{\text{RESET}}$. Also, with any pullup resistor, $\overline{\text{RESET}}$ is pulled high as V_{CC} decays toward zero. The voltage where this occurs depends on the pullup resistor value and the voltage to which it is connected.

Ensuring a Valid $\overline{\text{RESET}}$ Down to $V_{CC} = 0\text{V}$ (Push-Pull $\overline{\text{RESET}}$)

When V_{CC} falls below 1V, $\overline{\text{RESET}}$ current sinking capabilities decline drastically. The high-impedance CMOS logic inputs connected to $\overline{\text{RESET}}$ can drift to undetermined voltages. This presents no problems in most applications, since most μPs and other circuitry do not operate with V_{CC} below 1V.

In those applications where $\overline{\text{RESET}}$ must be valid down to 0V, add a pulldown resistor between $\overline{\text{RESET}}$ and GND for the MAX6746/MAX6748/MAX6750/MAX6752 push/pull outputs. The resistor sinks any stray leakage currents, holding $\overline{\text{RESET}}$ low ([Figure 7](#)). The value of the pulldown resistor is not critical; 100kΩ is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground. The external pulldown cannot be used with the open-drain reset outputs.

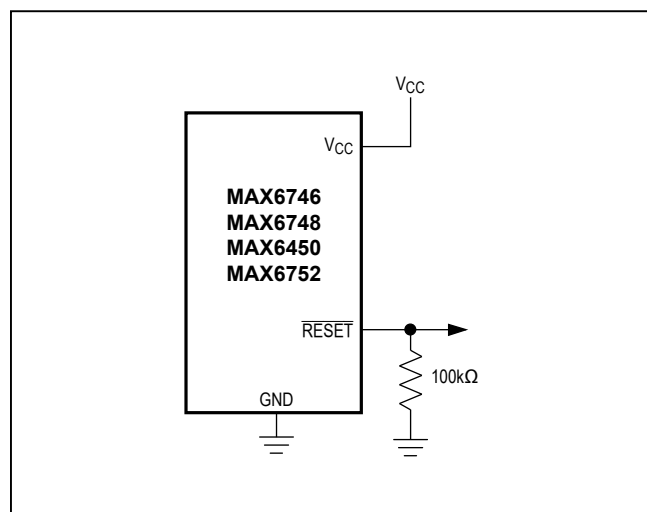


Figure 7. Ensuring $\overline{\text{RESET}}$ Valid to $V_{CC} = 0\text{V}$

Table 2. Reset Threshold Voltage Suffix
(T_A = -40°C to +125°C)

SUFFIX	MIN	TYP	MAX
50	4.900	5.000	5.100
49	4.802	4.900	4.998
48	4.704	4.800	4.896
47	4.606	4.700	4.794
46	4.533	4.625	4.718
45	4.410	4.500	4.590
44	4.288	4.375	4.463
43	4.214	4.300	4.386
42	4.116	4.200	4.284
41	4.018	4.100	4.182
40	3.920	4.000	4.080
39	3.822	3.900	3.978
38	3.724	3.800	3.876
37	3.626	3.700	3.774
36	3.528	3.600	3.672
35	3.430	3.500	3.570
34	3.332	3.400	3.468
33	3.234	3.300	3.366
32	3.136	3.200	3.264
32A (MAX6752AKA32 Only)	3.136	3.200	3.224
31	3.014	3.075	3.137
30	2.940	3.000	3.060
29	2.867	2.925	2.984
28	2.744	2.800	2.856
27	2.646	2.700	2.754
26	2.573	2.625	2.678
25	2.450	2.500	2.550
24	2.352	2.400	2.448
23	2.267	2.313	2.359
22	2.144	2.188	2.232
21	2.058	2.100	2.142
20	1.960	2.000	2.040
19	1.862	1.900	1.938
18	1.764	1.800	1.836
17	1.632	1.665	1.698
16	1.544	1.575	1.607

Table 3. Standard Version Table

PART	TOP MARK
MAX6746KA16	AEDI
MAX6746KA23	AEDJ
MAX6746KA26	AEDK
MAX6746KA29	AALN
MAX6746KA46	AEDL
MAX6747KA16	AALO
MAX6747KA23	AEDM
MAX6747KA26	AEDN
MAX6747KA29	AEDO
MAX6747KA46	AEDP
MAX6748KA	AALP
MAX6749KA	AALQ
MAX6750KA16	AEDQ
MAX6750KA23	AALR
MAX6750KA26	AEDR
MAX6750KA29	AEDS
MAX6750KA46	AEDT
MAX6751KA16	AEDU
MAX6751KA23	AEDV
MAX6751KA26	AEDW
MAX6751KA29	AEDX
MAX6751KA46	AEDY
MAX6752KA16	AEDZ
MAX6752KA23	AEEA
MAX6752KA26	AALT
MAX6752KA29	AEEB
MAX6752KA46	AEEC
MAX6753KA16	AEEH
MAX6753KA23	AEEE
MAX6753KA26	AEEF
MAX6753KA29	AEEG
MAX6753KA46	AEEH

Note: Standard versions are shown in **bold**. There is a 2500-piece minimum order increment for standard versions.

Sample stock is typically held on standard versions only.
Nonstandard versions require a minimum order increment of 10,000 pieces. Contact factory for availability

Selector Guide

PART	FIXED V _{CC} RESET THRESHOLD	ADJUSTABLE RESET THRESHOLD	STANDARD WATCHDOG TIMER	MIN/MAX WATCHDOG TIMER	PUSH/ PULL RESET	OPEN-DRAIN RESET	MANUAL- RESET INPUT
MAX6746	X	—	X	—	X	—	X
MAX6747	X	—	X	—	—	X	X
MAX6748	—	X	X	—	X	—	—
MAX6749	—	X	X	—	—	X	—
MAX6750	X	X	X	—	X	—	—
MAX6751	X	X	X	—	—	X	—
MAX6752	X	—	—	X	X	—	—
MAX6753	X	—	—	X	—	X	—

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6746KA__-T	-40°C to +125°C	8 SOT23
MAX6746KA__+T	-40°C to +125°C	8 SOT23
MAX6747KA__+T	-40°C to +125°C	8 SOT23
MAX6746KA__ /V+T	-40°C to +125°C	8 SOT23
MAX6747KA__-T	-40°C to +125°C	8 SOT23
MAX6747KA__ /V+T	-40°C to +125°C	8 SOT23
MAX6748KA+T	-40°C to +125°C	8 SOT23
MAX6749KA+T	-40°C to +125°C	8 SOT23
MAX6750KA__+T	-40°C to +125°C	8 SOT23
MAX6750KA__ /V+T	-40°C to +125°C	8 SOT23
MAX6751KA__-T	-40°C to +125°C	8 SOT23
MAX6751KA__+T	-40°C to +125°C	8 SOT23
MAX6751KA__ /V+T*	-40°C to +125°C	8 SOT23
MAX6752KA__+T	-40°C to +125°C	8 SOT23
MAX6752KA__ /V+T*	-40°C to +125°C	8 SOT23
MAX6752AKA32+T	-40°C to +125°C	8 SOT23
MAX6752AKA32/V+T*	-40°C to +125°C	8 SOT23
MAX6753KA__-T	-40°C to +125°C	8 SOT23
MAX6753KA__+T	-40°C to +125°C	8 SOT23
MAX6753KA__ /V+T	-40°C to +125°C	8 SOT23

Note: “__” represents the two number suffix needed when ordering the reset threshold voltage value for the MAX6746/MAX6747 and MAX6750–MAX6753. The reset threshold voltages are available in approximately 100mV increments. Table 2 contains the suffix and reset factory-trimmed voltages. All devices are available in tape-and-reel only. There is a 2500-piece minimum order increment for standard versions (see Table 3). Sample stock is typically held on standard versions only. Nonstandard versions require a minimum order increment of 10,000 pieces. Contact factory for availability. Devices are available in both leaded and lead(Pb)-free packaging. +Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

/V denotes an automotive qualified part.

*Future product—contact factory for availability.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SOT23	K8+5, K8-5	21-0078	90-0176

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/02	Initial release	—
3	12/05	Added the lead-free notation	1
4	9/10	Added the automotive version of the MAX6746 and the MAX6753 and revised the <i>Typical Operating Characteristics</i>	1, 4
5	12/10	Added the automotive version of the MAX6750	1
6	4/11	Added the automotive version of the MAX6747	1
7	12/13	Added the automotive version of the MAX6751	1
8	2/14	Added a future product reference to MAX6751KA__ /V+T	1
9	5/14	Corrected typo	10
10	6/14	Added the automotive version of the MAX6752	1
11	9/15	Added MAX6752A to data sheet with new limits	2, 12, 14
12	12/15	Added lead-free part numbers to <i>Ordering Information</i> table and lead-free package code to <i>Package Information</i> table	14
13	2/16	Added MAX6752AKA32+T to <i>Ordering Information</i> table	14
14	9/16	Updated t_{WD} equation value in <i>Pin Configuration</i> table and <i>Applications Information</i> section	6, 10

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