DATA SHEET

SKY12345-362LF: 0.7-4.0 GHz Five-Bit Digital Attenuator with Serial-to-Parallel Driver (0.5 dB LSB)

Applications

- Base stations
- Wireless and RF data
- Wireless local loop gain control circuits

Features

- Broadband operation: 0.7 to 4.0 GHz
- Attenuation: 15.5 dB
- LSB attenuation: 0.5 dB
- Low insertion loss: 1 dB @ 900 MHz
- Positive voltage operation: 5 V
- Integrated silicon serial-to-parallel driver
- Small, QFN (24-pin, 4 x 4 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

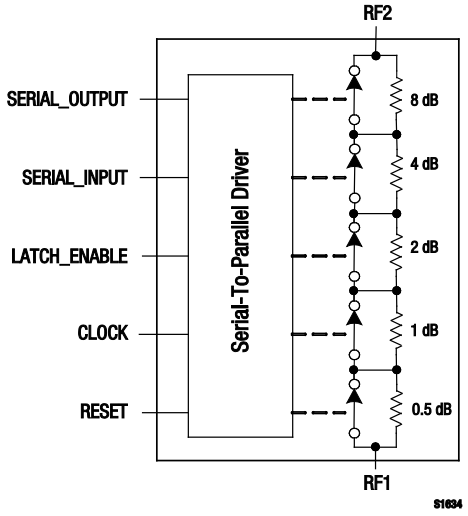


Figure 1. SKY12345-362LF Block Diagram

NEW **Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.**

Description

The SKY12345-362LF is a GaAs FET five-bit digital attenuator I/C with a serial-to-parallel driver. The device is provided in a 4 x 4 mm, 24-pin Quad Flat No-Lead (QFN) package.

The SKY12345-362LF is particularly suited for applications in which high attenuation accuracy, low insertion loss, and low intermodulation products are required.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

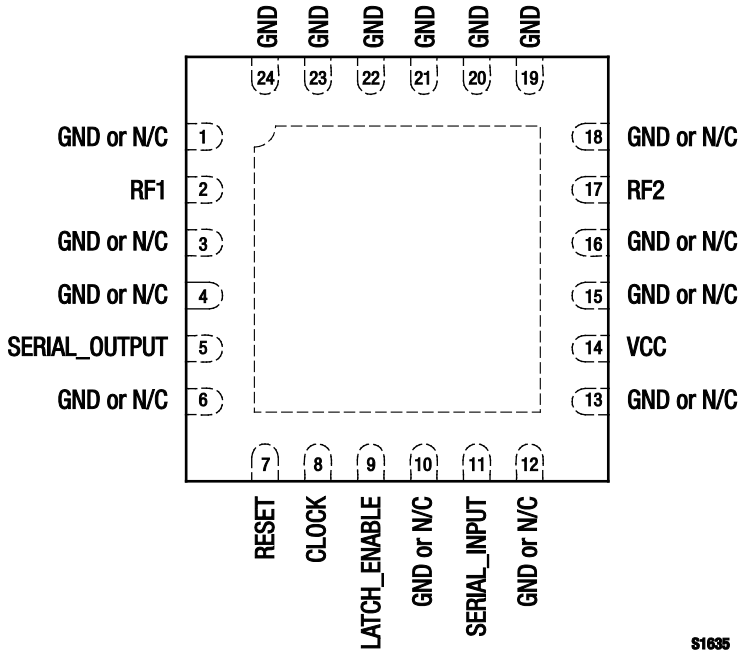


Figure 2. SKY12345-362LF Pinout – 24-Pin QFN
(Top View)

Table 1. SKY12345-362LF Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	GND or N/C	Ground or no connection	13	GND or N/C	Ground or no connection
2	RF1	RF input/output. Must be DC blocked.	14	VCC	Fixed bias for SPI
3	GND or N/C	Ground or no connection	15	GND or N/C	Ground or no connection
4	GND or N/C	Ground or no connection	16	GND or N/C	Ground or no connection
5	SERIAL_OUTPUT	Data output delayed by eight clock cycles	17	RF2	RF input/output. Must be DC blocked.
6	GND or N/C	Ground or no connection	18	GND or N/C	Ground or no connection
7	RESET	Reset. Clears shift registers.	19	GND	Ground
8	CLOCK	Serial clock input	20	GND	Ground
9	LATCH_ENABLE	On rising edge of pulse, shifts five most recent clocked-in bits to set attenuation state	21	GND	Ground
10	GND or N/C	Ground or no connection	22	GND	Ground
11	SERIAL_INPUT	Data input	23	GND	Ground
12	GND or N/C	Ground or no connection	24	GND	Ground

Note: Exposed pad must be grounded.

Functional Description

The SKY12345-362LF is a five bit digital attenuator comprised of a GaAs attenuator and a silicon CMOS driver. The attenuation setting is controlled by a serial-to-parallel interface. Attenuation is set by a stream of data that is clocked into the shift registers of the silicon chip by the clock signal. To set the attenuation state, a latch signal is sent to the appropriate pin to send the correct bias voltages to the GaAs attenuator.

More than one attenuator can be cascaded together and the data may be passed through one device to the other using the SERIAL_OUTPUT signal (pin 5). To reset the attenuator to the insertion loss state, a logic low signal may be sent to the RESET pin. DC bias voltage to the silicon CMOS chip is applied to pin 14 (VCC).

Power-Up/Power-Down Timing

Serial input data (SERIAL_INPUT pin) is shifted into the register on the rising edge of the clock (CLOCK pin), least significant bit (LSB) first. The attenuator changes states on the rising edge of the latch-enable (LATCH_ENABLE pin) signal, according to the most recent five bits of shifted data accepted since the previous falling edge of the latch enable signal. The serial data output is the serial input data delayed by eight clock cycldes.

Refer to the timing diagram in Figure 3 and timing parameter specifications in Table 2. Table 3 shows the transition states based on the latch enable, clock, and reset logic settings.

Power-up sequence is as follows:

0. Connect ground

1. Apply V_{CC}

2. Set all inputs (SCK, SDA, LE)

The power-down sequence is the reverse of above.

Figure 4 shows an example of how to set the attenuator to the 0.5 dB state. The progression of the bit states vs the clock signal is shown. The timing diagram shows that when the latch enable signal goes high, the voltages v1 to v5 set the attenuator to the 0.5 dB state.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY12345-362LF are provided in Table 4. Electrical specifications are provided in Tables 5 and 6.

Typical performance characteristics of the SKY12345-362LF are illustrated in Figures 5 through 11.

The state of the SKY12345-362LF is determined by the logic provided in Table 7.

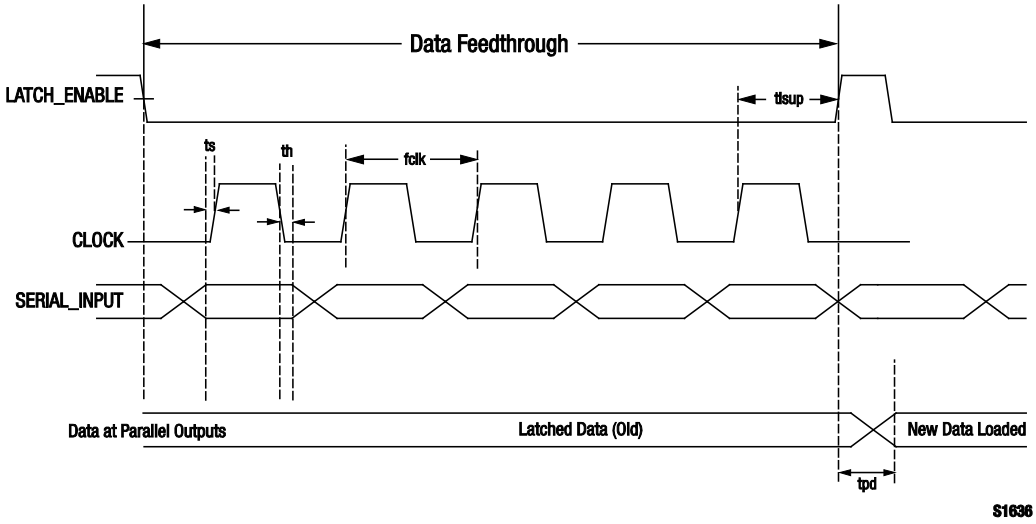


Figure 3. Power-Up/Power-Down Timing

Table 2. Power-Up/Power-Down Timing Parameters

Parameter	Symbol	V_{CC} = 5 V			V_{CC} = 3 V			Units
		Minimum	Typical	Maximum	Minimum	Typical	Maximum	
Serial input setup time	ts		5			5		ns
Hold time from serial input to shift clock	th		5			5		ns
Setup time from shift clock to latch enable	tlsup	40			100			ns
Propagation delay, latch enable to C0.5 through C8	tpd			30			70	ns
Setup time from reset to shift clock	–	20			50			ns
Clock frequency	f_{CLK}			30			10	MHz

Table 3. Transition State Logic

LATCH_ENABLE (Pin 9)	CLOCK (Pin 8)	RESET (Pin 7)	Function
X	X	L	Shift register cleared
X	→	H	Shift register clocked
→	X	H	Contents of shift register transferred to digital attenuator

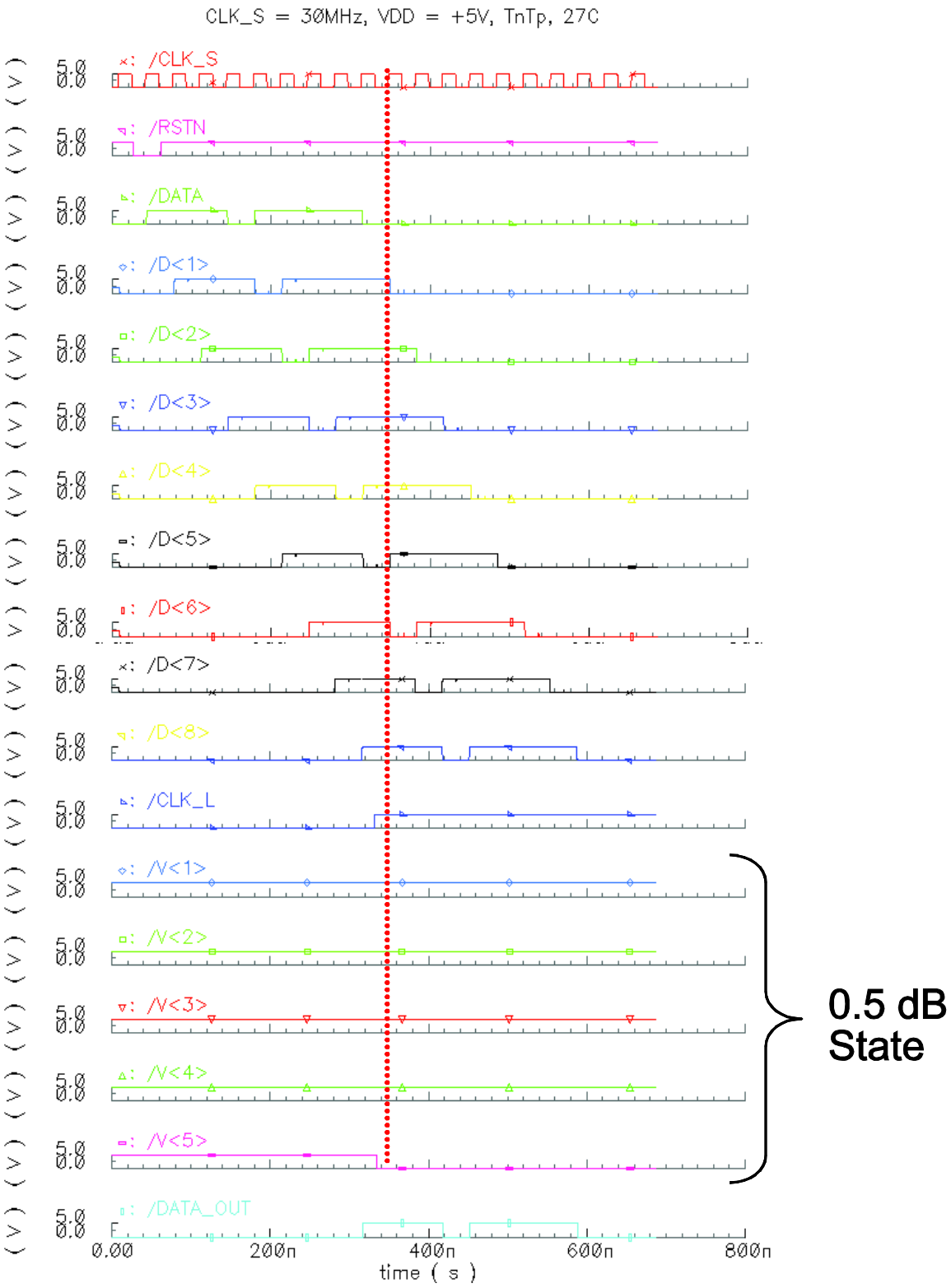


Figure 4. Example for Setting 0.5 dB State

Table 4. SKY12345-362LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
RF input power @ 5 V	P_{IN}			+30	dBm
Supply voltage	V_{CC}			6	V
Control voltage	V_{CTL}	–0.2		+8	V
Operating temperature	T_{OP}	–40		+85	°C
Storage temperature	T_{STG}	–65		+150	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 5. SKY12345-362LF Electrical Specifications (1 of 2) (Note 1)
(V_{CC} = 3 to 5 V, V_{CTL} = 0 to 3 V and 5 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z_0] = 50 Ω, , Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Insertion loss		0.7 to 1.4 GHz 1.4 to 2.3 GHz 2.3 to 2.7 GHz 2.7 to 4.0 GHz		1.2 1.3 1.8 2.0	1.5 2.0 2.3 2.7	dB dB dB dB
Attenuation range				15.5		dB
Attenuation accuracy		Attenuation referred to insertion loss, all attenuation states 0.7 to 0.9 GHz 0.9 to 2.2 GHz 2.2 to 4.0 GHz	±(0.5 + 5% of attenuation setting max) ±(0.3 + 4% of attenuation setting max) ±(0.5 + 5% of attenuation setting max)			 dB dB dB
Return loss		RF1 and RF2 pins, all attenuation states 0.7 to 1.4 GHz 1.4 to 2.3 GHz 2.3 to 2.7 GHz 2.7 to 4.0 GHz	 12 15 12 10	 14 18 15 13		 dB dB dB dB
Switching characteristics: On/rise time Off/fall time		 50% V_{CTL} to 90% RF or 10/90% RF 50% V_{CTL} to 10% RF or 90/10% RF		 1200 500		 ns ns

Table 5. SKY12345-362LF Electrical Specifications (2 of 2) (Note 1)
(V_{CC} = 3 to 5 V, V_{CTL} = 0 to 3 V and 5 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z_0] = 50 Ω, , Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Input power for 0.1 dB compression		0.7 to 3.8 GHz V_{CC} = V_{CTL} = 5 V V_{CC} = V_{CTL} = 3 V		 +25 +23		 dBm dBm
Input power for 1 dB compression		0.7 to 3.8 GHz V_{CC} = V_{CTL} = 5 V V_{CC} = V_{CTL} = 3 V		 +32 +30		 dBm dBm
3rd Order Input Intercept Point	IIP3	0.7 to 3.8 GHz, for two-tone input power. 0 dBm/tone, 1 MHz spacing V_{CC} = V_{CTL} = 5 V V_{CC} = V_{CTL} = 3 V		 +42 +42		 dBm dBm

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 6. DC Electrical Characteristics (Note 1)
(V_{CC} = 3 to 5 V, V_{CTL} = 0 to 3 V and 5 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z_0] = 50 Ω, , Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Input voltage, high	V_{IH}	V_{CC} = 3 V V_{CC} = 5 V	2.3 3.5		3.0 5.0	V V
Input voltage, low	V_{IL}	V_{CC} = 3 V V_{CC} = 5 V	0 0		1.0 1.5	V V
Input leakage current	I_L			0.5		µA
Quiescent current	I_{CC}			500		µA
Supply voltage	V_{CC}		3.0	5.0	5.5	V

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Typical Performance Characteristics

(V_{CC} = 5 V, V_{CTL} = 0 to 5 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, C_{BLK} = 47 pF, Characteristic Impedance [Z_O] = 50 Ω, , Unless Otherwise Noted)

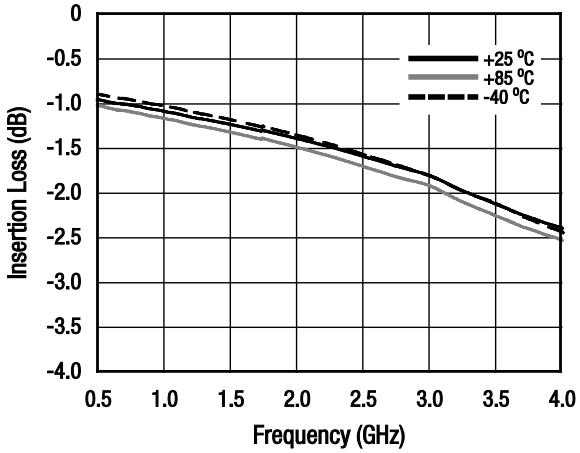


Figure 5. Insertion Loss vs Frequency

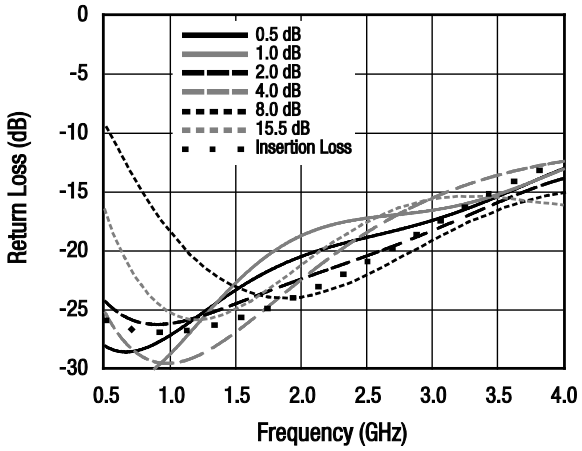


Figure 6. Return Loss: Major States

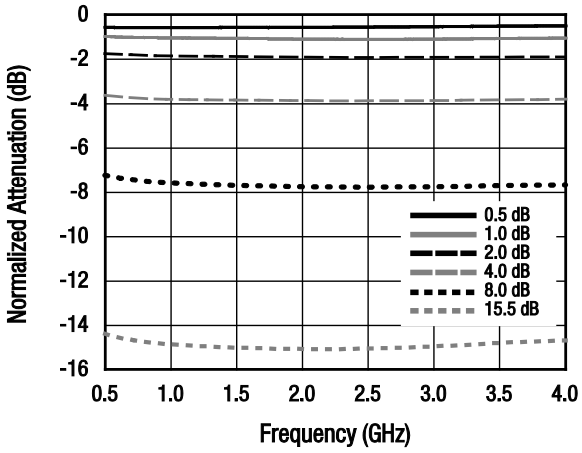


Figure 7. Normalized Attenuation: Major States

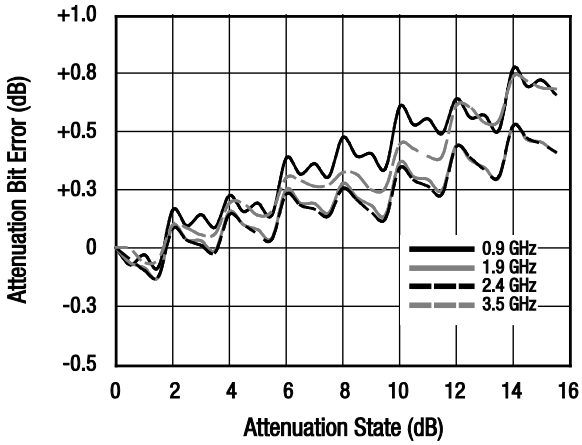


Figure 8. Attenuation Bit Error vs Attenuation State

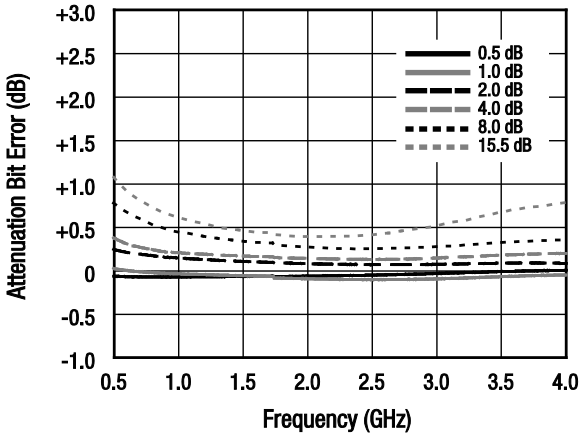


Figure 9. Attenuation Bit Error: Major States

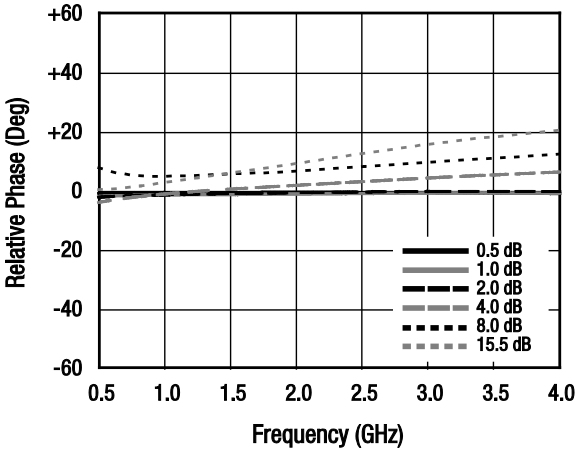


Figure 10. Relative Phase: Major States

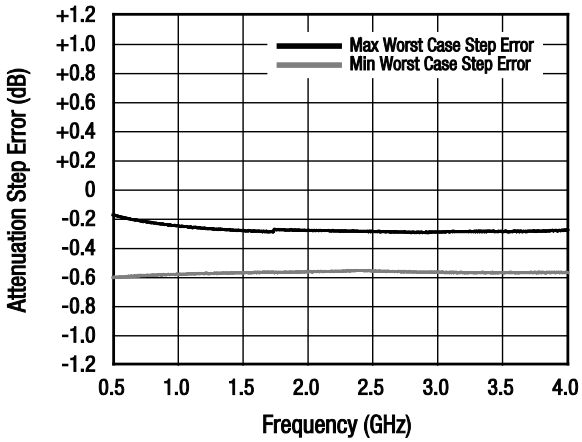


Figure 11. Worst Case Attenuation Step Error Between Successive Attenuation States

Table 7. SKY12345-362LF Truth Table

RF1/RF2 (Pins 2 & 17) Attenuation	RESET (Pin 7)	Serial Data Input				
		0.5 dB	1.0 dB	2.0 dB	4.0 dB	8.0 dB
Insertion loss	1	1	1	1	1	1
0.5 dB	1	0	1	1	1	1
1.0 dB	1	1	0	1	1	1
2.0 dB	1	1	1	0	1	1
4.0 dB	1	1	1	1	0	1
8.0 dB	1	1	1	1	1	0
15.5 dB	1	0	0	0	0	0
Insertion loss	0	X	X	X	X	X

Note: For V_{CC} = 5 V: "1" = V_{IH} = +3.5 V to +5 V. "0" = V_{IL} = 0 to +0.5 V.
For V_{CC} = 3 V: "1" = V_{IH} = +2.3 V to +3 V. "0" = V_{IL} = 0 to +0.5 V.
"X" = don't care. This Table shows the logic required for the major bits and full attenuation. Bit states need to be used in combination to set the sum of the bits selected.

Evaluation Board Description

The SKY12345-362LF Evaluation Board is used to test the performance of the SKY12345-362LF digital attenuator. An assembly drawing for the Evaluation Board is shown in Figure 12 and an Evaluation Board schematic diagram is shown in Figure 13.

Package Dimensions

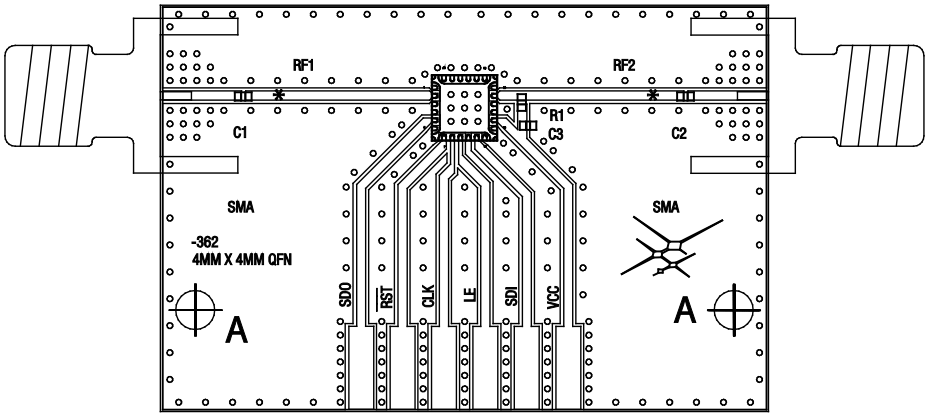
The PCB layout footprint for the SKY12345-362LF is shown in Figure 14. Typical case markings are noted in Figure 15. Package dimensions for the 24-pin QFN are shown in Figure 16, and tape and reel dimensions are provided in Figure 17.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

THE SKY12345-362LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format. For packaging details, refer to the Skyworks Application Note, *Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation*, document number 200083.



C1 = C2 = 47 to 300 pF
C3 = 0.01 µF
R1 = 5 kΩ

Figure 12. SKY12345-362LF Evaluation Board Assembly Diagram

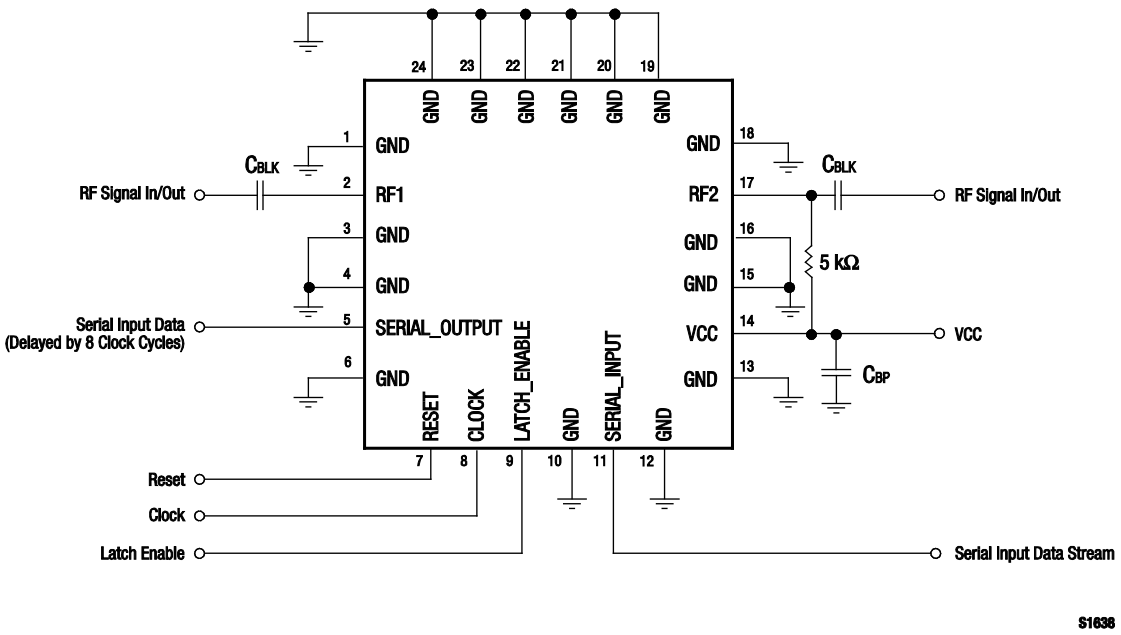


Figure 13. SKY12345-362LF Evaluation Board Schematic Diagram

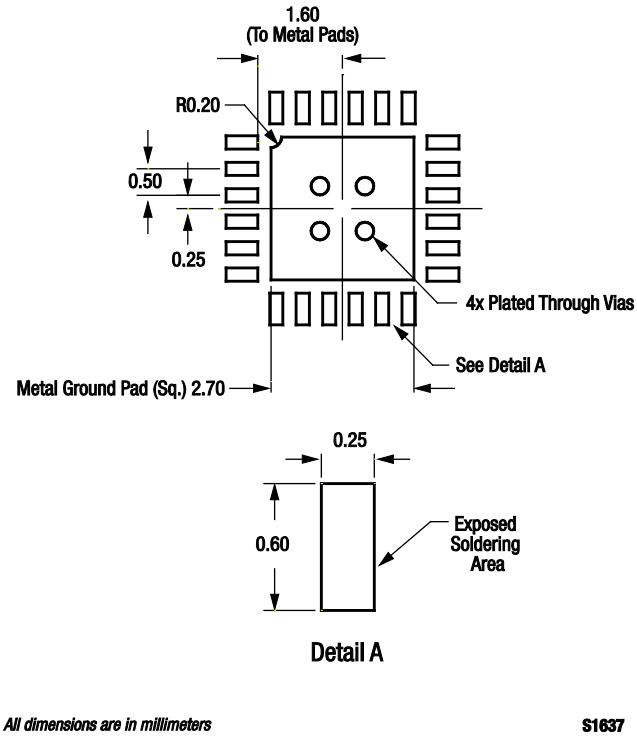


Figure 14. SKY12345-362LF PCB Layout Footprint

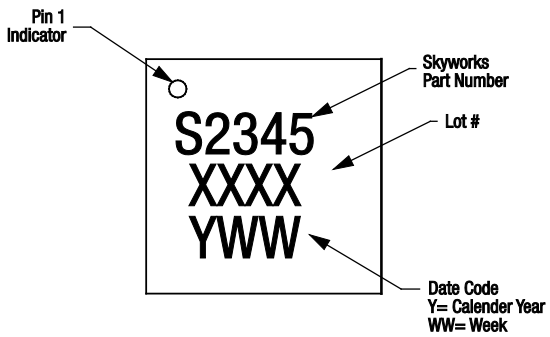


Figure 15. Typical Part Markings

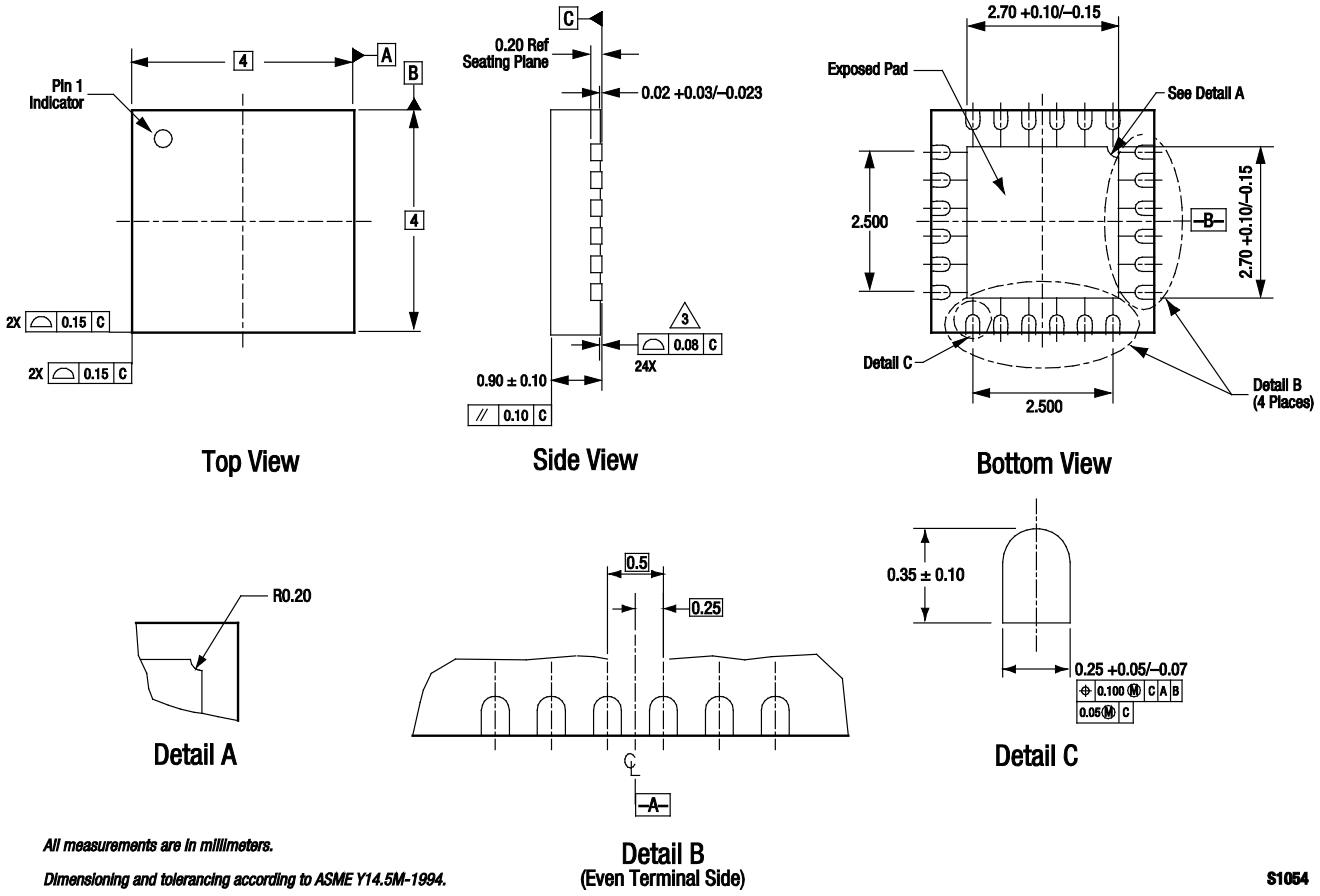
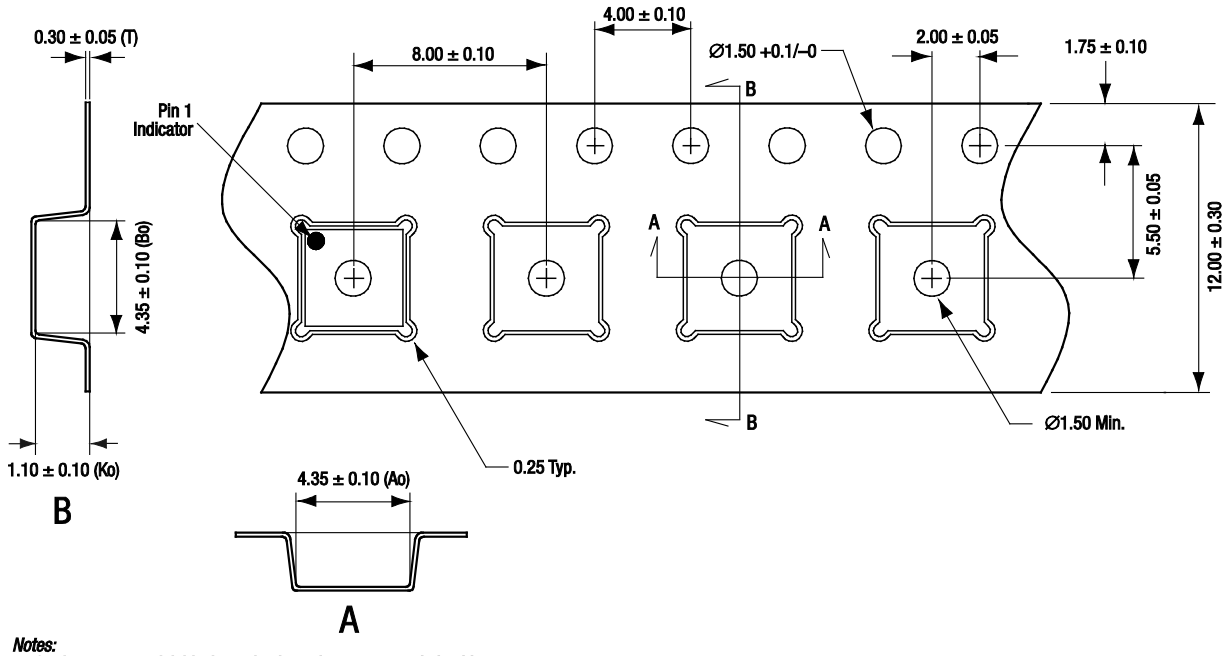


Figure 16. SKY12345-362LF 24-Pin QFN Package Dimensions



Notes:
1. Carrier tape material: black conductive polystyrene, non-bakeable
2. Cover tape material: transparent conductive HSA
3. Cover tape size: 9.2 mm width
4. All measurements are in millimeters

S1846

Figure 17. SKY12345-362LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY12345-362LF Digital Attenuator	SKY12345-362LF	SKY12345-362LF-EVB

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