# MC10E150, MC100E150

# 5V ECL 6-Bit D Latch

## Description

The MC10E/100E150 contains six D-type latches with differential outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent and input data transitions propagate through to the output. A logic HIGH on either LEN1 or LEN2 (or both) latches the data. The Master Reset (MR) overrides all other controls to set the Q outputs low.

The 100 Series contains temperature compensation.

## Features

- 800 ps Max. Propagation Delay
- PECL Mode Operating Range: $V_{CC}$ = 4.2 V to 5.7 V
  with $V_{EE}$ = 0 V
- NECL Mode Operating Range: $V_{CC}$ = 0 V
  with $V_{EE}$ = −4.2 V to −5.7 V
- Internal Input 50 k$\Omega$ Pulldown Resistors
- ESD Protection:  Human Body Model; > 2 kV,
  Machine Model; > 200 V
  Charged Device Model; > 2 kV
- Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level:
  Pb = 1
  Pb−Free = 3
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V−0 @ 0.125 in,
  Oxygen Index: 28 to 34
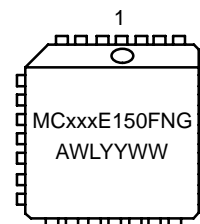- Transistor Count = 173 devices
- Pb−Free Packages are Available*

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http://onsemi.com
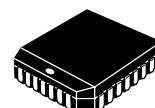
**PLCC−28**
**FN SUFFIX**
**CASE 776**

### MARKING DIAGRAM*

1

MCxxxE150FNG
AWLYYWW

| | |
|---|---|
| xxx | = 10 or 100 |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
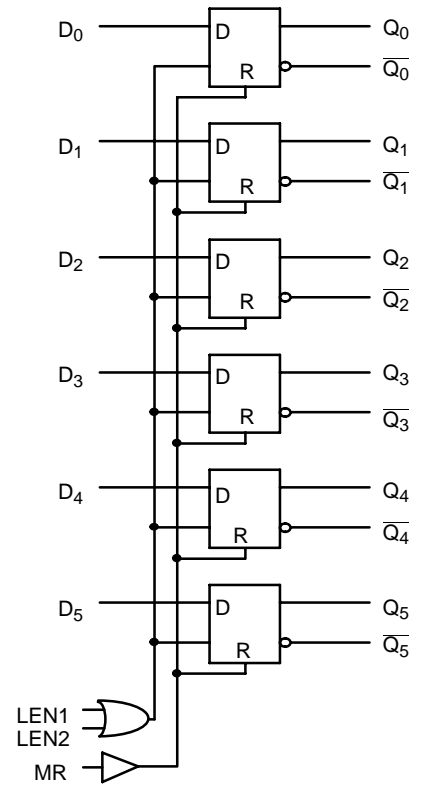
# MC10E150, MC100E150



**Figure 1. 28–Lead Pinout**

Pinout: 28-Lead PLCC
(Top View)
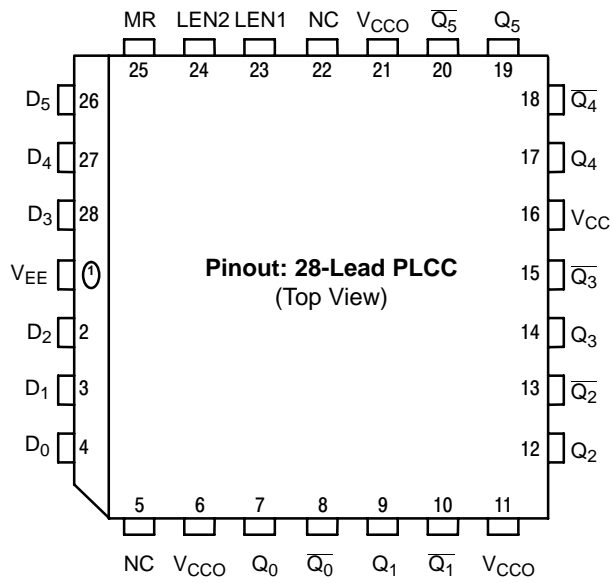
* All $V_{CC}$ and $V_{CCO}$ pins are tied together on the die.

Warning: All $V_{CC}$, $V_{CCO}$, and $V_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation.



**Figure 2. Logic Diagram**

**Table 1. PIN DESCRIPTION**

| PIN | FUNCTION |
| --- | --- |
| $D_0 - D_5$ | ECL Data Inputs |
| LEN1, LEN2 | ECL Latch Enables |
| MR | ECL Master Reset |
| $Q_0 - Q_5$, $\overline{Q_0} - \overline{Q_5}$ | ECL Differential Outputs |
| $V_{CC}$, $V_{CCO}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |
| NC | No Connect |

**Table 2. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|--------|-----------|-------------|-------------|--------|------|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 8 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | −8 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6<br>−6 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $T_A$ | Operating Temperature Range | | | 0 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | PLCC−28<br>PLCC−28 | 63.5<br>43.5 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | Standard Board | PLCC−28 | 22 to 26 | °C/W |
| $V_{EE}$ | PECL Operating Range<br>NECL Operating Range | | | 4.2 to 5.7<br>−5.7 to −4.2 | V<br>V |
| $T_{sol}$ | Wave Solder     Pb<br>               Pb−Free | | | 265<br>265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 3. 10E SERIES PECL DC CHARACTERISTICS** $V_{CC}$ = 5.0 V, $V_{EE}$ = 0.0 V (Note 1)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|--------|----------------|-----|-----|-----|------|-----|-----|------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 52 | 62 | | 52 | 62 | | 52 | 62 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 3980 | 4070 | 4160 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 3050 | 3210 | 3370 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV |
| $V_{IH}$ | Input HIGH Voltage | 3830 | 3995 | 4160 | 3870 | 4030 | 4190 | 3940 | 4110 | 4280 | mV |
| $V_{IL}$ | Input LOW Voltage | 3050 | 3285 | 3520 | 3050 | 3285 | 3520 | 3050 | 3302 | 3555 | mV |
| $I_{IH}$ | Input HIGH Current<br>         D<br>    LEN, MR | | | 200<br>150 | | | 200<br>150 | | | 200<br>150 | μA<br>μA |
| $I_{IL}$ | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.3 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary −0.46 V / +0.06 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.

**Table 4. 10E SERIES NECL DC CHARACTERISTICS** $V_{CCx}$ = 0.0 V; $V_{EE}$ = –5.0 V (Note 3)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 52 | 62 | | 52 | 62 | | 52 | 62 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 4) | –1020 | –930 | –840 | –980 | –895 | –810 | –910 | –815 | –720 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 4) | –1950 | –1790 | –1630 | –1950 | –1790 | –1630 | –1950 | –1773 | –1595 | mV |
| $V_{IH}$ | Input HIGH Voltage | –1170 | –1005 | –840 | –1130 | –970 | –810 | –1060 | –890 | –720 | mV |
| $V_{IL}$ | Input LOW Voltage | –1950 | –1715 | –1480 | –1950 | –1715 | –1480 | –1950 | –1698 | –1445 | mV |
| $I_{IH}$ | Input HIGH Current<br>D<br>LEN, MR | | | 200<br>150 | | | 200<br>150 | | | 200<br>150 | μA<br>μA |
| $I_{IL}$ | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.065 | | 0.3 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary –0.46 V / +0.06 V.
4. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ – 2.0 V.

**Table 5. 100E SERIES PECL DC CHARACTERISTICS** $V_{CC}$ = 5.0 V, $V_{EE}$ = 0.0 V (Note 5)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 52 | 62 | | 52 | 62 | | 60 | 72 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 6) | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 6) | 3190 | 3295 | 3380 | 3190 | 3255 | 3380 | 3190 | 3260 | 3380 | mV |
| $V_{IH}$ | Input HIGH Voltage | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | mV |
| $V_{IL}$ | Input LOW Voltage | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | mV |
| $I_{IH}$ | Input HIGH Current<br>D<br>LEN, MR | | | 200<br>150 | | | 200<br>150 | | | 200<br>150 | μA<br>μA |
| $I_{IL}$ | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary –0.46 V / +0.8 V.
6. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ – 2.0 V.

**Table 6. 100E SERIES NECL DC CHARACTERISTICS** $V_{CCx} = 0.0$ V; $V_{EE} = -5.0$ V (Note 7)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 52 | 62 | | 52 | 62 | | 60 | 72 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 8) | −1025 | −950 | −880 | −1025 | −950 | −880 | −1025 | −950 | −880 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 8) | −1810 | −1705 | −1620 | −1810 | −1745 | −1620 | −1810 | −1740 | −1620 | mV |
| $V_{IH}$ | Input HIGH Voltage | −1165 | −1025 | −880 | −1165 | −1025 | −880 | −1165 | −1025 | −880 | mV |
| $V_{IL}$ | Input LOW Voltage | −1810 | −1645 | −1475 | −1810 | −1645 | −1475 | −1810 | −1645 | −1475 | mV |
| $I_{IH}$ | Input HIGH Current<br>D<br>LEN, MR | | | 200<br>150 | | | 200<br>150 | | | 200<br>150 | μA<br>μA |
| $I_{IL}$ | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary −0.46 V / +0.8 V.
8. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0$ V.

**Table 7. AC CHARACTERISTICS** $V_{CCx} = 5.0$ V; $V_{EE} = 0.0$ V or $V_{CCx} = 0.0$ V; $V_{EE} = -5.0$ V (Note 9)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Toggle Frequency | 900 | 1100 | | 900 | 1100 | | 900 | 1100 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output<br>D<br>LEN<br>MR | 250<br>375<br>450 | 375<br>500<br>625 | 550<br>800<br>750 | 250<br>375<br>450 | 375<br>500<br>625 | 550<br>800<br>750 | 250<br>375<br>450 | 375<br>500<br>625 | 550<br>800<br>750 | ps |
| $t_s$ | Setup Time<br>D | 200 | 50 | | 200 | 50 | | 200 | 50 | | ps |
| $t_h$ | Hold Time<br>D | 200 | −50 | | 200 | −50 | | 200 | −50 | | ps |
| $t_{RR}$ | Reset Recovery Time | 750 | 650 | | 750 | 650 | | 750 | 650 | | ps |
| $t_{PW}$ | Minimum Pulse Width<br>MR | 400 | | | 400 | | | 400 | | | ps |
| $t_{SKEW}$ | Within-Device Skew (Note 10) | | 50 | | | 50 | | | 50 | | ps |
| $t_{JITTER}$ | Random Clock Jitter (RMS) | | < 1 | | | < 1 | | | < 1 | | ps |
| $t_r$<br>$t_f$ | Rise/Fall Time<br>(20 - 80%) | 300 | 450 | 650 | 300 | 450 | 650 | 300 | 450 | 650 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. 10 Series: $V_{EE}$ can vary −0.46 V / +0.06 V.
   100 Series: $V_{EE}$ can vary −0.46 V / +0.8 V.
10. Within-device skew is defined as identical transitions on similar paths through a device.
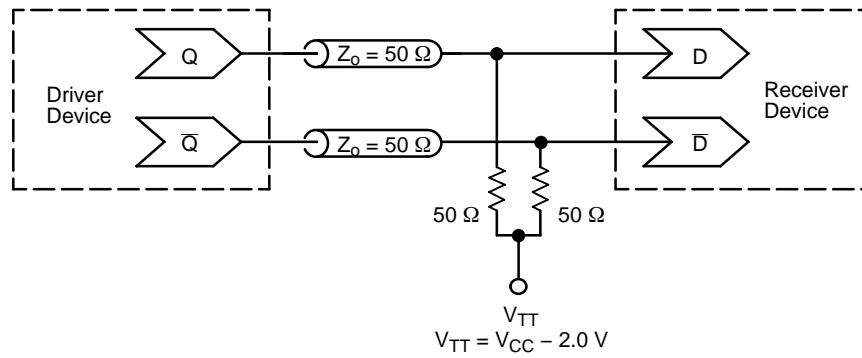
**Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

## ORDERING INFORMATION

| Device | Package | Shipping[†] |
|---|---|---|
| MC10E150FN | PLCC−28 | 37 Units / Rail |
| MC10E150FNG | PLCC−28 (Pb−Free) | 37 Units / Rail |
| MC10E150FNR2 | PLCC−28 | 500 / Tape & Reel |
| MC10E150FNR2G | PLCC−28 (Pb−Free) | 500 / Tape & Reel |
| MC100E150FN | PLCC−28 | 37 Units / Rail |
| MC100E150FNG | PLCC−28 (Pb−Free) | 37 Units / Rail |
| MC100E150FNR2 | PLCC−28 | 500 / Tape & Reel |
| MC100E150FNR2G | PLCC−28 (Pb−Free) | 500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### Resource Reference of Application Notes

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1672/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

**AND8020/D** – Termination of ECL Logic Devices

**AND8066/D** – Interfacing with ECLinPS

**AND8090/D** – AC Characteristics of ECL Devices

## PACKAGE DIMENSIONS

**PLCC–28**
**FN SUFFIX**
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE E



**VIEW D–D**



**VIEW S**
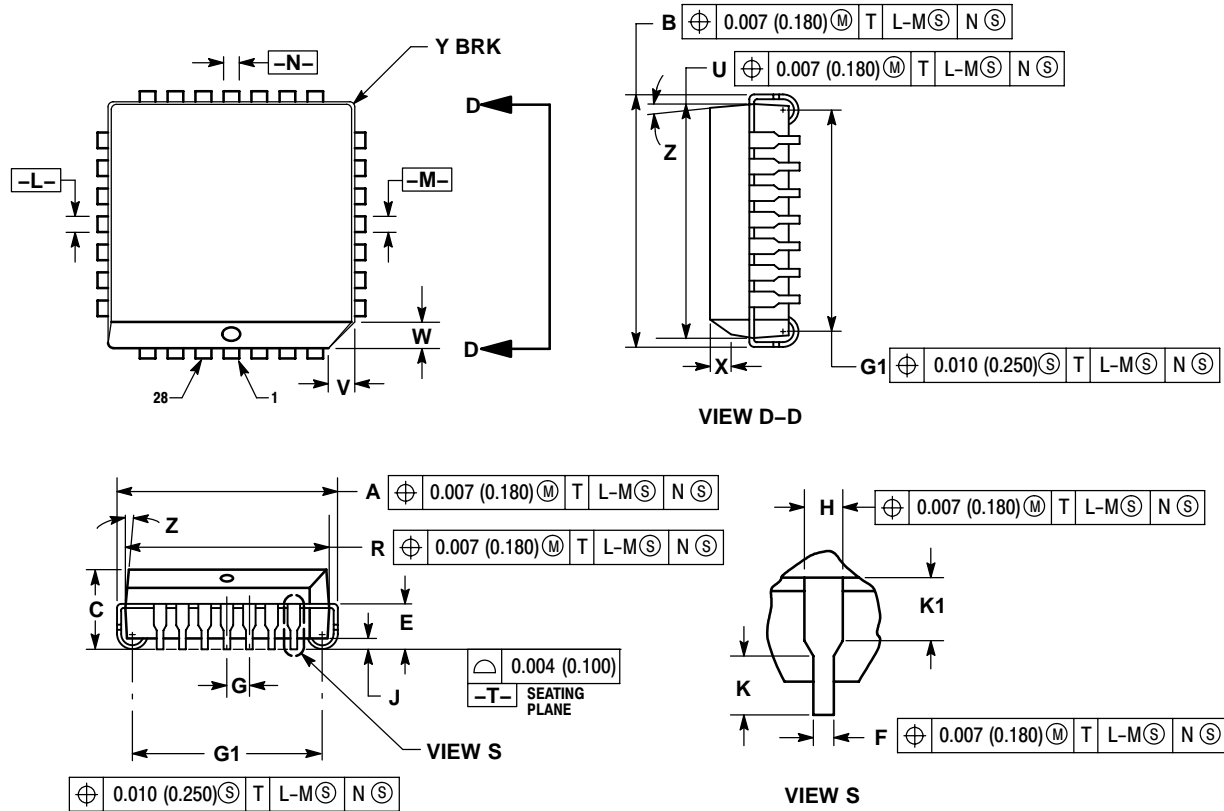
NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|--------|--------|--------|
| | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | --- | 0.51 | --- |
| K | 0.025 | --- | 0.64 | --- |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | --- | 0.020 | --- | 0.50 |
| Z | 2 ° | 10° | 2 ° | 10° |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | --- | 1.02 | --- |

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