

# MC14504B

## Hex Level Shifter for TTL to CMOS or CMOS to CMOS

The MC14504B is a hex non-inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level: Either up or down level translating is accomplished by selection of power supply levels  $V_{DD}$  and  $V_{CC}$ . The  $V_{CC}$  level sets the input signal levels while  $V_{DD}$  selects the output voltage levels.

### Features

- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for  $V_{DD}$  and  $V_{CC}$
- Diode Protected Inputs to  $V_{SS}$
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}$	Input Voltage Range (DC or Transient)	-0.5 to +18.0	V
$V_{out}$	Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

#### 1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

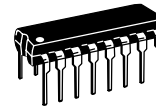
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



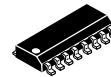
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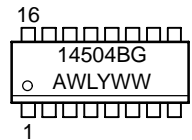
### MARKING DIAGRAMS



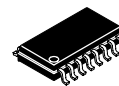
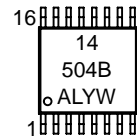
PDIP-16  
P SUFFIX  
CASE 648



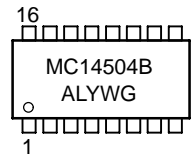
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G = Pb-Free Indicator

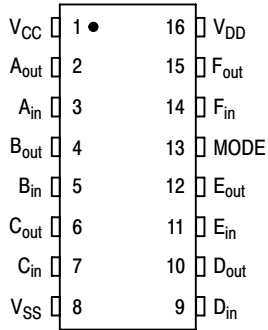
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

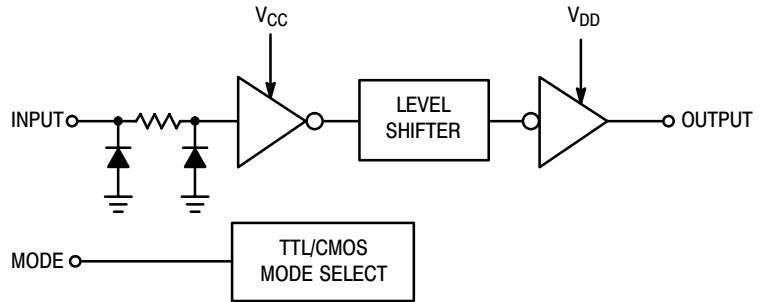
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## PIN ASSIGNMENT



## LOGIC DIAGRAM



Mode Select	Input Logic Levels	Output Logic Levels
1 (V <sub>CC</sub> )	TTL	CMOS
0 (V <sub>SS</sub> )	CMOS	CMOS

1/6 of package shown.

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC14504BCP	PDIP-16	500 Units / Rail
MC14504BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14504BD	SOIC-16	48 Units / Rail
MC14504BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14504BDR2	SOIC-16	2500 Units / Tape & Reel
MC14504BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14504BDT	TSSOP-16*	96 Units / Rail
MC14504BDTR2	TSSOP-16*	2500 Units / Tape & Reel
MC14504BF	SOEIAJ-16	50 Units / Rail
MC14504BFEL	SOEIAJ-16	2000 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{CC}$ Vdc	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage $V_{in} = 0\text{ V}$  $V_{in} = V_{CC}$	"0" Level  $V_{OL}$	-	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
		-	10	-	0.05	-	0	0.05	-	0.05	
		-	15	-	0.05	-	0	0.05	-	0.05	
	"1" Level  $V_{OH}$	-	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		-	10	9.95	-	9.95	10	-	9.95	-	
		-	15	14.95	-	14.95	15	-	14.95	-	
Input Voltage ( $V_{OL} = 1.0\text{ Vdc}$ ) TTL-CMOS ( $V_{OL} = 1.5\text{ Vdc}$ ) TTL-CMOS ( $V_{OL} = 1.0\text{ Vdc}$ ) CMOS-CMOS ( $V_{OL} = 1.5\text{ Vdc}$ ) CMOS-CMOS ( $V_{OL} = 1.5\text{ Vdc}$ ) CMOS-CMOS	"0" Level  $V_{IL}$	5.0	10	-	0.8	-	1.3	0.8	-	0.8	Vdc
		5.0	15	-	0.8	-	1.3	0.8	-	0.8	
		5.0	10	-	1.5	-	2.25	1.5	-	1.4	
		5.0	15	-	1.5	-	2.25	1.5	-	1.5	
		10	15	-	3.0	-	4.5	3.0	-	2.9	
		10	15	-	3.0	-	4.5	3.0	-	2.9	
Input Voltage ( $V_{OH} = 9.0\text{ Vdc}$ ) TTL-CMOS ( $V_{OH} = 13.5\text{ Vdc}$ ) TTL-CMOS ( $V_{OH} = 9.0\text{ Vdc}$ ) CMOS-CMOS ( $V_{OH} = 13.5\text{ Vdc}$ ) CMOS-CMOS ( $V_{OH} = 13.5\text{ Vdc}$ ) CMOS-CMOS	"1" Level  $V_{IH}$	5.0	10	2.0	-	2.0	1.5	-	2.0	-	Vdc
		5.0	15	2.0	-	2.0	1.5	-	2.0	-	
		5.0	10	3.6	-	3.5	2.75	-	3.5	-	
		5.0	15	3.6	-	3.5	2.75	-	3.5	-	
		10	15	7.1	-	7.0	5.5	-	7.0	-	
		10	15	7.1	-	7.0	5.5	-	7.0	-	
Output Drive Current ( $V_{OH} = 2.5\text{ Vdc}$ ) ( $V_{OH} = 4.6\text{ Vdc}$ ) ( $V_{OH} = 9.5\text{ Vdc}$ ) ( $V_{OH} = 13.5\text{ Vdc}$ )  ( $V_{OL} = 0.4\text{ Vdc}$ ) ( $V_{OL} = 0.5\text{ Vdc}$ ) ( $V_{OL} = 1.5\text{ Vdc}$ )	Source  $I_{OH}$	-	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc
		-	5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
		-	10	-1.6	-	-1.3	-2.25	-	-0.9	-	
		-	15	-4.2	-	-3.4	-8.8	-	-2.4	-	
	Sink  $I_{OL}$	-	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
		-	10	1.6	-	1.3	2.25	-	0.9	-	
-		15	4.2	-	3.4	8.8	-	2.4	-		
Input Current	$I_{in}$	-	15	-	$\pm 0.1$	-	$\pm 0.00001$	$\pm 0.1$	-	$\pm 1.0$	$\mu\text{Adc}$
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	-	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package) CMOS-CMOS Mode	$I_{DD}$ or $I_{CC}$	-	5.0	-	0.05	-	0.0005	0.05	-	1.5	$\mu\text{Adc}$
		-	10	-	0.10	-	0.0010	0.10	-	3.0	
		-	15	-	0.20	-	0.0015	0.20	-	6.0	
Quiescent Current (Per Package) TTL-CMOS Mode	$I_{DD}$	5.0	5.0	-	0.5	-	0.0005	0.5	-	3.8	$\mu\text{Adc}$
		5.0	10	-	1.0	-	0.0010	1.0	-	7.5	
		5.0	15	-	2.0	-	0.0015	2.0	-	15	
Quiescent Current (Per Package) TTL-CMOS Mode	$I_{CC}$	5.0	5.0	-	5.0	-	2.5	5.0	-	6.0	mAdc
		5.0	10	-	5.0	-	2.5	5.0	-	6.0	
		5.0	15	-	5.0	-	2.5	5.0	-	6.0	

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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## SWITCHING CHARACTERISTICS (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	Shifting Mode	V <sub>CC</sub> Vdc	V <sub>DD</sub> Vdc	Limits			Unit
					Min	Typ (Note 3)	Max	
Propagation Delay, High to Low	t <sub>PHL</sub>	TTL – CMOS V <sub>DD</sub> > V <sub>CC</sub>	5.0	10	–	140	280	ns
			5.0	15	–	140	280	
		CMOS – CMOS V <sub>DD</sub> > V <sub>CC</sub>	5.0	10	–	120	240	
			5.0	15	–	120	240	
			10	15	–	70	140	
		CMOS – CMOS V <sub>CC</sub> > V <sub>DD</sub>	10	5.0	–	185	370	
15	5.0		–	185	370			
15	10		–	175	350			
Propagation Delay, Low to High	t <sub>PLH</sub>	TTL – CMOS V <sub>DD</sub> > V <sub>CC</sub>	5.0	10	–	170	340	ns
			5.0	15	–	160	320	
		CMOS – CMOS V <sub>DD</sub> > V <sub>CC</sub>	5.0	10	–	170	340	
			5.0	15	–	170	340	
			10	15	–	100	200	
		CMOS – CMOS V <sub>CC</sub> > V <sub>DD</sub>	10	5.0	–	275	550	
15	5.0		–	275	550			
15	10		–	145	290			
Output Rise and Fall Time	t <sub>TLH</sub> , t <sub>THL</sub>	ALL	–	5.0	–	100	200	ns
			–	10	–	50	100	
			–	15	–	40	80	

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

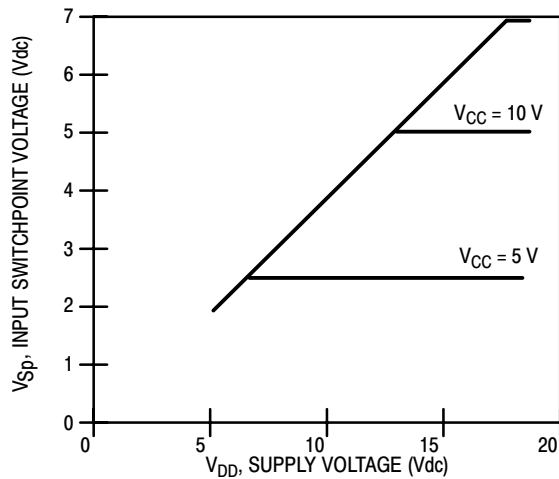


Figure 1. Input Switchpoint CMOS to CMOS Mode

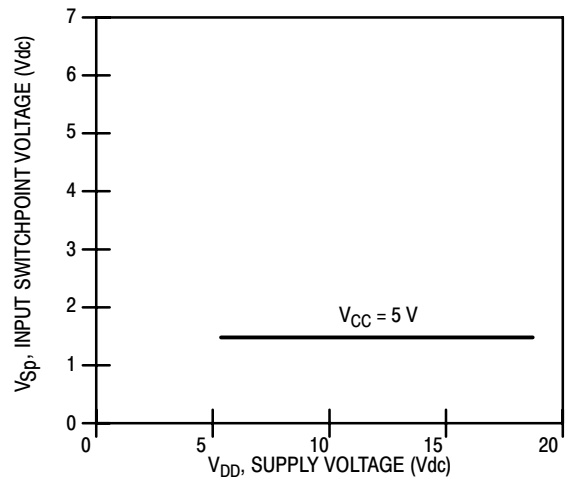


Figure 2. Input Switchpoint TTL to CMOS Mode

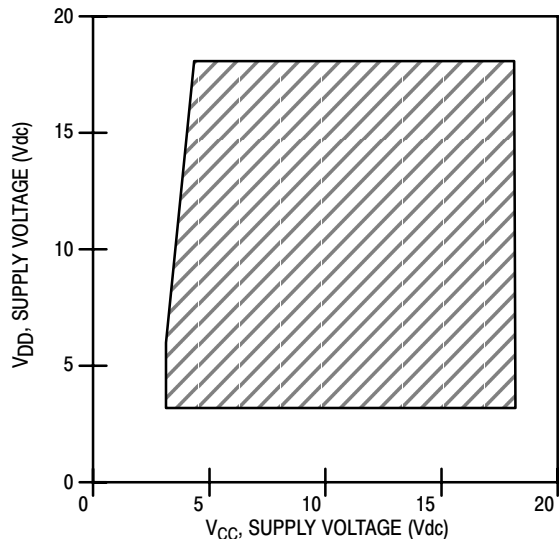


Figure 3. Operating Boundary CMOS to CMOS Mode

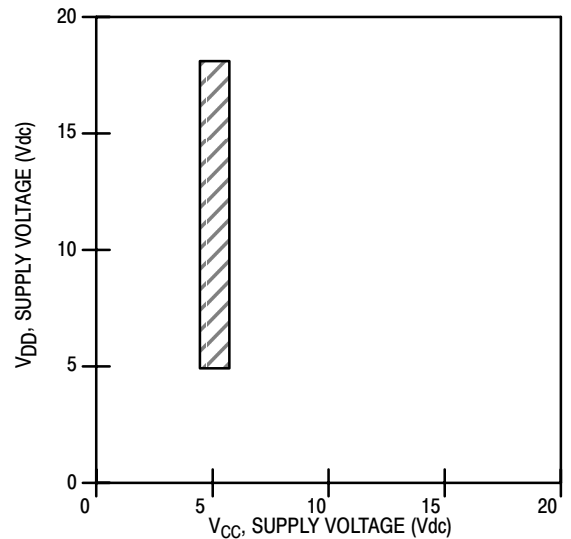
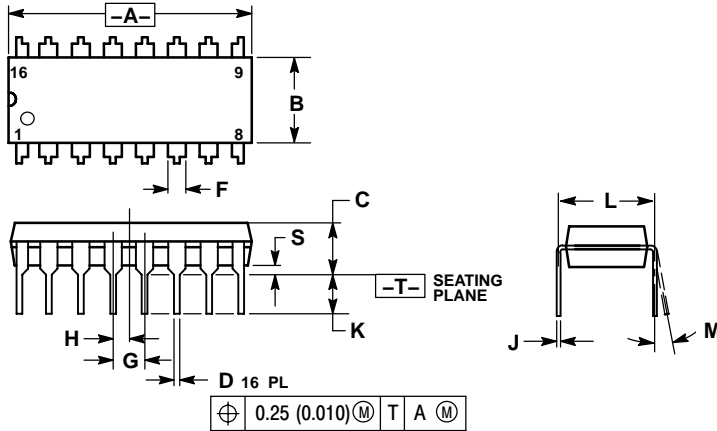


Figure 4. Operating Boundary TTL to CMOS Mode

# MC14504B

## PACKAGE DIMENSIONS

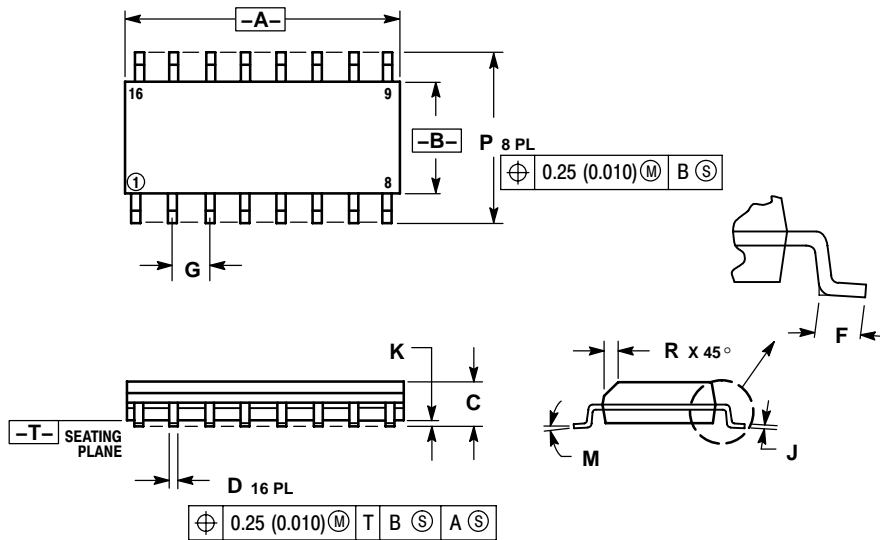
PDIP-16  
P SUFFIX  
PLASTIC DIP PACKAGE  
CASE 648-08  
ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751B-05  
ISSUE J



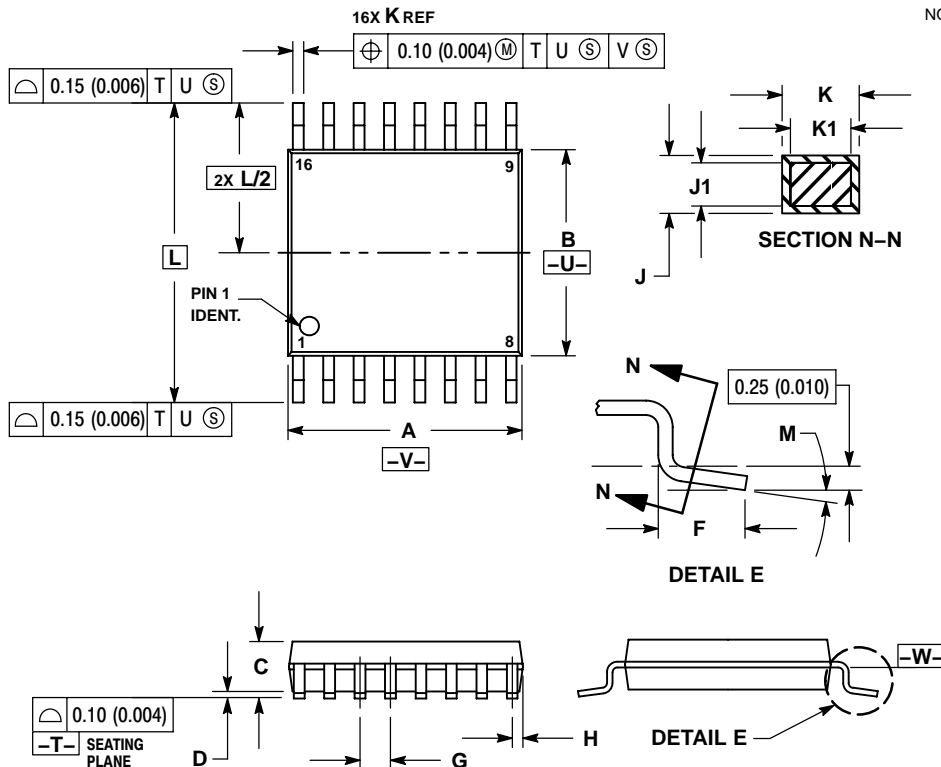
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

# MC14504B

## PACKAGE DIMENSIONS

TSSOP-16  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948F-01  
ISSUE A



### NOTES:

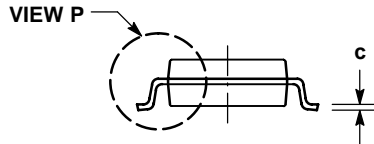
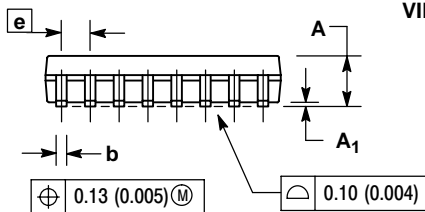
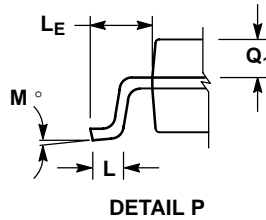
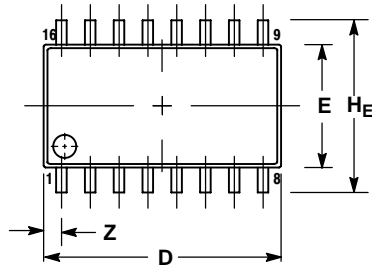
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

# MC14504B

## PACKAGE DIMENSIONS

SOEIAJ-16  
F SUFFIX  
PLASTIC EIAJ SOIC PACKAGE  
CASE 966-01  
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

# MC14504B

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