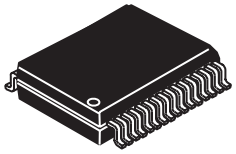
System Basis Chip with LIN Transceiver

33689
33689D

SYSTEM BASIS CHIP WITH LIN



DWB SUFFIX
98ARH99137A
32-TERMINAL SOICW

The 33689 is a SPI-controlled System Basis Chip (SBC) that combines many frequently used functions in an MCU-based system plus a Local Interconnect Network (LIN) transceiver. Applications include power window, mirror, and seat controls. The 33689 has a 5.0 V, 50 mA low dropout regulator with full protection and reporting features. The device provide full SPI-readable diagnostics and a selectable timing watchdog for detecting errant operation.

The LIN transceiver waveshaping circuitry can be disabled for higher data rates. One 50 mA and two 150 mA high-side switches with output protection are available to drive inductive or resistive loads. The 150 mA switches can be pulse-width modulated (PWM).

Two high-voltage inputs are available for contact monitoring or as external wake-up inputs. A current sense operational amplifier is available for load current monitoring.

The 33689 has three operational modes:

- Normal (all functions available)
- Sleep (VDD OFF, wake-up via LIN bus or wake-up inputs)
- Stop (VDD ON, wake-up via MCU, LIN bus, or wake-up inputs)

Features

- Full-Duplex SPI Interface at Frequencies up to 4.0 MHz
- LIN Transceiver Capable to 100 kbps with Waveshaping Capability
- 5.0 V Low Dropout Regulator Full Fault Detection and Protection
- One 50 mA and Two 150 mA Protected High-Side Switches
- Current Sense Operational Amplifier
- The 33689 is compatible with LIN 2.0 Specification Package.

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33689DDWB/R2	-40°C to 125°C	32 SOICW
MC33689DWB/R2		

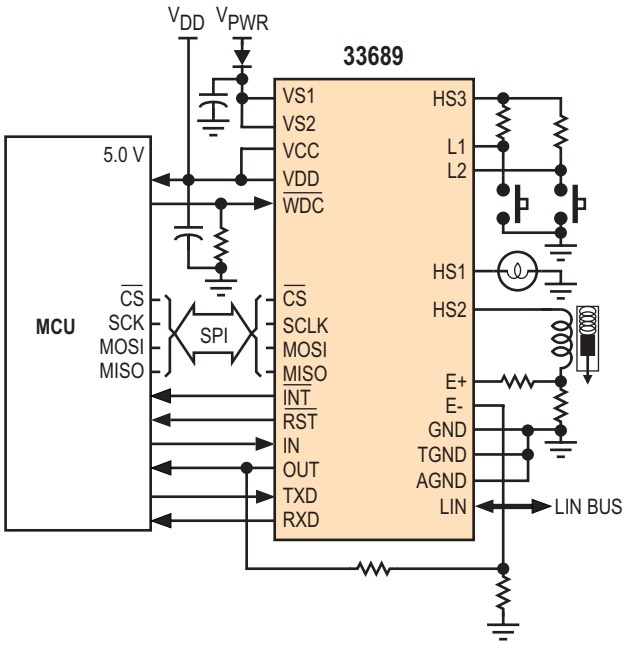


Figure 1. 33689 Simplified Application Diagram

*This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

DEVICE VARIATIONS

Table 1. Device Variations Between the 33689 and the 33689D Versions[1]

Freescale Part No.	Revision	Device Variations	See Page
33689D[2]	4.0	Improved electromagnetic capabilities (EMC). Please refer to separate Application Note for details.	1–29
33689[2]	2.7	N/A	30–47

Notes

1. This datasheet uses the term 33689 in the inclusive sense, referring to both the non-D version (33689) and the D version (33689D).
2. The 33689 and the 33689D datasheets are under separate revision control.

INTERNAL BLOCK DIAGRAM

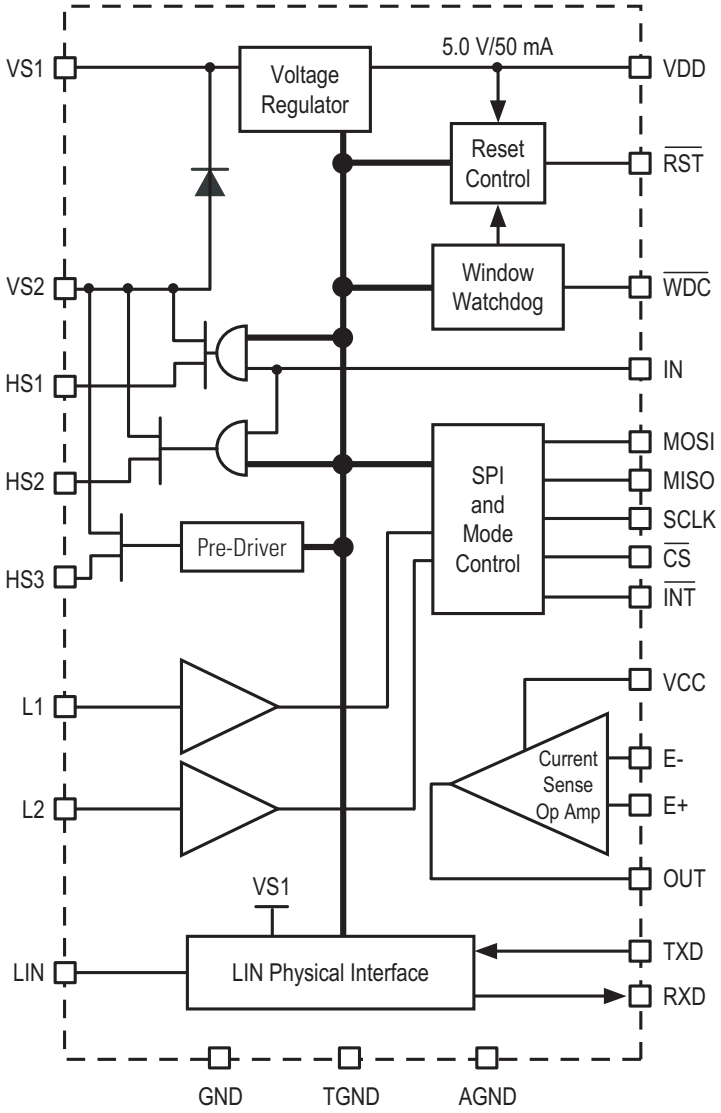


Figure 2. 33689 Simplified Internal Block Diagram

TERMINAL CONNECTIONS

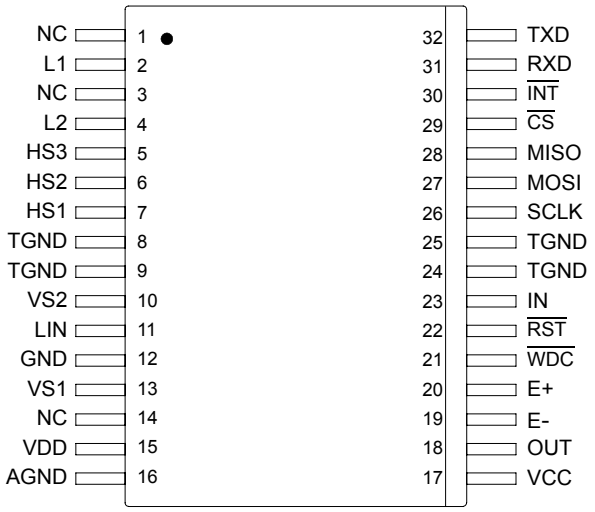


Figure 3. 33689D 32-SOICW Terminal Connections

Table 2. 33689D 32-SOICW Terminal Definitions

A functional description of each terminal can be found in the FUNCTIONAL TERMINAL DESCRIPTION section beginning on page 20.

Terminal	Terminal Name	Formal Name	Terminal Function	Definition
1, 3, 14	NC	No Connect	N/A	No internal connection to these terminals.
2, 4	L1, L2	Level Inputs 1 and 2	Input	Inputs from external switches or from logic circuitry.
5–7	HS3–HS1	High-Side Driver Outputs 3 through 1	Output	High-side (HS) drive power outputs. SPI-controlled for driving system loads.
8, 9, 24, 25	TGND	Thermal Ground	N/A	Thermal ground terminals for the device.
10	VS2	Voltage Supply 2	Input	Supply terminal for the high-side switches HS1, HS2, and HS3.
11	LIN	LIN Bus	Input/Output	Bidirectional terminal that represents the single-wire bus transmitter and receiver.
12	GND	Ground	N/A	Electrical ground terminal for the device.
13	VS1	Voltage Supply 1	Input	Supply terminal for the 5.0 V regulator, the LIN physical interface, and the internal logic.
15	VDD	5.0 V Regulator Output	Output	Output of the 5.0 V regulator.
16	AGND	Analog Ground	N/A	Analog ground terminal for voltage regulator and current sense operational amplifier.
17	VCC	Power Supply In	Input	5.0 V supply for the internal current sense operational amplifier.
18	OUT	Amplifier Output	Output	Output of the internal current sense operational amplifier.
19	E-	Amplifier Inverted Input	Input	Inverted input of the internal current sense operational amplifier.
20	E+	Amplifier Non-Inverted Input	Input	Non-inverted input of the internal current sense operational amplifier.
21	$\overline{\text{WDC}}$	Watchdog Configuration (Active Low)	Reference	Configuration terminal for the watchdog timer.

Table 2. 33689D 32-SOICW Terminal Definitions (continued)

A functional description of each terminal can be found in the FUNCTIONAL TERMINAL DESCRIPTION section beginning on page 20.

Terminal	Terminal Name	Formal Name	Terminal Function	Definition
22	$\overline{\text{RST}}$	Reset Output (Active LOW)	Output	5.0 V regulator and watchdog reset output terminal.
23	IN	PWM Input Control	Input	External input PWM control terminal for high-side switches HS1 and HS2.
26	SCLK	Serial Data Clock	Input	Clock input for the SPI of the 33689.
27	MOSI	Master Out Slave In	Input	SPI data received by the 33689.
28	MISO	Master In Slave Out	Output	SPI data sent to the MCU by the 33689. When $\overline{\text{CS}}$ is HIGH, terminal is in the high-impedance state.
29	$\overline{\text{CS}}$	Chip Select (Active LOW)	Input	SPI control chip select input terminal.
30	$\overline{\text{INT}}$	Interrupt Output (Active LOW)	Output	This output terminal reports faults to the MCU when an enabled interrupt condition occurs.
31	RXD	Receiver Output	Output	Receiver output of the LIN interface and reports the state of the bus voltage.
32	TXD	Transmitter Input	Input	Transmitter input of the LIN interface and controls the state of the bus output.

MAXIMUM RATINGS

Table 3. Maximum Ratings for 33689D

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
Electrical Ratings			
V_{PWR} Supply Voltage at VS1 and VS2			V
Continuous	V_{SUPDC}	-0.3 to 27	
Transient (Load Dump)	V_{SUPTR}	40	
Supply Voltage at VDD and VCC	V_{DD}	-0.3 to 5.5	V
Output Current at VDD	I_{DD}	Internally Limited	A
Logic Input Voltage at MOSI, SCLK, $\overline{CS}$, IN, and TXD	V_{INLOG}	-0.3 to V_{DD}+0.3	V
Logic Output Voltage at MISO, $\overline{INT}$, $\overline{RST}$, and RXD	V_{OUTLOG}	-0.3 to V_{DD}+0.3	V
Input Voltage at E+ and E-	V_{E+}/V_{E-}	-0.3 to 7.0	V
Input Current at E+ and E-	I_{E+}/I_{E-}	±20	mA
Output Voltage at OUT	V_{OUT}	-0.3 to V_{CC}+0.33	V
Output Current at OUT	I_{OUT}	±20	mA
Input Voltage at L1 and L2			V
DC Input with a 33 kΩ Resistor	V_{LXDC}	-18 to 40	
Transient Input with External Component (per ISO7637 Specification) (See Figure 4, page 7)	V_{LXTR}	±100	
Input/Output Voltage at LIN			V
DC Voltage	V_{BUSDC}	-18 to 40	
Transient Input Voltage with specified External Component (per ISO7637 Specification) (See Figure 4, page 7)	V_{BUSTR}	-150 to 100	
DC Output Voltage at HS1 and HS2			V
Positive	V_{HS+}	V_{VS2} + 0.3	
Negative	V_{HS-}	Internally Clamped	
DC Output Voltage at HS3	V_{HS3}	-0.3 to V_{VS2} + 0.3	V
ESD Voltage, Human Body Model [1]	V_{ESD1}		V
GND Configured as Ground. TGND and AGND Configured as I/O Terminals (33689D)			
LIN, L1, and L2		±4000	
All Other Terminals		±2000	
ESD Voltage, Charge Device Model (33689D only) [2]	V_{ESD2}		V
Corner Terminals (Terminals 1, 16, 17, and 32)		±750	
All other Terminals (Terminals 2–15 and 18–31)		±500	

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
2. ESD2 testing is performed in accordance with the Charge Device Model, Robotic (C_{ZAP} = 4.0 pF).

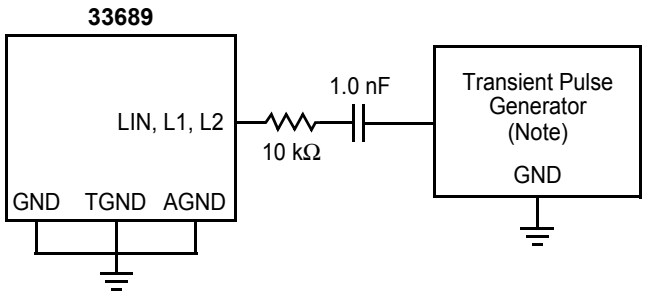
Table 3. Maximum Ratings for 33689D (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
Thermal Ratings			
Operating Temperature			°C
Ambient	T_A	-40 to 125	
Junction	T_J	-40 to 150	
Storage Temperature	T_{STG}	-55 to 165	°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	80	°C/W
Peak Package Reflow Temperature During Solder Mounting (3)	T_{SOLDER}	240	°C

Notes

3. Terminal soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause permanent damage to the device.



Note Waveform per ISO 7637-1. Test Pulses 1, 2, 3a, and 3b.

Figure 4. ISO 7637 Test Setup for LIN, L1, and L2 Terminals

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics for 33689D

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VS1 and VS2 Input Terminals (Device Power Supply)					
Supply Input Voltage					V
Nominal DC	V_{SUP}	5.5	—	18	
Load Dump	V_{SUPLD}	—	—	40	
Jump Start (4)	V_{SUPJS}	—	—	27	
Supply Input Current (5)					
Normal Mode, I_{OUT} at VDD = 10 mA, LIN Recessive State	$I_{SUP(NORM)}$	—	5.0	8.0	mA
Sleep Mode, VDD OFF, V_{SUP} ≤ 13.5 V	I_{SLEEP}	—	35	45	µA
Stop Mode, VDD ON with I_{OUT} < 100 µA, V_{SUP} ≤ 13.5 V	I_{STOP}	—	60	75	µA
Input Threshold Voltage (Normal Mode, Interrupt Generated)					V
Fall Early Warning, Bit VSUV Set	V_{SUVEW}	5.7	6.1	6.6	
Overvoltage Warning, Bit VSOV Set	V_{SOVW}	18	19.75	20.5	
Hysteresis (6)	V_{HYS}				
VSUV Flag		—	1.0	—	V
VSOV Flag		—	220	—	mV
VDD Output Terminal (External 5.0 V Output for MCU Use) (7)					
Output Voltage	V_{DDOUT}				V
I_{DD} from 2.0 mA to 50 mA, 5.5 V < V_{SUP} < 27 V		4.75	5.0	5.25	
Dropout Voltage (8)	V_{DDDROP}				V
I_{DD} = 50 mA		—	0.1	0.2	
Output Current Limitation (9)	I_{DD}	50	120	200	mA
Overtemperature Pre-warning (Junction)	T_{PRE}				°C
Normal Mode, Interrupt Generated, Bit VDDT Set		120	135	160	
Thermal Shutdown (Junction)	T_{SD}				°C
Normal Mode		165	170	—	

Notes

4. Device is fully functional. All features are operating. An overtemperature fault may occur.
5. Total current (I_{VS1} + I_{VS2}) at VS1 and VS2 terminals is measured at the ground terminals.
6. Parameter guaranteed by design; however, it is not production tested.
7. Specification with external capacitor 2.0 µF < C < 10 µF and 200 mΩ ≤ ESR ≤ 10 Ω. Normal mode. Low ESR electrolytic capacitor values up to 47 µF can be used.
8. Measured when the voltage has dropped 100 mV below its nominal value.
9. Internally limited. Total 5.0 V regulator current. A 5.0 mA current for the Current Sense Operational Amplifier operation is included. Digital outputs are supplied from VDD.

Table 4. Static Electrical Characteristics for 33689D (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VDD Output Terminal (5.0 V Output for MCU Use) (continued) (10)					
Temperature Threshold Difference Normal Mode (T_{SD} - T_{PRE})	T_{DIFF}	20	30	40	°C
V_{SUP} Range for Reset Active 0.5 V < V_{DD} < V_{DD} ($V_{\overline{RST}TH}$)	V_{SUPR}	4.0	—	—	V
Line Regulation 5.5 V < V_{SUP} < 27 V, I_{DD} = 10 mA	V_{LR1}	—	20	150	mV
Load Regulation 1.0 mA < I_{DD} < 50 mA	V_{LD1}	—	10	150	mV
VDD Output Terminal in Stop Mode					
Output Voltage (11) I_{DD} ≤ 2.0 mA	V_{DDS}	4.75	5.0	5.25	V
Output Current Capability (12)	I_{DDS}	4.0	8.0	14	mA
Line Regulation 5.5 V < V_{SUP} < 27 V, I_{DD} = 2.0 mA	V_{LRS}	—	10	100	mV
Load Regulation 1.0 mA < I_{DD} < 5.0 mA	V_{LDS}	—	40	150	mV
$\overline{RST}$ Output Terminal in Normal and Stop Modes					
Reset Threshold Voltage	$V_{\overline{RST}TH}$	4.5	4.7	V_{DD}-0.2	V
Low-Level Output Voltage I_O = 1.5 mA, 4.5 V < V_{SUP} < 27 V	V_{OL}	0.0	—	0.9	V
High-Level Output Current 0.0 V < V_{OUT} < 0.7 V_{DD}	I_{OH}	—	-275	—	µA
Reset Pulldown Current Internally Limited, V_{DD} < 4.0 V, $V_{\overline{RST}}$ = 4.6 V	$I_{PD\overline{RST}}$	1.5	—	8.0	mA
IN Input Terminal					
Low-Level Input Voltage	V_{IL}	-0.3	—	0.3 V_{DD}	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD}	—	V_{DD} +0.3	V
Input Current 0.0 V < V_{IN} < V_{DD}	I_{IN}	-10	—	10	µA

Notes

10. Specification with external capacitor 2.0 µF < C < 10 µF and 200 mΩ ≤ ESR ≤ 10 Ω. Normal mode. Low ESR electrolytic capacitor values up to 47 µF can be used.
11. When switching from Normal mode to Stop mode or from Stop mode to Normal mode, the voltage can vary within the output voltage specification.
12. When I_{DD} is above I_{DDS}, the 33689 enters the Reset mode.

Table 4. Static Electrical Characteristics for 33689D (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
MISO SPI Output Terminal					
Low-Level Output Voltage I_{OUT} = 1.5 mA	V_{OL}	0.0	—	1.0	V
High-Level Output Voltage I_{OUT} = 250 µA	V_{OH}	V_{DD} - 0.9	—	V_{DD}	V
Tri-Stated MISO Output Leakage Current 0.0 V < V_{MISO} < V_{DD}	I_{HZ}	-2.0	—	2.0	µA
MOSI, SCLK, $\overline{CS}$ SPI Input Terminals					
Low-Level Input Voltage	V_{IL}	-0.3	—	0.3 V_{DD}	V
High-Level Input Voltage	V_{IH}	0.7 V_{DD}	—	V_{DD} +0.3	V
Pullup Input Current on $\overline{CS}$ $V_{\overline{CS}}$ = 4.0 V	$I_{PU\overline{CS}}$	-100	—	-20	µA
MOSI, SCLK Input Current 0.0 V < V_{IN} < V_{DD}	I_{IN}	-10	—	10	µA
$\overline{INT}$ Output Terminal					
Low-Level Output Voltage I_O = 1.5 mA	V_{OL}	0.0	—	0.9	V
High-Level Output Voltage I_O = -250 µA	V_{OH}	V_{DD} - 0.9	—	V_{DD}	V
$\overline{WDC}$ Terminal					
External Resistor Range	R_{EXT}	10	—	100	kΩ
HS1 and HS2 High-Side Output Terminals					
Output Clamp Voltage I_{OUT} = -100 mA	V_{CL}	-6.0	—	—	V
Output Drain-to-Source ON Resistance T_A = 25°C, I_{OUT} -150 mA T_A = 125°C, I_{OUT} -150 mA T_A = 125°C, I_{OUT} -120 mA	$R_{DS(ON)}$	— — —	2.0 — 3.0	2.5 4.5 4.0	Ω
Output Current Limitation	I_{LIM}	300	430	600	mA
Overtemperature Shutdown [13]	T_{OTSD}	155	—	190	°C
Output Leakage Current	I_{LEAK}	—	—	10	µA

Notes

13. When overtemperature occurs, switch is turned off and latched off. Flag is set in SPI Register. Refer to description on page 27.

Table 4. Static Electrical Characteristics for 33689D (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HS3 High-Side Output Terminal					
Output Drain-to-Source ON Resistance	$R_{DS(ON)}$				Ω
T_A = 25°C, I_{OUT} -50 mA		—	5.5	7.0	
T_A = 125°C, I_{OUT} -50 mA		—	—	10	
T_A = 125°C, I_{OUT} -30 mA		—	10	14	
Output Current Limitation	I_{LIM}	60	100	200	mA
Overtemperature Shutdown (14)	T_{OTSD}	155	—	190	°C
Output Leakage Current	I_{LEAK}	—	—	10	µA
OUT, E+, and E- Terminals at Current Sense Operational Amplifier					
Input Voltage – Rail-to-Rail at E+ and E-	V_{IMC}	-0.1	—	V_{CC} +0.1	V
Output Voltage Range at OUT	V_{OUT}				V
With ±1.0 mA Output Load Current		0.1	—	V_{CC} -0.1	
With ±5.0 mA Output Load Current		0.3	—	V_{CC} -0.3	
Input Bias Current	I_B	—	—	250	nA
Input Offset Voltage	V_{IO}	-15	—	15	mV
Input Offset Current	I_O	-100	—	100	nA
L1 and L2 Input Terminals					
Low-Voltage Detection Input Threshold Voltage	V_{THL}				V
5.5 V < V_{SUP} < 6.0 V		2.0	2.5	3.0	
6.0 V < V_{SUP} < 18 V		2.5	3.0	3.5	
18 V < V_{SUP} < 27 V		2.7	3.2	3.7	
High-Voltage Detection Input Threshold Voltage	V_{THH}				V
5.5 V < V_{SUP} < 6.0 V		2.7	3.3	3.8	
6.0 V < V_{SUP} < 18 V		3.0	4.0	4.5	
18 V < V_{SUP} < 27 V		3.5	4.2	4.7	
Input Hysteresis	V_{HYS}				V
5.5 V < V_{SUP} < 27 V		0.5	—	1.3	
Input Current	I_{IN}				µA
-0.2 V < V_{IN} < 40 V		-10	—	10	

Notes

14. When overtemperature occurs, switch is turned off and latched off. Flag is set in SPI Register. Refer to description on page 27.

Table 4. Static Electrical Characteristics for 33689D (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
RXD Output Terminal (LIN Physical Layer)					
Low-Level Output Voltage I_{OUT} ≤ 1.5 mA	V_{OL}	 0.0	 —	 0.9	V
High-Level Output Voltage I_{OUT} ≤ 250 µA	V_{OH}	 3.75	 —	 5.25	V
TXD Input Terminal (LIN Physical Layer)					
Low-Level Input Voltage	V_{IL}	—	—	1.5	V
High-Level Input Voltage	V_{IH}	3.5	—	—	V
Input Hysteresis	V_{INHYS}	50	145	300	mV
Pullup Current Source 1.0 V < V_{TXD} < 3.5 V	I_{PUTXD}	 -100	 —	 -20	µA
LIN Physical Layer, Transceiver					
Transceiver Output Voltage Dominant State, TXD LOW, External Bus Pullup 500 Ω Recessive State, TXD HIGH, I_{OUT} = 1.0 µA	 V_{LINDOM} V_{LINREC}	 — V_{SUP}-1.0	 — —	 1.4 —	V
Pullup Resistor to VSUP In Normal Mode and in Sleep and Stop Modes When Not Disabled by SPI	R_{PU}	 20	 30	 47	kΩ
Pullup Current Source In Sleep and Stop Modes When Pullup Disabled by SPI	I_{PULIN}	 —	 1.3	 —	µA
Output Current Shutdown Threshold	I_{OUTSD}	50	75	150	mA
Leakage Output Current to GND VS1 and VS2 Disconnected, V_{LIN} = 18 V Recessive State, 8.0 V < V_{SUP} < 18 V, 8.0 V < V_{LIN} < 18 V GND Disconnected, V_{GND} = V_{SUP}, V_{LIN} = -18 V	$I_{BUSLEAK}$	 — 0.0 -1.0	 1.0 3.0 —	 10 20 1.0	 µA µA mA
LIN Physical Layer, Receiver					
Receiver Input Threshold Voltage Dominant State, TXD HIGH, RXD LOW Recessive State, TXD HIGH, RXD HIGH Center (V_{BUSDOM}-V_{BUSREC})/2 Hysteresis (V_{BUSDOM}-V_{BUSREC})	 V_{BUSDOM} V_{BUSREC} V_{BUSCNT} V_{BUSHYS}	 0.0 0.6 0.475 —	 — — 0.5 —	 0.4 1.0 0.525 0.175	V_{SUP}
Bus Wake-Up Threshold	V_{BUSWU}	—	0.5	—	V_{SUP}

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics for 33689D

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI Interface Characteristics					
SPI Operation Frequency	f_{SPI}	0.25	—	4.0	MHz
SCLK Clock Period	t_{PSCLK}	250	—	N/A	ns
SCLK Clock High Time	t_{WSCLKH}	125	—	N/A	ns
SCLK Clock Low Time	t_{WSCLKL}	125	—	N/A	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	t_{LEAD}	100	—	N/A	ns
Falling Edge of SCLK to $\overline{CS}$ Rising Edge	t_{LAG}	100	—	N/A	ns
MOSI to Falling Edge of SCLK (Data Setup Time)	$t_{SI(SU)}$	40	—	N/A	ns
Falling Edge of SCLK to MOSI (Data Hold Time)	$t_{SI(HOLD)}$	40	—	N/A	ns
MISO Rise Time (15) C_L = 220 pF	t_{RSO}	—	25	50	ns
MISO Fall Time (15) C_L = 220 pF	t_{FSO}	—	25	50	ns
Time from Falling or Rising Edge of $\overline{CS}$ to: (15) MISO Low Impedance (Enable) MISO High Impedance (Disable)	 $t_{SO(EN)}$ $t_{SO(DIS)}$	 0.0 0.0	 — —	 50 50	ns
Time from Rising Edge of SCLK to MISO Data Valid (15) 0.2 V_{DD} ≤ MISO ≥ 0.8 V_{DD}, C_L = 100 pF	t_{VALID}	0.0	—	50	ns
$\overline{RST}$ Output Terminal in Normal and Stop Modes					
Reset Duration After VDD HIGH	$t_{DUR\overline{RST}}$	0.65	1.0	1.35	ms
$\overline{WDC}$ Terminal					
Watchdog Period Accuracy Using an External Resistor (Excluding Resistor Tolerances) (16)	$ACC_{\overline{WDC}}$	-15	—	15	%
Watchdog Time Period (16) 10 kΩ External Resistor 100 kΩ External Resistor No External Resistor, $\overline{WDC}$ Open, Normal Mode	$t_{\overline{WDC}}$	 — — 107	 10.558 99.748 160	 — — 215	ms

Notes

15. Parameter guaranteed by design; however, it is not production tested.
16. Watchdog time period calculation formula: $t_{\overline{WDC}}$ = 0.991 * R + 0.648 (R in kΩ and $t_{\overline{WDC}}$ in ms).

Table 5. Dynamic Electrical Characteristics for 33689D (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Current Sense Operational Amplifier					
Supply Voltage Rejection Ratio (17)	SVR	60	—	—	dB
Common Mode Rejection Ratio (17)	CMR	70	—	—	dB
Gain Bandwidth (17)	GBP	1.0	—	—	MHz
Output Slew Rate	SR	0.5	—	—	V/µs
Phase Margin	PHMO	40	—	—	deg.
Open Loop Gain (17)	OLG	—	85	—	dB
L1 and L2 Input Terminals					
Wake-Up Filter Time (17)	t_{WUF}	8.0	20	38	µs
State Machine Timing					
Delay Between $\overline{CS}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop Mode Activation (17)	t_{STOP}				µs
Minimum Watchdog Period		1.4	—	5.0	
No Watchdog Selected		6.0	—	30	
Maximum Watchdog Period		12	—	50	
Interrupt Low-Level Duration	$t_{\overline{INT}}$	7.0	10	13	µs
Internal Oscillator Frequency Accuracy (All Modes, for Information Only)	f_{OSC}	-35	—	35	%
Normal Request Mode Time-Out (Normal Request Mode)	t_{NRTOUT}	97	150	205	ms
Delay Between SPI Command and HS1 or HS2 Turn On (18), (19) Normal Mode, V_{SUP} > 9.0 V, V_{HS} ≥ 0.2 V_{VS2}	t_{SHSON}	—	—	20	µs
Delay Between SPI Command and HS1 or HS2 Turn Off (18), (19) Normal Mode, V_{SUP} > 9.0 V, V_{HS} ≤ 0.8 V_{VS2}	t_{SHSOFF}	—	—	20	µs
Delay Between SPI Command and HS3 Turn On (18), (20) Normal Mode, V_{SUP} > 9.0 V, V_{HS} ≥ 0.2 V_{VS2}	t_{SHSON}	—	—	20	µs
Delay Between SPI Command and HS3 Turn Off (18), (20) Normal Mode, V_{SUP} > 9.0 V, V_{HS} ≤ 0.8 V_{VS2}	t_{SHSOFF}	—	—	20	µs
Delay Between Normal Request and Normal Mode After a Watchdog Trigger Command (Normal Request Mode) (17)	t_{SNR2N}	7.0	15	30	µs
Delay Between $\overline{CS}$ Wake-Up ($\overline{CS}$ LOW to HIGH) in Stop Mode and:					µs
Normal Request Mode, VDD ON and $\overline{RST}$ HIGH	$t_{WU\overline{CS}}$	15	40	80	
First Accepted SPI Command	t_{WUSPI}	90	—	N/A	
Delay Between Interrupt Pulse in Stop Mode After Wake-Up and First Accepted SPI Command	$t_{S1STSPI}$	30	—	N/A	µs
Minimum Time Between Rising and Falling Edge on the $\overline{CS}$	$t_{2\overline{CS}}$	15	—	—	µs

Notes

17. Parameter guaranteed by design; however, it is not production tested.
18. When IN input is set to HIGH, delay starts at falling edge of clock cycle #8 of the SPI command and start of device activation/deactivation. 30 mA load on high-side switches. Excluding rise or fall time due to external load.
19. When IN is used to control the high-side switches, delays are measured between IN and HS1 or HS2 ON/OFF. 30 mA load on high-side switches, excluding rise or fall time due to external load.
20. Delay between turn on or turn off command and HS ON or HS OFF, excluding rise or fall time due to external load.

Table 5. Dynamic Electrical Characteristics for 33689D (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN Physical Layer: Bus Driver Timing Characteristics for Normal Slew Rate (21)					
Propagation Delay TXD to LIN (22)					µs
Dominant State Minimum Threshold (50% TXD to 58.1% V_{SUP})	t_{DOMMIN}	—	—	50	
Dominant State Maximum Threshold (50% TXD to 28.4% V_{SUP})	t_{DOMMAX}	—	—	50	
Recessive State Minimum Threshold (50% TXD to 42.2% V_{SUP})	t_{RECMIN}	—	—	50	
Recessive State Maximum Threshold (50% TXD to 74.4% V_{SUP})	t_{RECMAX}	—	—	50	
Propagation Delay Symmetry					µs
t_{DOMMIN} - t_{RECMAX}	dt1s	-10.44	—	—	
t_{DOMMAX} - t_{RECMIN}	dt2s	—	—	11	
LIN Physical Layer: Bus Driver Timing Characteristics for Slow Slew Rate (21)					
Propagation Delay TXD to LIN (23)					µs
Dominant State Minimum Threshold (50% TXD to 61.6% V_{SUP})	t_{DOMMIN}	—	—	100	
Dominant State Maximum Threshold (50% TXD to 25.1% V_{SUP})	t_{DOMMAX}	—	—	100	
Recessive State Minimum Threshold (50% TXD to 38.9% V_{SUP})	t_{RECMIN}	—	—	100	
Recessive State Maximum Threshold (50% TXD to 77.8% V_{SUP})	t_{RECMAX}	—	—	100	
Propagation Delay Symmetry					µs
t_{DOMMIN} - t_{RECMAX}	dt1s	-22	—	—	
t_{DOMMAX} - t_{RECMIN}	dt2s	—	—	23	
LIN Physical Layer: Bus Driver Fast Slew Rate					
LIN High Slew Rate (Programming Mode)	dv/dt Fast	—	13	—	V/µs
LIN Physical Layer, Transceiver					
Output Current Shutdown Delay (24)	t_{OUTDLY}	—	10	—	µs

Notes

21. 7.0 V < V_{SUP} < 18 V, bus load C0 and R0 1.0 nF/1.0 kΩ, 6.8 nF/660 Ω, 10 nF/500 Ω. 50% of TXD signal to LIN signal threshold. See Figure 5, page 17.
22. See Figure 7, page 18.
23. See Figure 8, page 18.
24. Parameter guaranteed by design; however, it is not production tested.

Table 5. Dynamic Electrical Characteristics for 33689D (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0.0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN Physical Layer: Receiver Characteristics and Wake-Up Timings					
Propagation Delay LIN to RXD [25]					µs
Dominant State (LIN LOW to RXD LOW)	t_{RDOM}	—	3.0	6.0	
Recessive State (LIN HIGH to RXD HIGH)	t_{RREC}	—	3.0	6.0	
Symmetry (t_{RDOM} - t_{RREC})	t_{RSYM}	-2.0	—	2.0	
Bus Wake-Up Deglitcher (Sleep and Stop Modes) [26]	t_{PROPWL}	30	70	90	µs
Bus Wake-Up Event Reported					µs
From Sleep Mode [27]	t_{WU}	—	30	—	
From Stop Mode [28]	t_{WU}	—	20	—	

Notes

25. Measured between LIN signal threshold V_{INL} or V_{INH} and 50% of RXD signal.
26. See Figures 9 and 10, page 19.
27. t_{WU} is typically 2 internal clock cycles after a LIN rising edge is detected. In Sleep Mode, the measurement is done without a capacitor connected to the regulator. The delay is measured between the V_{SUP}/2 rising edge of the LIN bus and when V_{DD} reaches 3.0 V. The V_{DD} rise time is strongly dependent upon the decoupling capacitor at V_{DD} terminal. See Figure 9, page 19.
28. t_{WU} is typically 2 internal clock cycles after a LIN rising edge is detected. In Stop Mode, the delay is measured between the V_{SUP}/2 rising edge of the LIN bus and the falling edge of the $\overline{INT}$ terminal. See Figure 10, page 19.

TIMING DIAGRAMS

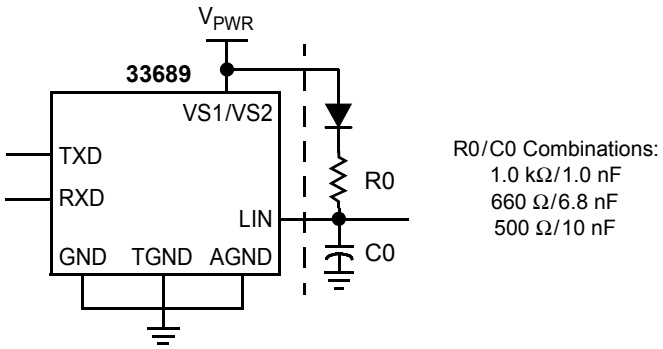
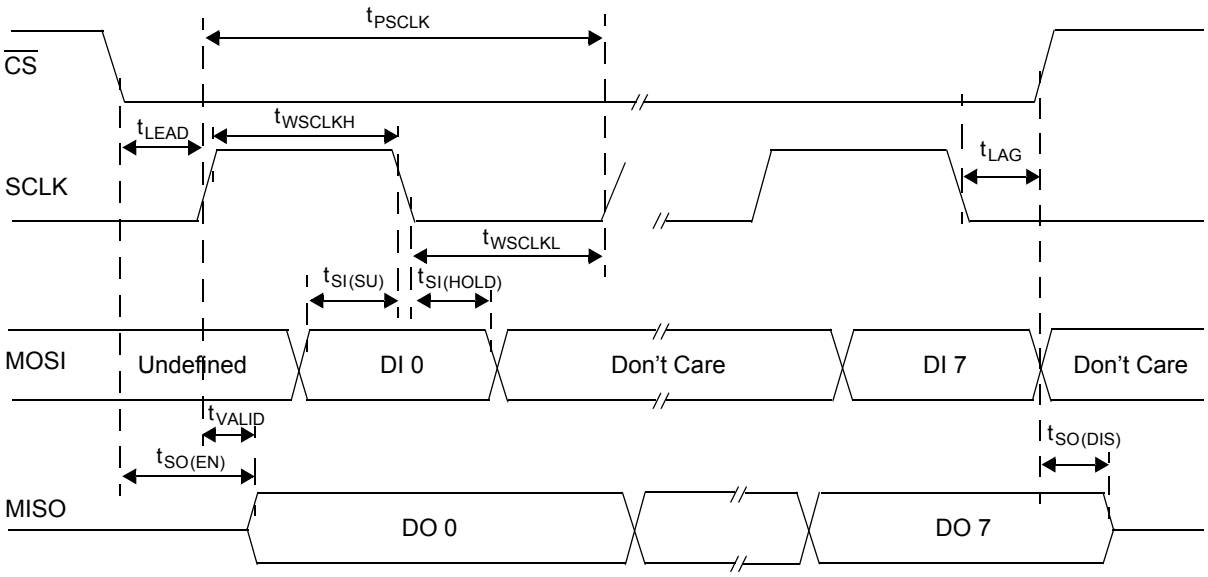


Figure 5. Test Circuit for Timing Measurements



Note Incoming data at MOSI terminal is sampled by the 33689 at SCLK falling edge. Outgoing data at MISO is set by the 33689 at SCLK rising edge (after t_{VALID} delay time).

Figure 6. SPI Timing Characteristics

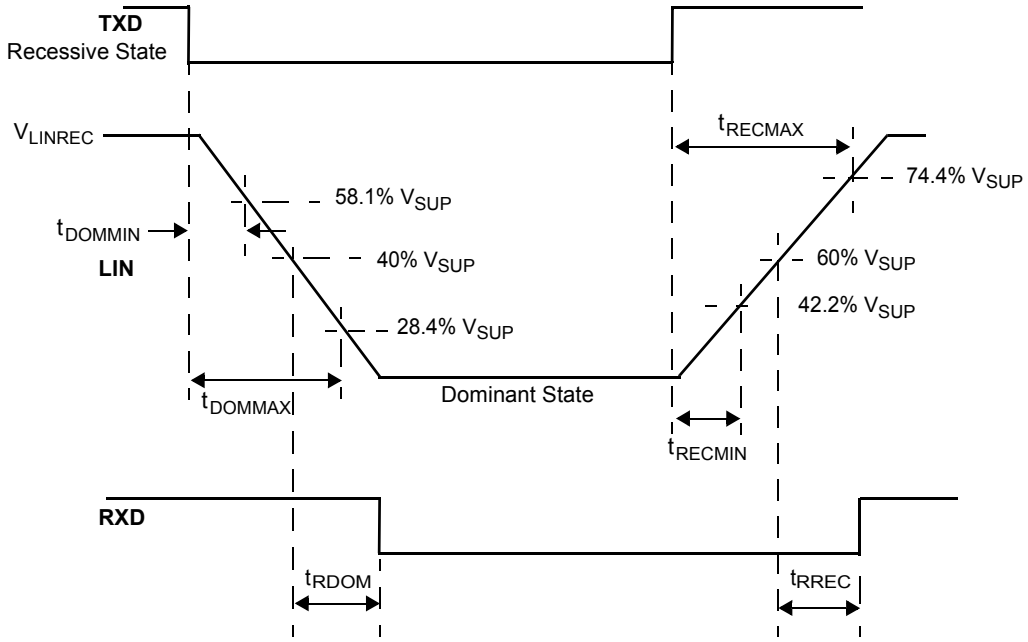


Figure 7. Timing Characteristics for Normal LIN Output Slew Rate

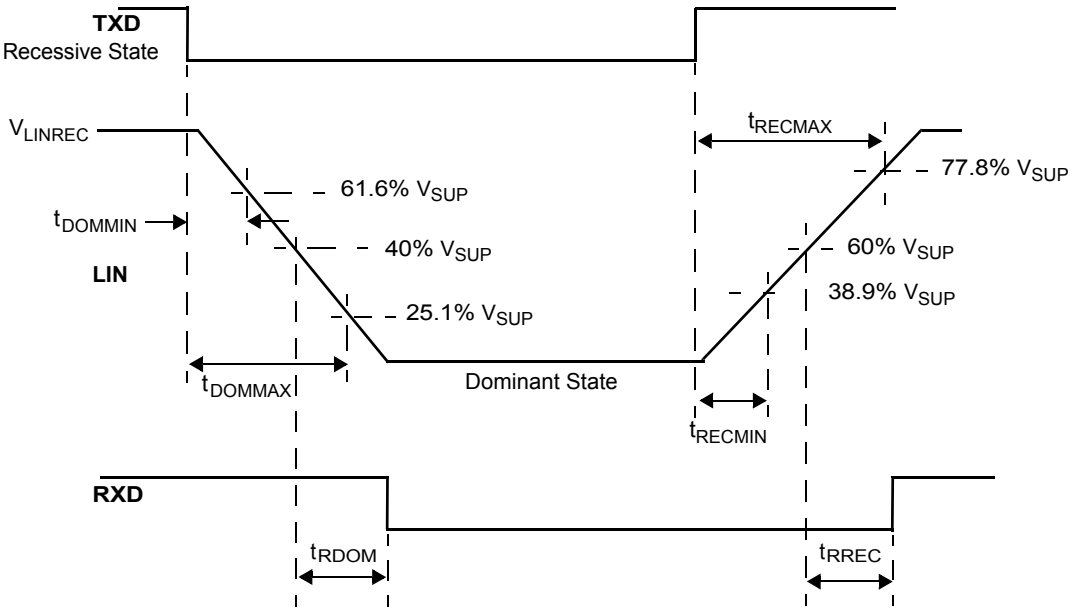


Figure 8. Timing Characteristics for Slow LIN Output Slew Rate

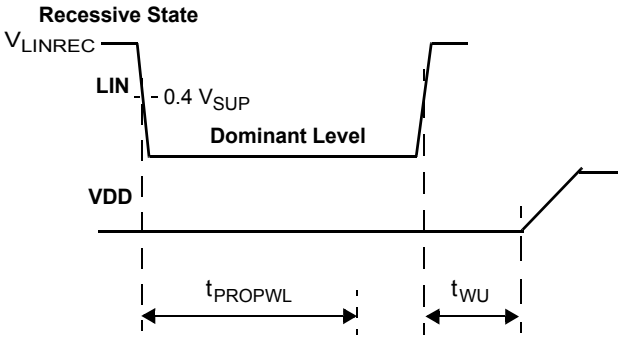


Figure 9. LIN Bus Wake-Up Behavior, Sleep Mode

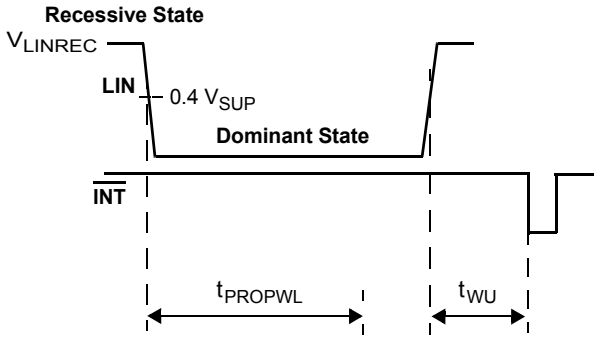


Figure 10. LIN Bus Wake-Up Behavior, Stop Mode

FUNCTIONAL DESCRIPTION FOR 33689D

INTRODUCTION

A System Basis Chip (SBC) is a monolithic IC combining many functions found in standard microcontroller-based systems; e.g., power management, communication interface, system protection, and diagnostics.

The 33689 is a SPI-controlled SBC combining many functions with a LIN transceiver for slave node applications. The 33689 has a 5.0 V, 50 mA regulator with undervoltage reset, output current limiting, overtemperature pre-warning, and thermal shutdown. An externally selectable timing Window Watchdog is also included.

The LIN transceiver has waveshaping that can be disabled when high data rates are warranted. A single 50 mA and two 150 mA fully protected high-side switches with output clamping are available for switching inductive or resistive loads. The 150 mA switches are PWM capable.

Two high-voltage inputs can be used to monitor switches or provide external wake-up. An internal current sense operational amplifier is available for load current monitoring.

FUNCTIONAL TERMINAL DESCRIPTION

LEVEL 1 AND LEVEL 2 INPUT TERMINALS (L1 AND L2)

These terminals are used to sense external switches and to wake up the 33689 from Sleep or Stop mode. During Normal mode, the state of these terminals can be read through the SPI Register. (Refer to the section entitled SPI Interface and Register Description on page 25 for information on the SPI Register.)

HIGH-SIDE DRIVER OUTPUT TERMINALS 1 AND 2 (HS1 AND HS2)

These two high-side switches are able to drive loads such as relays or lamps. They are protected against overcurrent and overtemperature and include internal clamp circuitry for inductive load protection. Switch control is done through selecting the correct bit in the SPI Register. HS1 and HS2 can be PWM-ed if required through the IN input terminal. The internal circuitry that drives both high-side switches is an AND function between the SPI bit HS1 (or HS2) and the IN input terminal.

If no PWM control is required, the IN terminal must be connected to the VDD terminal.

HIGH-SIDE DRIVER OUTPUT TERMINAL 3 (HS3)

This high-side switch can be used to drive small lamps, Hall sensors, or switch pullup resistors. Control is done through the SPI Register only.

No direct PWM control is possible on this terminal.

This high-side switch features current limit to protect it against overcurrent and short circuit conditions. It is also protected against overtemperature.

VOLTAGE SUPPLY TERMINALS 1 AND 2 (VS1 AND VS2)

The 33689 is supplied from a battery line or other supply source through the VS1 and VS2 terminals. An external diode is required to protect against negative transients and reverse battery. The 33689 can operate from 4.5 V and under the jump start condition at 27 V DC. Device functionality is guaranteed down to 4.5 V at VS1 and VS2 terminals. These terminals sustain standard automotive voltage conditions such as load dump at 40 V.

LIN BUS TERMINAL (LIN)

The LIN terminal represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

VOLTAGE SOURCE TERMINAL (VDD)

The VDD terminal is the 5.0 V supply terminal for the MCU and the current sense operational amplifier.

CURRENT SENSE OPERATIONAL AMPLIFIER TERMINALS (E+, E-, VCC, AND OUT)

These are the terminals of the single-supply current sense operational amplifier.

- The E+ and the E- input terminals are the non-inverting and inverting inputs of the current sense operational amplifier, respectively.
- The OUT terminal is the output terminal of the current sense operational amplifier.
- The VCC terminal is the +5.0 V single-supply connection for the current sense operational amplifier.

The current sense operational amplifier is enabled in Normal mode only.

WATCHDOG CONFIGURATION TERMINAL ($\overline{\text{WDC}}$)

The $\overline{\text{WDC}}$ terminal is the configuration terminal for the internal watchdog. A resistor is connected to this terminal. The resistor value defines the watchdog period. If the terminal is left open, the watchdog period is fixed to its default value (150 ms typical). If no watchdog function is required, the $\overline{\text{WDC}}$ terminal must be connected to GND.

RESET OUTPUT TERMINAL ($\overline{\text{RST}}$)

The $\overline{\text{RST}}$ terminal is the 5.0 V regulator and Watchdog reset output terminal.

PWM INPUT CONTROL TERMINAL (IN)

The IN terminal is the external PWM control terminal for the HS1 and HS2 high-side switches.

SERIAL DATA CLOCK TERMINAL (SCLK)

The SCLK terminal is the SPI clock input terminal. MISO data changes on the negative transition of the SCLK. MOSI is sampled on the positive edge of the SCLK.

MASTER OUT SLAVE IN TERMINAL (MOSI)

The MOSI terminal receives SPI data from the MCU. This data input is sampled on the positive edge of SCLK.

MASTER IN SLAVE OUT TERMINAL (MISO)

The MISO terminal sends data to an SPI-enabled MCU. Data on this output terminal changes on the negative edge of the SCLK. When $\overline{\text{CS}}$ is HIGH, this terminal enters the high-impedance state.

CHIP SELECT TERMINAL ($\overline{\text{CS}}$)

The $\overline{\text{CS}}$ terminal is the chip select input terminal for SPI use. When this signal is high, SPI signals are ignored. Asserting this terminal LOW starts an SPI transaction. The transaction is completed when this signal returns HIGH.

INTERRUPT OUTPUT TERMINAL ($\overline{\text{INT}}$)

The $\overline{\text{INT}}$ terminal is used to report 33689 faults to the MCU. Interrupt pulses are generated for:

- Voltage regulator temperature pre-warning
- HS1, HS2, or HS3 thermal shutdown
- VS1 or VS2 overvoltage (20 V typical)
- VS1 or VS2 undervoltage (6.0 V typical)

If an interrupt is generated, then when the next SPI read operation is performed bit D7 in the SPI Register will be set to logic [1] and bits D6:D0 will report the interrupt source.

In cases of wake-up from the Stop mode, $\overline{\text{INT}}$ is set LOW in order to signal to the MCU that a wake-up event from the L1, L2, or LIN bus terminal has occurred.

RECEIVER OUTPUT TERMINAL (RXD)

The RXD terminal is the receiver output of the LIN interface and reports the state of the bus voltage (RXD LOW when LIN bus is dominant, RXD HIGH when LIN bus is recessive).

TRANSMITTER INPUT TERMINAL (TXD)

The TXD terminal is the transmitter input of the LIN interface and controls the state of the bus output (dominant when TXD is LOW, recessive when TXD is HIGH).

GROUND TERMINALS (GND, TGND, AND AGND)

The 33689 has three different types of ground terminals.

- The GND terminal is the electrical ground terminal for the device.
- The AGND is the analog ground terminal for the voltage regulator and current sense operational amplifier.
- The four TGND terminals are the thermal ground terminals for the device.

Important The GND, the AGND, and the four TGND terminals must be connected together to a ground external to the 33689.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

WINDOW WATCHDOG

The window watchdog can be configured using an external resistor at $\overline{WDC}$ terminal. The watchdog is cleared through MODE1 and MODE2 bit in the SPI Register (refer to Table 2, page 25; also refer to the section entitled FUNCTIONAL TERMINAL DESCRIPTION on page 20.

A watchdog clear is only allowed in the open window (see Figure 1). If the watchdog is cleared in the closed window or has not been cleared at the end of the open window, the watchdog will generate a reset on the $\overline{RST}$ terminal and reset the whole device.

Note The watchdog clear in Normal request mode (150 ms) (first watchdog clear) has no window.

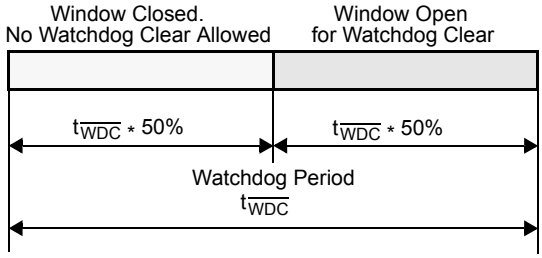


Figure 1. Window Watchdog Operation

Window Watchdog Configuration

If the $\overline{WDC}$ terminal is left open, the default watchdog period is selected (typ. 150 ms). If no watchdog function is required, the $\overline{WDC}$ terminal must be connected to GND.

The watchdog timer's period is calculated using the following formula:

$t_{\overline{WDC}}$ = 0.991 * R +0.648 (with R in kΩ and $t_{\overline{WDC}}$ in ms).

VDD VOLTAGE REGULATOR

The 33689 chip contains a low-power, low dropout voltage regulator to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main voltage regulator and the low-voltage reset circuit.

The VDD regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD terminal to provide the 5.0 V to the microcontroller.

Current Limit (Overcurrent) Protection

The voltage regulator has current limit to protect the device against overcurrent and short circuit conditions.

Overtemperature Protection

The voltage regulator also features overtemperature protection that has an overtemperature warning (Interrupt - VDDT) and an overtemperature shutdown.

Stop Mode

During Stop mode, the Stop mode regulator supplies a regulated output voltage. The Stop mode regulator has a limited output current capability.

Sleep Mode

In Sleep mode, the voltage regulator external VDD is turned off.

VDD VOLTAGE REGULATOR TEMPERATURE PREWARNING

VDD voltage regulator temperature prewarning (VDDT) is generated if the voltage regulator temperature is above the T_{PRE} threshold. It will set the VDDT bit in the SPI Register and an interrupt will be initiated. The VDDT bit remains set as long as the error condition is present.

During Sleep and Stop modes the VDD voltage regulator temperature prewarning circuitry is disabled.

HIGH-SIDE SWITCH THERMAL SHUTDOWN

The high-side switch thermal shutdown HSST is generated if one of the high-side switches HS1:HS3 is above the HSST threshold. It will shutdown the corresponding high-side switch and set the HSST flag in the SPI Register, and an interrupt will be initiated. The HSST bit remains set as long as the error condition is present. During Sleep and Stop modes the high-side switch thermal shutdown circuitry is disabled.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

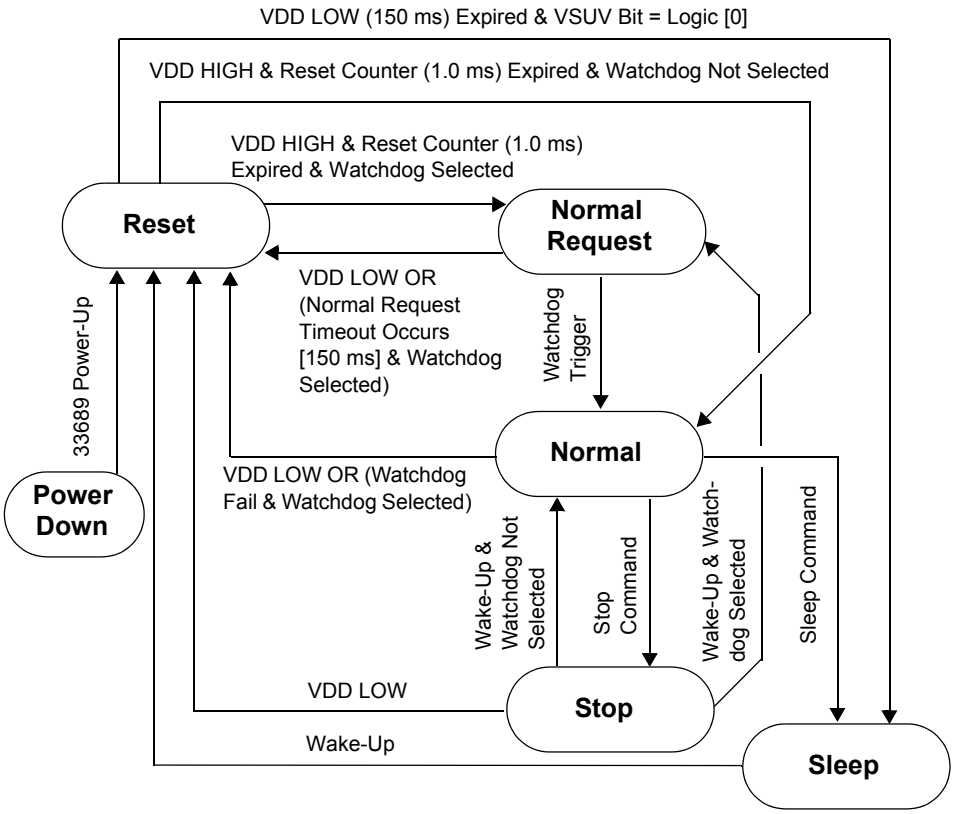
As described below and depicted in Figure 1 below and Table 1 on page 24, the 33689 has three operational modes: Normal, Sleep, and Stop. Operational modes are controlled by MODE1 and MODE2 bits in the SPI Register (refer to Logic Commands and Registers on page 25). In additional, there are two transitional modes: Reset and Normal Request.

RESET MODE

At power up, the 33689 switches automatically to Reset Mode for 1 ms if V_{DD} goes high. If V_{DD} stays low, after 150 ms the 33689 goes in Sleep Mode.

NORMAL REQUEST MODE

Before entering in Normal Request Mode, the 33689 stays for 1 ms in Reset Mode. In this mode, the LIN bus can transmit and receive information.



Legend
Watchdog Selected: External resistor between $\overline{WDC}$ terminal and GND or $\overline{WDC}$ terminal open.
Watchdog Not Selected: $\overline{WDC}$ terminal connected to GND.
Watchdog Fail: Watchdog trigger occurs in closed window or no SPI Watchdog trigger command.
Stop Command: SPI stop command.
Sleep Command: SPI sleep request followed by SPI sleep command.
Wake-Up: L1 or L2 state change or LIN bus wake-up or $\overline{CS}$ rising edge.

Figure 1. 33689 Modes State Diagram

NORMAL MODE

In Normal Mode, the 33689 has slew rate and timing compatible with the LIN protocol specification. The LIN bus can transmit and receive information. The V_{DD} regulator is ON and the watchdog function can be enabled.

SLEEP AND STOP MODE

To safely enter Sleep or Stop modes and to ensure that these modes are not inadvertently entered due to noise issues during SPI transmission, a dedicated sequence must be sent twice: data with the bits controlling the LIN bus and the device mode.

Entering Sleep Mode

First and second SPI commands (with bit D6=1, D7=1, D5 =0 or 1, D1=0, and D0=0) 11x00000 must be sent.

Entering Stop Mode

First and second SPI commands (with bit D6=1, D7=1, D5 =0 or 1, D1=0, and D0=1) 11x00001 must be sent.

Sleep or Stop modes are entered after the second SPI command. Register bit D5 must be set accordingly.

Table 1. Operational Modes and Associated Functions

Device Mode	VDD Voltage Regulator	Wake-Up Capabilities	$\overline{\text{RST}}$ Output	Watchdog Function	HS1, HS2, HS3	LIN Interface	Operational Amplifier
Reset	VDD: ON	N/A	LOW for 1.0 ms typical, then HIGH (if VDD above threshold)	Disabled	OFF	Recessive only	Not active
Normal Request	VDD: ON	N/A	HIGH. Active LOW if VDD undervoltage occurs and if Normal Request timeout (if Watchdog enabled)	150 ms timeout if Watchdog enabled	ON or OFF	Transmit and receive	Not active
Normal	VDD: ON	N/A	HIGH. Active LOW if VDD undervoltage occurs or if Watchdog fail (if Watchdog enabled)	Window Watchdog if enabled	ON or OFF	Transmit and receive	Active
Stop	VDD: ON (Limited current capability)	LIN and state change on L1:L2 inputs	Normally HIGH. Active LOW if VDD undervoltage occurs	Disabled	OFF	Recessive state with Wake capability	Not active
Sleep	VDD: OFF (Set to 5.0 V after Wake-Up to enter Normal Request)	LIN and state change on L1:L2 inputs	LOW. Go to HIGH after Wake-Up and VDD within specification	Disabled	OFF	Recessive state with Wake capability	Not active

LOGIC COMMANDS AND REGISTERS

SPI INTERFACE AND REGISTER DESCRIPTION

As shown in Figure 2, the SPI is an 8-bit SPI. All data is sent as bytes. The MSB, D7, is sent first. The minimum time between two rising edges on the $\overline{CS}$ terminal is 15 µs.

During an SPI data communication, the state of MISO reports the state of the 33689 at time of a $\overline{CS}$ HIGH-to-LOW transition. The status flags are latched at a $\overline{CS}$ HIGH-to-LOW transition.

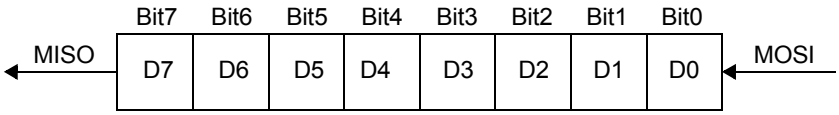


Figure 2. Data Format Description

The following tables describe the SPI Register bits, showing reset values and reset conditions.

Table 2. SPI Register Overview

Read/Write Information	MSB			Bits				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Write	LINSL2	LINSL1	LIN-PU	HS3	HS2	HS1	MODE2	MODE1
Read	INTSRC (1)	LINWU or LINFAIL	VSOV	VSUV or BATFAIL (2)	VDDT	HSST	L2	L1
Write Reset Value	0	0	0	0	0	0	—	—
Write Reset Condition	POR, RESET	POR, RESET	POR	POR, RESET	POR, RESET	POR, RESET	—	—

Notes
1. D7 signals interrupt source. After interrupt occurs, if D7 is a logic [1] D6:D0 indicate the interrupt source. If D7 is a logic [0] no interrupt has occurred and D6:D0 report real-time status.
2. The first SPI read after a 33689 reset returns the BATFAIL status flag bit D4.

SPI Register: Write Control Bits

LINSL2 and LINSL1—LIN Baud Rate and Low-Power Mode Pre-Selection Bits

These bits select the LIN slew rate and requested low-power mode in accordance with Table 3. Reset clears the LINSL2:1 bits.

Table 3. LIN Slew Rate Control and Device Low Power Mode Pre-Selection Bits (D7 and D6)

LINSL2	LINSL1	Description
0	0	LIN slew rate normal (baud rate up to 20 kbps)
0	1	LIN slew rate slow (baud rate up to 10 kbps)
1	0	LIN slew rate fast (for program download, baud rate up to 100 kbps)
1	1	Low power mode (Sleep or Stop mode) request, no change in LIN slew rate

LIN-PU—LIN Pullup Enable Bit

This bit controls the LIN pullup resistor during Sleep and Stop modes in accordance with Table 4. Reset clears the LIN-PU bit.

Table 4. LIN Pullup Termination Control Bit (D5)

LIN-PU	Description
0	30 kΩ pullup connected in Sleep and Stop mode
1	30 kΩ pullup disconnected in Sleep and Stop mode

HS3:HS1—High-Side H3:HS1 Enable Bits

These bits enable the HS3:HS1 bits in accordance with Table 5. Reset clears the HSx bit.

Note If no PWM on HS1 and HS2 is required, the IN terminal must be connected to the VDD terminal.

Table 5. High-Side Switches Control Bits (D4, D3, and D2)

HS3	Description	HS2	Description	HS1	Description
0	HS3 OFF	0	HS2 OFF	0	HS1 OFF
1	HS3 ON	1	HS2 ON (if IN = 1)	1	HS1 ON (if IN = 1)

MODE2 and MODE1—Mode Section Bits

The MODE2 and MODE1 bits control the 33689 operating modes in accordance with Table 6.

Table 6. Mode Control Bits (D1 and D0)

MODE2	MODE1	Description
0	0	Sleep mode (3)
0	1	Stop mode
1	0	Normal mode + Watchdog clear (4)
1	1	Normal mode

Notes

3. Special SPI command and sequence is implemented in order to avoid going into Sleep or Stop mode with a single 8-bit SPI command. Refer to Tables 7 and 8.
4. When a logic [0] is written to MODE1 bit while MODE2 bit is written as a logic [1]. After the SPI command is completed, MODE1 bit is set to logic [1] and the 33689 stays in Normal mode. In order to set the 33689 in Sleep mode, both MODE1 and MODE2 bits must be written in the same 8-bit SPI command. The Watchdog clear on Normal Request mode (150 ms) has no window.

To safely enter Sleep or Stop mode and to ensure that these modes are not affected by noise issue during SPI transmission, the Sleep/Stop commands require two SPI transmissions.

Sleep Mode Sequence The Sleep command, as shown in Table 7, must be sent twice.

Table 7. Sleep Command Bits

LINSL2	LINSL1	LIN-PU	HS3	HS2	HS1	MODE2	MODE1
1	1	x	0	0	0	0	0

x = Don't care.

Stop Mode Sequence The Stop command, as shown in Table 8, must be sent twice.

Table 8. Stop Command Bits

LINSL2	LINSL1	LIN-PU	HS3	HS2	HS1	MODE2	MODE1
1	1	x	0	0	0	0	1

x = Don't care.

SPI Register: Read Control Bits

INTSCR—Register Content Flags or Interrupt Source

The INTSCR bit, as shown in Table 9, indicates if the register contents reflect the flags or an interrupt/wake-up source.

Table 9. Interrupt Status (D7)

INTSCR	Description
0	SPI word read reflects the flag state
1	SPI word read reflects the interrupt or wake-up source

LINWU/LINFAIL—LIN Bus Status Flag Bit

This bit indicates a LIN wake-up condition or a LIN overcurrent/overtemperature in accordance with Table 10.

Table 10. LIN Bus Status (D6)

LINWU/ LINFAIL	Description
0	No LIN bus wake-up **or** failure
1	LIN bus wake-up occurred or LIN overcurrent/ overtemperature

VSOV—Overvoltage Flag Bit, VSUV/BATFAIL—Undervoltage Flag Bit, VDDT—VDD Voltage Regulator Status Flag Bit, and HSST—High-Side Status Flag Bit

Table 11 indicates the register contents of the following flags:

- VSOV flag is set on an overvoltage condition.
- VSUV/BATFAIL flag is set on an undervoltage condition.
- VDDT flag is set as pre-warning in case of an overtemperature condition on the voltage regulator.
- HSST flag is set on overtemperature conditions on one of the high-side outputs.

Table 11. Over- and Undervoltage, VDD Voltage Regulator, and High-Side Status Flag Bits (D5, D4, D3, and D2)

VSOV	Description	VSUV/ BATFAIL	Description	VDDT	Description	HSST	Description
0	V_{SUP} below 19 V	0	V_{SUP} above 6.0 V	0	No overtemperature	0	HS No overtemperature
1	V_{SUP} above 18 V	1	V_{SUP} below 6.0 V	1	VDD overtemperature pre-warning	1	HS1, HS2, or HS3 OFF (overtemperature)

L2 and L1—Wake-Up Inputs L2 and L1 Status Flag Bit

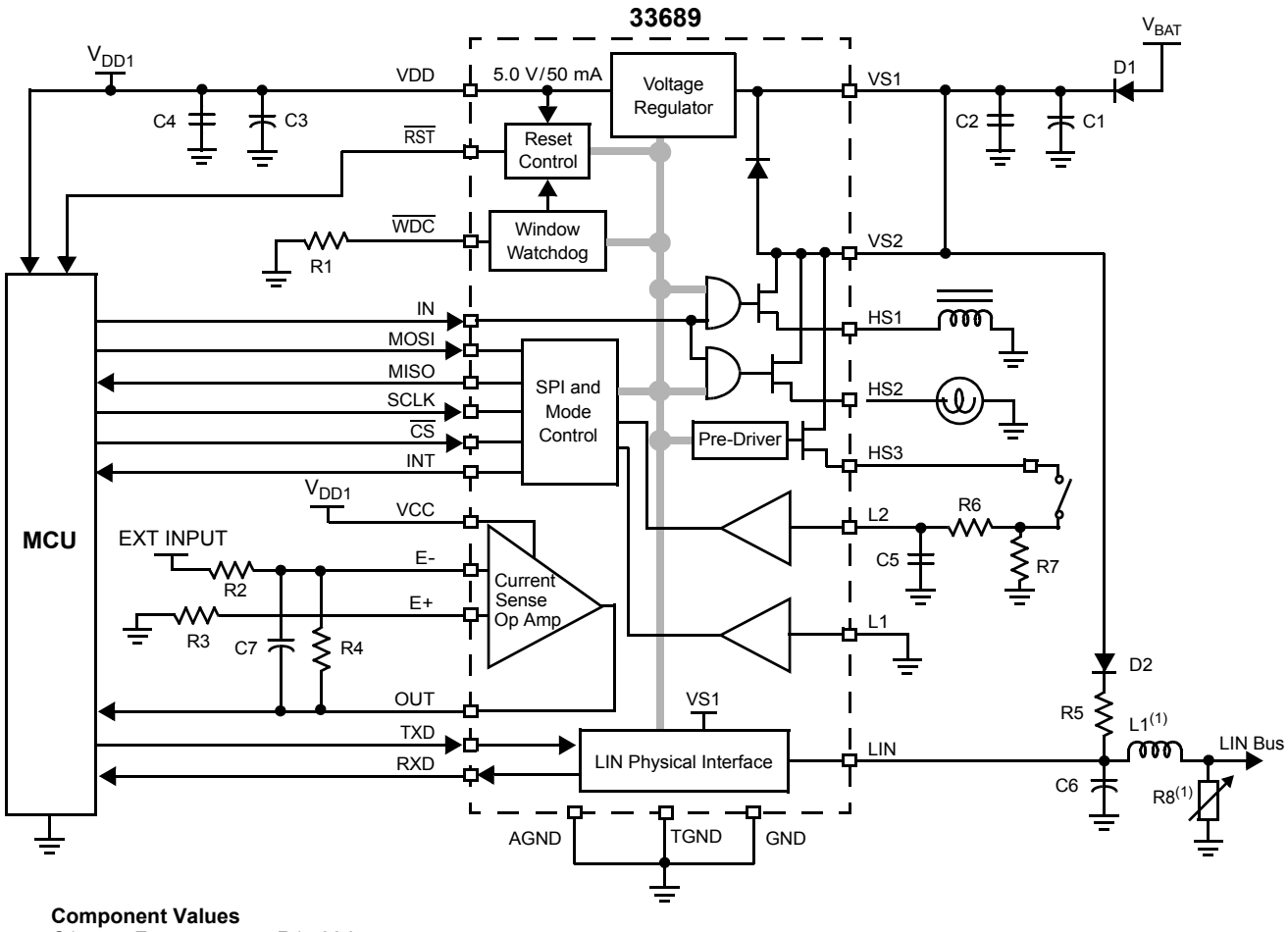
The L2 and L1 flags, as shown in Table 12, reflect the status of the L2 and L1 input terminals and indicate the wake-up source.

Table 12. Switch Input Wake-Up and Real Time Status (D1 and D0)

L2	Description	L1	Description
0	L2 input LOW	0	L1 input LOW
1	L2 input HIGH or wake-up by L2 (first register read after wake-up)	1	L1 input HIGH or wake-up by L1 (first register read after wake-up)

TYPICAL APPLICATIONS

The 33689 can be configured in several applications. Figure 3 shows the 33689 in the typical master node application.



Component Values

C1=47 µF	R1=33 kΩ
C2=C4=C5=100 nF	R2 and R3 depend on the application
C3=10 µF	R4>5.0 kΩ
C6=220 pF	R5=1.0 kΩ
C7=4.7 nF	R6=10 kΩ
	R7=2.2 kΩ
	R8=Varistor type TDK AVR-M1608C270MBAAB(1)
	L1 = SMD Ferrite Bead-Type TDK MMZ2012Y202B(1)

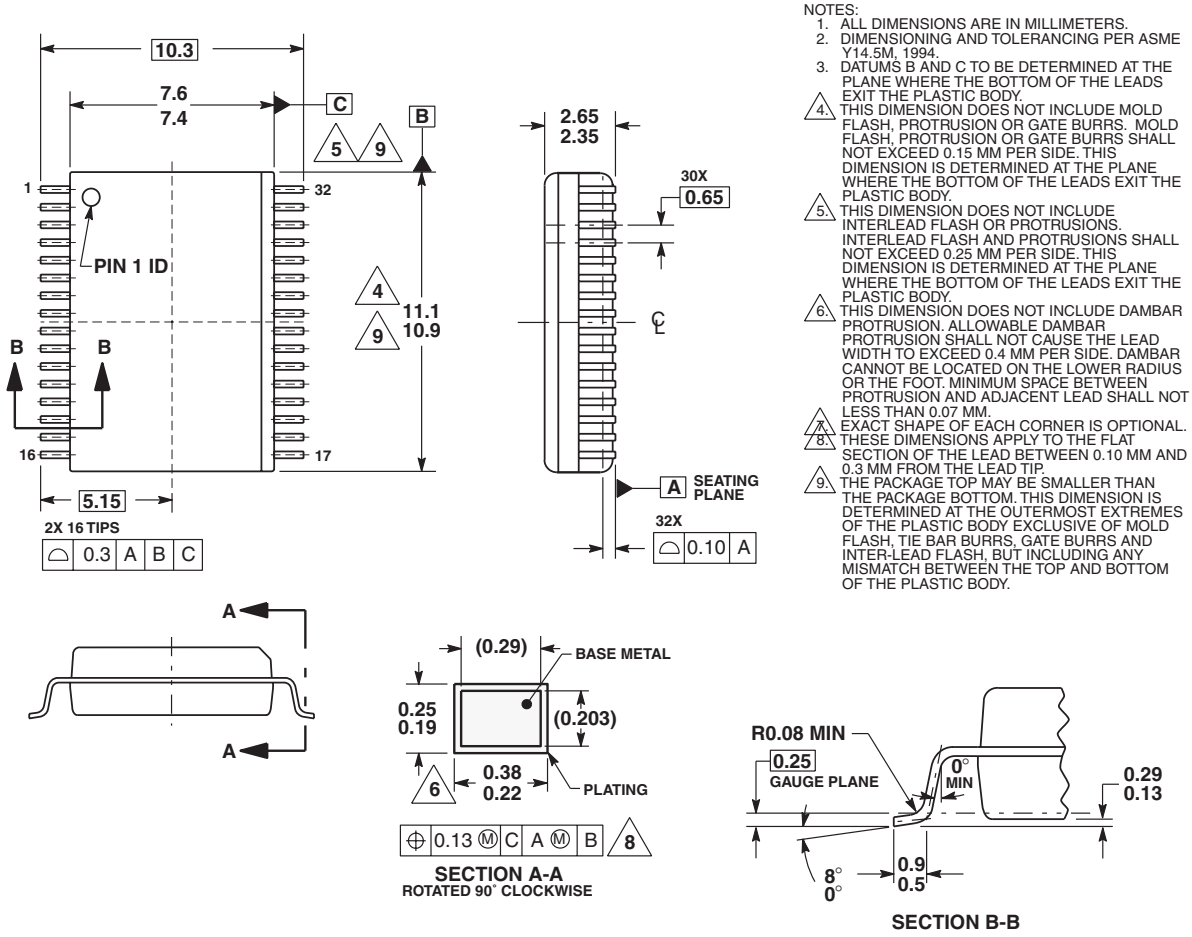
Notes:

1. L1 and R8 are external components to improve EMC and ESD performances.
2. Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

Figure 3. 33689 in Typical Master Node Application

PACKAGING DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98A drawing number below.



DWB SUFFIX
32-TERMINAL SOIC WIDE BODY
PLASTIC PACKAGE
98ARH99137A
ISSUE A

33689

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MOTOROLA
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TECHNICAL DATA

Product Preview

MC33689

System Basis Chip with LIN transceiver

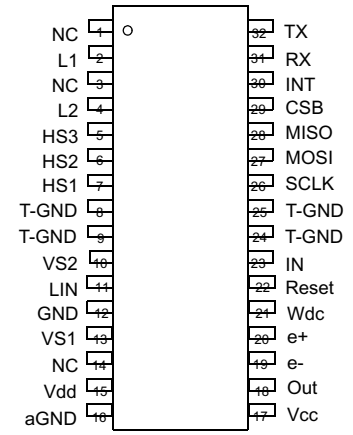
LIN System basis chip

SILICON MONOLITHIC
INTEGRATED CIRCUIT

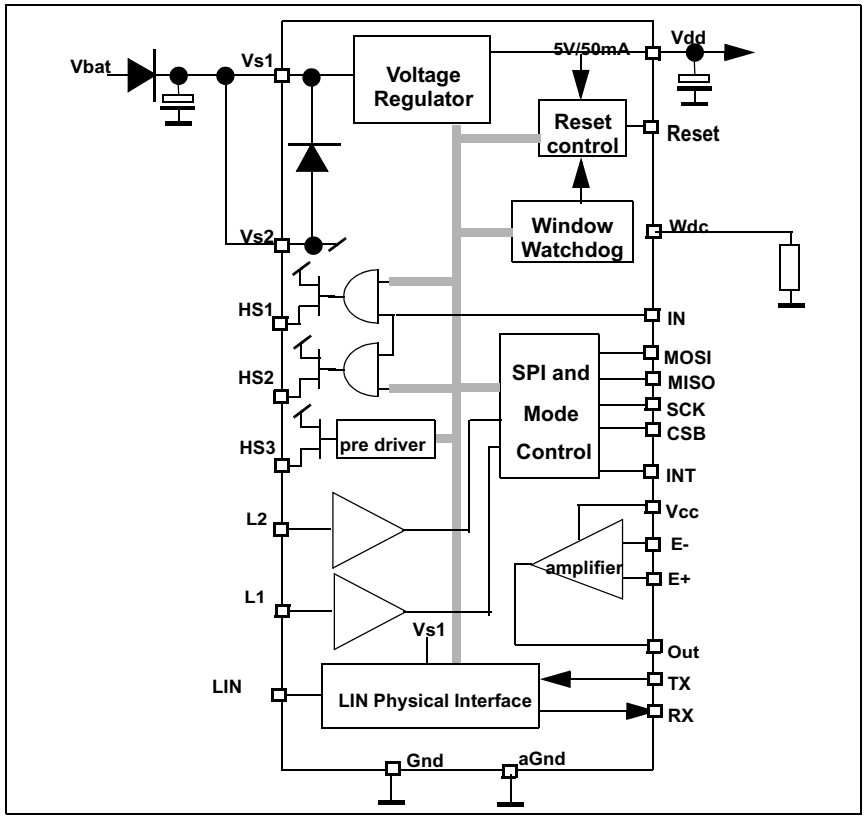
The LIN SBC is a monolithic integrated circuit combining many functions frequently used by automotive LIN distributed slave nodes. It incorporates:
- Single voltage regulator with low power modes
- LIN physical interface.
- Wake up inputs.
- Triple high side driver
- Current sense op amp

• Vdd: Low drop voltage regulator, current limitation, over temperature detection, monitoring and reset function, current capability 50mA.
• Programmable window watchdog
• Three operational modes (normal, stop and sleep modes)
• Low current consumption in sleep and stop modes
• LIN physical interface compatible with LIN standard.
• Two external high voltage wake-up inputs
• Dual high side switches, relay driver capability, internal clamp, PWM capability.
• Single low current high side switch, 50mA capability for switch bias and hall sensor supply
• Current sense amplifier
• Nominal DC operating voltage from 5.5 to 27V
• 40V maximum transient voltage
• Wake up capabilities (wake up inputs, LIN interface)

Pin out SO32WB fine pitch



Simplified Block Diagram

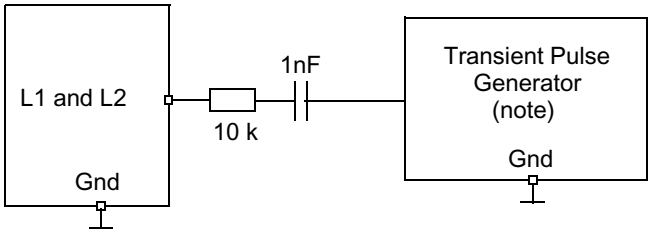


ORDERING INFORMATION		
Device	Operating Temperature Range	Package
MC33689DWB/R2	T_A = -40 to 125°C	SO-32

1 MAXIMUM RATINGS

Ratings	Symbol	Min	Typ	Max	Unit
ELECTRICAL RATINGS					
Supply Voltage at Vs1 and Vs2 - Continuous voltage - Transient voltage (Load dump)	 Vsupdc Vsuptr	 -0.3		 27 40	V
Supply Voltage Vdd and Vcc	Vdd	-0.3		5.5	V
Logic Inputs: MOSI, SCK, CSB, IN, Tx	Vinlog	- 0.3		Vdd+0.3	V
Logic output: MISO, INT, Rx, Reset	Voutlog	- 0.3		Vdd+0.3	V
Output current Vdd	Idd		Internally limited		A
E+, E- input voltage	Ve+-	-0.3		7	V
E+, E- input current	Ie+-	-20		20	mA
Out output voltage	Vout	-0.3		Vcc+0.3	V
Out output current	Iout	-20		20	mA
L1 and L2 - DC Input voltage with a 33k resistor - Transient input voltage (according to ISO7637 specification) and with external component (see figure 1 below).	 Vlxdc Vlxtr	 -18V -100		 40 +100	 V V
HS1 and HS2 output	Vhs12	internally clamped		Vs2+0.3	V
HS3	Vhs3	-0.3		Vs2+0.3	V
LIN - DC voltage Transient input voltage (according to ISO7637 specification) and with external component (see figure 1 below).	 Vbusdc Vbustr	 -18 -150		 +40 +100	V
ESD voltage (HBM 100pF, 1.5k) (GND, T-GND and aGND pins connected together and configured as ground) - LIN, L1, L2 - All other pins	Vesdh	 -4 -2		 4 2	kV
ESD voltage (HBM 100pF, 1.5k) (GND pin configured as ground, T-GND and aGND pins as I/O) - LIN, L1, L2 - All other pins	Vesdh	 -4 -2		 4 2	kV
ESD voltage (Machine Model) All pins (GND, T-GND and aGND pins connected together and configured as ground)	Vesdm	-200		200	V
ESD voltage (Machine Model) All pins (GND pin configured as ground, T-GND and aGND pins as I/O)	Vesdm	-150		150	V
THERMAL RATINGS					
Junction Temperature	T_j	- 40		+150	∀C
Storage Temperature	T_s	- 55		+165	∀C
Ambient Temperature (for info only)	T_a	- 40		+85	∀C
Thermal resistance junction to ambient	Rthj/a			80	°C/W

Figure 1. : Transient test pulses for LIN and Wake pins



note: Waveform in accordance to ISO7637 part1, test pulses 1, 2, 3a and 3b.

2 ELECTRICAL CHARACTERISTICS

(V_{s1} and V_{s2} from 5.5V to 18V and T_{amb} from -40°C to 125°C unless otherwise noted)

Description	Symbol	Characteristics			Unit	Conditions
		Min	Typ	Max		
Vs1 and Vs2 pins (Device power supply)						
Nominal DC Voltage range	Vsup	5.5		18	V	
Input Voltage during Load Dump	VsupLD			40	V	Load dump situation
Input Voltage during jump start	VsupJS			27	V	Jump start situation (note 1)
Supply Current in Normal Mode (note 2)	Isup(norm)		5	7.5	mA	Iout at Vdd =10mA, LIN recessive state
Supply Current in Sleep Mode (note 2)	Isleep		30	40	uA	Vdd off, Vsup<=13.5V
Supply Current in Stop Mode (note 2)	Istop		60	75	uA	Vdd ON with Iout<100uA, Vsup<=13.5V
Supply voltage fall early warning threshold	VSUVew	5.7	6	6.6	V	Normal mode, INT generated, bit VSUV set
VSUV flag hysteresis	VSUVhyst		1		V	guaranteed by design
Supply voltage over voltage warning threshold	VSOVw	18	19.25	20.50	V	Normal mode, INT generated, bit VSOV set
VSOV flag hysteresis	VSOVhyst		220		mV	guaranteed by design

note 1: Device is fully functional. All functions are operating. Over temperature may occur.
note 2: Total current (IVs1+IVs2) measured at gnd pins.

Vdd (external 5V output for MCU supply). Specification with external capacitor 2uF<C<10uF and 200mOhms<=ESR<=1O ohm. Normal mode. Capacitor value up to 47uF chemical can be used.

Vdd Output Voltage	Vddout	4.75	5	5.25	V	Idd from 2 to 50mA 5.5V< Vsup <27V
Dropout Voltage (note 1)	Vdddrop		100	200	mV	Idd = 50mA (note 1) Vsup > 4.5V
Idd output current limitation (note 2)	Idd	50	110	200	mA	Internally limited
Over temperature pre warning (junction)	Tpre	120	135	160	∀C	Normal mode, INT generated, Bit VddT set guaranteed by design
Thermal Shutdown (junction)	Tsd	155	170		∀C	Normal mode guaranteed by design
Temperature threshold difference		20	30	45	°C	Normal mode (Tsd-Tpre) guaranteed by design
Vsup range for Reset Active	$Vsup_r$	3.5			V	0.5<Vdd<Vdd (Rst-th1)
Line Regulation	LR		20	150	mV	5.5V<V_{sup}<27V, I_{dd}=10mA
Load Regulation	LD		40	150	mV	1mA<I_{Idd}<50mA

note 1: measured when voltage has dropped 100mV below its nominal value.
note 2: total Vdd regulator current. A 5mA current for operational amplifier operation is included. Digital output supplied from Vdd.

Vdd: in Stop mode

Vdd Output Voltage (note 1)	Vddstop	4.75	5,00	5.25	V	Idd<=2mA
Idd current capability (note 2)	Idds	4	8	14	mA	Stop mode
Line regulation	LR-s		10	100	mV	5.5V<V_{sup}<27V, I_{dd}=2mA
Load regulation	LD-s		40	150	mV	1mA<I_{Idd}<5mA

note 1: when switching from Normal mode to Stop mode, or from Stop mode to Normal mode the output voltage can varies within the output voltage specification.
note 2: when Idd is above Idds device enters reset mode

Reset: normal and stop modes (output pin only)

Reset threshold	Rst-th1	4.50	4.68	Vdd-0.2	V	
High Level Output current	Ioh		-250		σA	V_{out}>0.7Vdd
Low Level Output Voltage (I_0=1.5mA)	Vol	0		0.9	V	4.5V<V_{sup}<27V

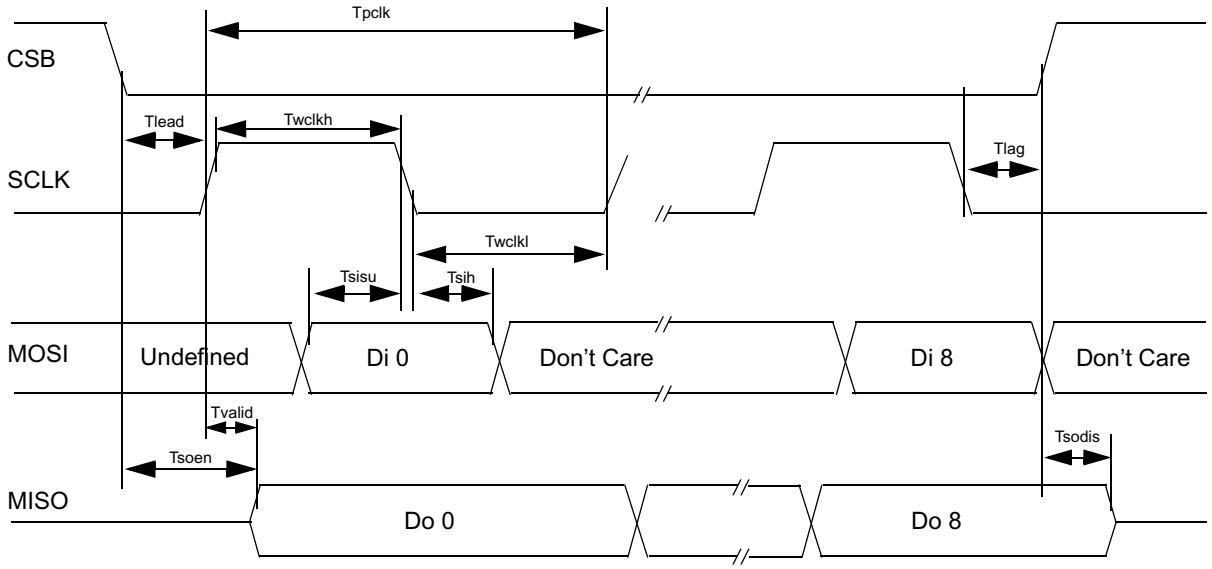
(V_{s1} and V_{s2} from 5.5V to 18V and T_{amb} from -40°C to 125°C unless otherwise noted)

Description	Symbol	Characteristics			Unit	Conditions
		Min	Typ	Max		
Reset pull down current	Ipdw	1.5		8	mA	Internally limited. Vdd<4V, Vreset = 4.6V
Reset Duration after Vdd High	reset-dur	0.65	1	1.35	ms	
IN: input						
High Level Input Voltage	Vih	0.7Vdd		Vdd+0.3	V	
Low Level Input Voltage	Vil	-0.3		0.3Vdd	V	
Input Current	Iin	-10		10	σA	$0<V_{IN}<Vdd$
MISO: SPI output						
Low Level Output Voltage	Vol	0		1.0	V	I out = 1.5mA
High Level Output Voltage	Voh	Vdd-0.9		Vdd	V	I out = -250uA
Tristated MISO Leakage Current		-2		+2	uA	$0V<V_{miso}<Vdd$
MOSI, SCLK, CSB: SPI input						
High Level Input Voltage	Vih	0.7Vdd		Vdd+0.3		
Low Level Input Voltage	Vil	-0.3		0.3Vdd	V	
CSB Pull up current source	Iih	-100		-20	uA	V_i 1V to 3.5V
MOSI, SCK Input Current	Iin	-10		10	uA	$0<V_{IN}<Vdd$
SPI: DIGITAL INTERFACE TIMING						
SPI operation frequency	Freq	0.25		4	MHz	
SCLK Clock Period	t_{pCLK}	250		N/A	ns	
SCLK Clock High Time	t_{wSCLKH}	125		N/A	ns	
SCLK Clock Low Time	t_{wSCLKL}	125		N/A	ns	
Falling Edge of CS to Rising Edge of SCLK	t_{lead}	100		N/A	ns	
Falling Edge of SCLK to CS Rising Edge	t_{lag}	100		N/A	ns	
MOSI to Falling Edge of SCLK	t_{SISU}	40		N/A	ns	
Falling Edge of SCLK to MOSI	t_{SIH}	40		N/A	ns	
MISO Rise Time (CL = 220pF)	t_{rSO}		25	50	ns	guaranteed by design
MISO Fall Time (CL = 220pF)	t_{fSO}		25	50	ns	guaranteed by design
Time from Falling or Rising Edges of CS to: - MISO Low Impedance - MISO High Impedance	 t_{SOEN} t_{SODIS}	0		 50 50	ns	guaranteed by design
Time from Rising Edge of SCLK to MISO Data Valid	t_{valid}	0		50	ns	0.2 V1=<MISO>=0.8V1, C_L=100pF guaranteed by design

(V_{s1} and V_{s2} from 5.5V to 18V and T_{amb} from -40°C to 125°C unless otherwise noted)

Description	Symbol	Characteristics			Unit	Conditions
		Min	Typ	Max		

Figure 2. SPI Timing characteristic



Note:
Incoming data at MOSI pin is sampled by the SBC at SCLK falling edge.
Outcoming data at MISO pin is set by the SBC at SCLK rising edge (after Tvalid delay time)

INT: output pin

Low Level Output Voltage (I_0=1.5mA)	Vol	0		0.9	V	
High Level Output Voltage (I_0=-250uA)	Voh	Vdd-0.9		Vdd		

WDC: window watchdog configuration pin

External resistor range	Rext	10		100	kohms	
Watchdog period accuracy with external resistor	Wdcacc	-15		15	%	Excluding resistor accuracy. Note 1
Watchdog period with external resistor	Wdp 10		10.558		ms	R = 10 kohms. note 1
Watchdog period with external resistor	Wdp 100		99.748		ms	R = 100 kohms. note 1
Watchdog period without external resistor, Conf pin open	PWdoff	97	150	205	ms	Normal mode

note 1: watchdog timing period calculation formula: **Twd = 0.991 * R + 0.648** (R in kohms and Twd in ms).

HS1 and HS2: High side output pin

Rdson at Ta=25°C, and Iout -150mA	Ron25		2	2.5	Ohms	Vsup>9V
Rdson at Ta=125°C, and Iout -150mA	Ron125			4.5	Ohms	Vsup>9V
Rdson at Ta=125°C, and Iout -120mA	Ron3		3		Ohms	5.5<Vsup<9V
Output current limitation	Ilim	300	430	600	mA	
Over temperature Shutdown	Ovt	155		190	°C	note 1
Leakage current	Ileak			10	uA	
Output Clamp Voltage at Iout = -100mA	Vcl	-6			V	

(V_{s1} and V_{s2} from 5.5V to 18V and T_{amb} from -40°C to 125°C unless otherwise noted)

Description	Symbol	Characteristics			Unit	Conditions
		Min	Typ	Max		
note 1: when over temperature occurs, switch is turned off and latched off. Flag is set in SPI.						
HS3: High side output pin						
Rdson at Tj=25°C, and Iout -50mA	Ron25			7	Ohms	Vsup>9V
Rdson at Ta=125°C, and Iout -50mA	Ron125			10	Ohms	Vsup>9V
Rdson at Ta=125°C, and Iout -30mA	Ron3			14	Ohms	5.5<Vsup<9V
Output current limitation	Ilim	60	100	200	mA	
Over temperature Shutdown	Ovt	155		190	°C	note 1
Leakage current	Ileak			10	uA	
note 1: when over temperature occurs, switch is turned off and latched off. Flag is set in SPI						
SENSE CURRENT AMPLIFIER SECTION:						
Rail to rail input voltage	Vimc	-0.1		Vcc+0.1	V	
Output voltage range	Vout1	0.1		Vcc-0.1	V	Output current +- 1mA
Output voltage range	Vout2	0.3		Vcc-0.3	V	Output current +-5 mA
Input bias current	Ib			250	nA	
Input offset current	Io	-100		100	nA	
Input offset voltage	Vio	-15		15	mV	
Supply voltage rejection ratio	SVR	60			dB	Guaranteed by design
Common mode rejection ratio	CMR	70			dB	Guaranteed by design
Gain bandwidth	GBP	1			Mhz	Guaranteed by design
Slew rate	SR	0.5			V/us	
Phase margin	PHMO	40			°	For gain=1,load 100pF// 5kohms. Guaranteed by design
Open loop gain	OLG		85		dB	Guaranteed by design
L1, L2 inputs						
Negative Switching Threshold	Vthn	2 2.5 2.7	2.5 3 3.2	3 3.5 3.7	V	5.5V<Vsup<6V 6V<Vsup<18V 18V<Vsup<27
Positive Switching Threshold	Vthp	2.7 3 3.5	3.3 4 4.2	3.8 4.5 4.7	V	5.5V<Vsup<6V 6V<Vsup<18V 18V<Vsup<27
Hysteresis	Vhyst	0.5		1.3	V	5.5V<Vsup<27
Input current	Iin	-10		10	uA	-0.2V < Vin < 40V
Wake up Filter Time	Twuf	8	20	38	us	Guaranteed by design

STATE MACHINE TIMING

Delay between CSB low to high transition (at end of SPI stop command) and Stop mode activation (Guaranteed by design)	Tstop-m Tstop-nw Tstop-M	1.4 6 12		5 30 50	us us us	Minimum Watchdog period No watchdog selected Maximum watchdog period
Interrupt low level duration	Tint	7	10	13	us	
Internal oscillator frequency accuracy	Osc-f1	-35		35	%	All modes, for info only
Normal request mode time out	NRtout	97	150	205	ms	Normal request mode
Delay between SPI command and HS1, HS2 or HS3 turn on (note 1, 2)	Ts-HSon			20	us	Normal mode Vsup>9V, Vhs >= 0.2 Vs1
Delay between SPI command and HS1, HS2 or HS3 turn off (note 1, 2)	Ts-HSoff			20	us	Normal mode Vsup>9V, Vhs <= 0.8 Vs1
Delay between Normal Request and Normal mode, after W/D trigger command	Ts-NR2N	6	35	30	us	Normal request mode, Guaranteed by design
Delay between CSB wake up (CSB low to high) and SBC normal request mode (Vdd1 on & reset high)	Tw-csb	15	40	80	us	SBC in stop mode

(V_{s1} and V_{s2} from 5.5V to 18V and T_{amb} from -40°C to 125°C unless otherwise noted)

Description	Symbol	Characteristics			Unit	Conditions
		Min	Typ	Max		
Delay between CSB wake up (CSB low to high) and first accepted SPI command	Tw-spi	90		N/A	us	SBC in stop mode
Delay between INT pulse and 1st SPI command accepted	Ts-1stspi	30		N/A	us	In stop mode after wake up
The minimum time between two rising edges on the CSB	T2csb	15			us	

note 1: when IN input is set to high, delay starts at falling edge of clock cycle #8 of the SPI command and start of device activation/deactivation. 30mA load on HS switches. Excluding rise or fall time due to external load.

note 2: when IN used to control HS switches, delays measured betxween IN and HS1 or HS2 on /off. 30mA load on HS switches. Excluding rise or fall time due to external load.

Rx: LIN physical layer output

Low Level Voltage Output	Vol	0		0.9	V	I in Ω+1.5mA
High Level Voltage Output	Voh	3.75		5.25	V	I out Ω250uA

Tx: LIN physical layer input

Low Level Voltage Input	Vil			1.5	V	
High Level Voltage Input	Vih	3.5			V	
Input Threshold Hysteresis	Vinhyst	50	550	800	mV	
Pull-up Current Source	Is	-100		-20	uA	1V <V(Tx) < 3.5V

LIN: physical layer bus (Voltage Expressed versus Vsup Voltage)

Low Level Dominant Voltage	Vlin-low			1.4	V	external bus pull 500 Ohms
High Level Voltage (Tx high, Iout = 1uA)	Vlin-high	Vsup-1			V	Recessive state
Pull up Resistor to Vsup	Rpu	20	30	47	kohms	In normal mode. In sleep and stop mode if not turned off by SPI
Pull up current source	Ipu		1.3		uA	In sleep and stop mode with 30k disconnected
Over current shutdown threshold	Iov-cur	50	75	150	mA	
Over current shutdown delay	Iov-delay		10		us	Guaranteed by design
Leakage Current to GND	Ibus-pas-rec	0	3	20	uA	Recessive state, Vsup 8V to 18V, Vlin 8V to 18V
Gnd disconnected, Vgnd = Vsup, VLin at -18V	Ibus no gnd	-1		1	mA	
Leakage Current to GND, Vsup Disconnected, VLin at +18V	Ibus		1	10	uA	Vsup disconnected Vlin at +18V
Lin Receiver Vil (Tx high, Rx low)	Lin-vil	0		$0.4V_{SUP}$		
Lin Receiver Vih (Tx high, Rx high)	Lin-vih	$0.6\ V_{SUP}$		V_{SUP}		
LIN Receiver Threshold center	Lin-thres	0.475	0.5	0.525	Vsup	(Lin-vih - Lin-vil) / 2
LIN Receiver Input Hysteresis	LIN hyst			0.175	Vsup	Lin-vih - Lin-vil
LIN wake up threshold	LIN wu		0.5		Vsup	

LIN physical layer: bus driver timing characteristics for normal slew rate (note 1)

Dominant propagation delay Tx to LIN	tdom min			50	us	Measurement threshold 58.1% Vsup
Dominant propagation delay Tx to LIN	tdom max			50	us	Measurement threshold 28.4% Vsup
Recessive propagation delay Tx to LIN	trec min			50	us	Measurement threshold 42.2% Vsup
Recessive propagation delay Tx to LIN	trec max			50	us	Measurement threshold 74.4% Vsup
Prop delay symmetry: tdom min - trec max	dt1	-10.44		-	us	

Prop delay symmetry: tdom max - trec min	dt2	-		11	us	

note 1: Vsup from 7V to 18V, bus load R0 and C0 1nF/1k, 6.8nF/660, 10nF/500. Measurement thresholds: 50% of Tx signal to LIN signal threshold defined in the column “condition”

LIN physical layer: bus driver timing characteristics for slow slew rate (note 1)						
Dominant propagation delay Tx to LIN	tdom min			100	us	Measurement threshold 61.6% Vsup
Dominant propagation delay Tx to LIN	tdom max			100	us	Measurement threshold 25.1% Vsup
Recessive propagation delay Tx to LIN	trec min			100	us	Measurement threshold 38.9% Vsup
Recessive propagation delay Tx to LIN	trec max			100	us	Measurement threshold 77.8% Vsup
Prop delay symmetry: tdom min - trec max	dt1s	-22		-	us	
Prop delay symmetry: tdom max - trec min	dt2s	-		23	us	

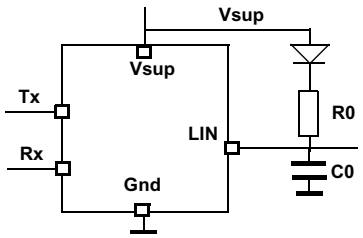
note 1: Vsup from 7V to 18V, bus load R0 and C0 1nF/1k, 6.8nF/660, 10nF/500. Measurement thresholds: 50% of Tx signal to LIN signal threshold defined in the column “condition”

LIN physical layer: bus driver fast slew rate						
LIN high slew rate (programming mode)	Dv/Dt fast		13		V/us	Fast slew rate

LIN physical layer: receiver characteristics and wake up timings						
Receiver dominant propagation delay	TrL		3.5	6	us	LIN low to Rx low. Note 2
Receiver recessive propagation delay	TrH		3.5	6	us	LIN high to Rx high. note 2
Receiver prop delay symmetry	Tr-sym	-2		2	us	TrL - TrH
Bus wake up deglitcher	TpropWL	30	70	90	us	Sleep and stop mode
Bus wake up event reported	Twake		20		us	Note 3

note 2: Measured between LIN signal threshold “Lin-vil” or “Lin-vih” and 50% of Rx signal.
note 3: Twake is typically 2 internal clock cycles after LIN rising edge detected. Ref to “LIN bus wake up behavior” figure. In sleep mode the Vdd rise time is strongly dependant upon the decoupling capacitor at Vdd pin.

Figure 3. Test circuit for timing measurements



R0 and C0: 1k/1nF, 660ohms/6.8nF and 500ohms/10nF

Figure 4. timing measurements for normal slew rate

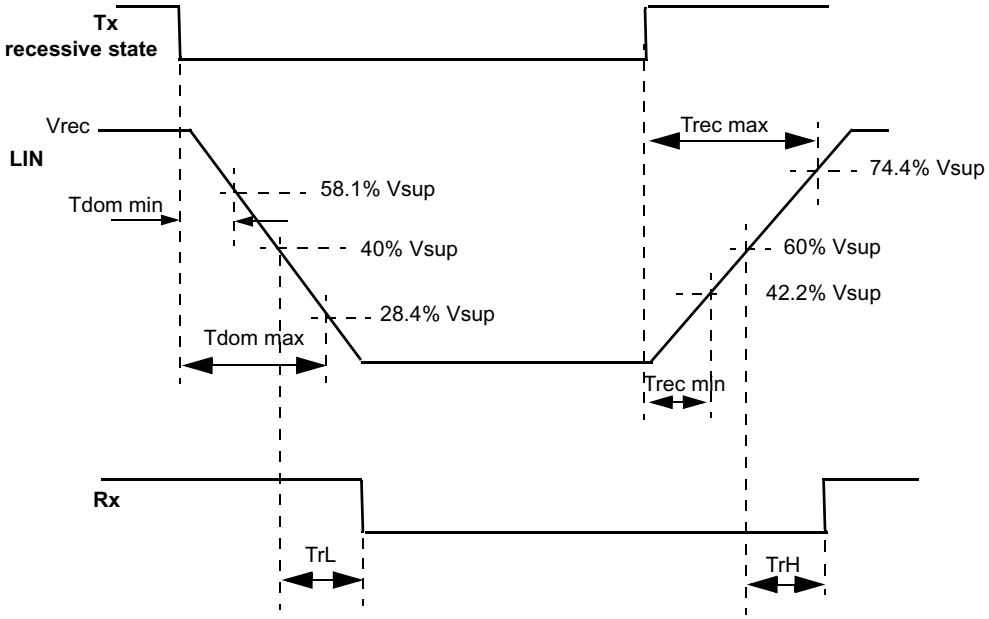


Figure 5. timing measurements for slow slew rate

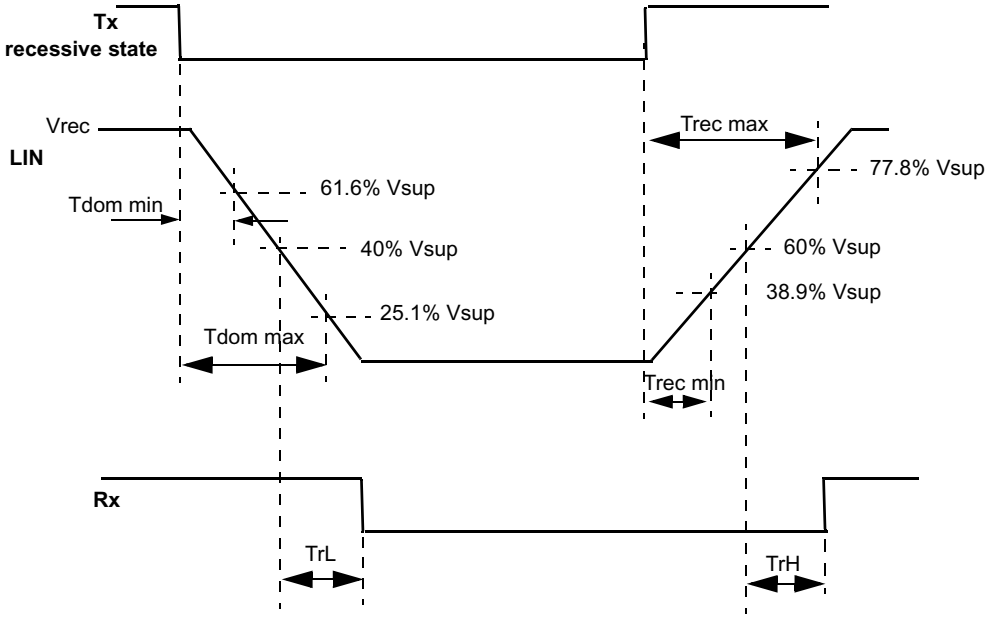
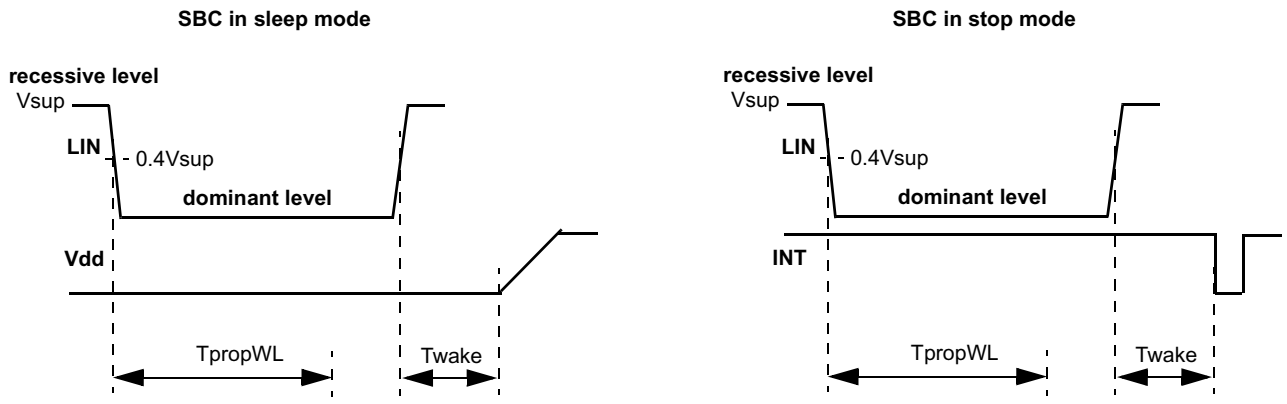
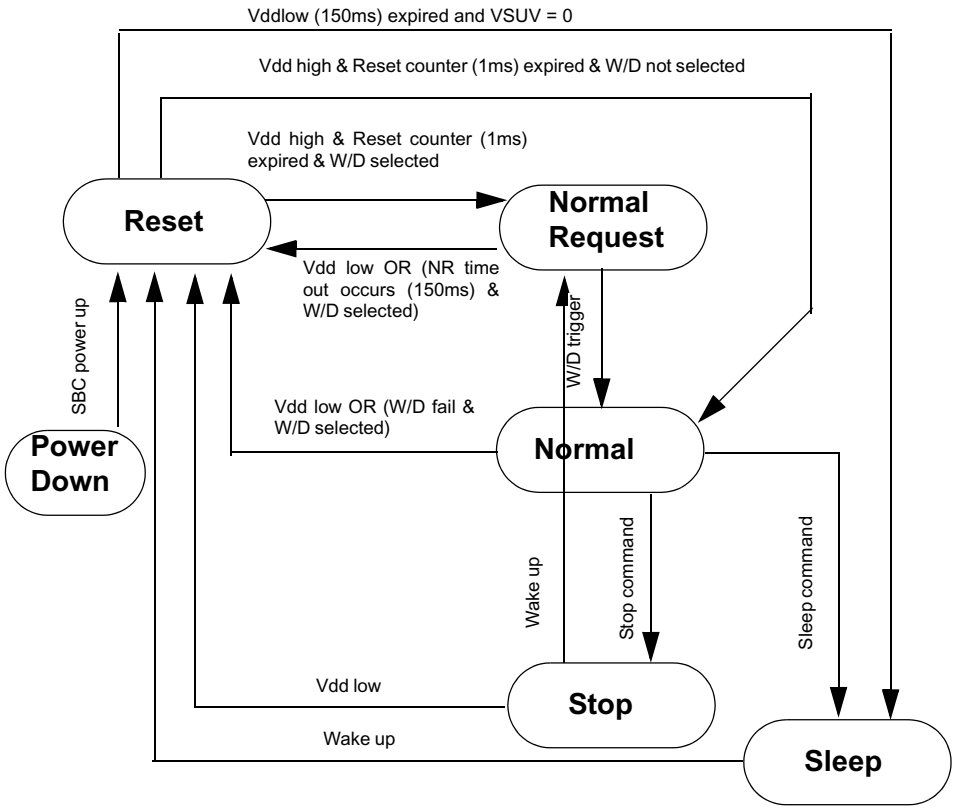


Figure 6. LIN bus wake up behavior



3 STATE MACHINE



W/D selected means: external resistor between Wdc pin and gnd or Wdc pin open.
W/D not selected means Wdc pin connected to gnd.
W/D fail means: W/D trigger occurs in closed window or no SPI W/D trigger command.
Stop command means: SPI stop command.
Sleep command means: SPI sleep request followed by SPI sleep command.
Wake up means: L1 or L2 state change or LIN bus wake up or CSB rising edge.

4 PIN DESCRIPTION

pin name	Pin number	function
Vs1	13	Power supply pin. Supply for the voltage regulator and the internal logic.
Vs2	10	Power supply pin. Supply for the high side switches.
GND	12	Electrical ground pin pins for the device.
aGND	16	Analog ground pin for voltage regulator and sense amplifier.
T-GND	8,9,24,25	Thermal ground pins for the device
Vdd	15	5V regulator output.
Reset	22	Reset output
Wdc	21	Configuration pin for the watchdog. A resistor is connected to this pin.The resistor value defines the watchdog period. If the pin is open, the W/D period is fixed (default value). If this pin is tied to gnd the watchdog is disabled.
Tx	32	Transmitter input of the LIN interface
Rx	31	Receiver output of the LIN interface
LIN	11	LIN bus line
HS1, HS2, HS3	7,6,5	High side driver output 1, output 2 and output 3
L1, L2	2,4	Wake input 1, wake up input 2
Vcc	17	5V supply input of operational amplifier
E-	19	Inverted input of the sense amplifier
E+	20	Non inverted input of the sense amplifier
Out	18	Output of the sense amplifier
MOSI	27	SPI: Master Out Slave In pin
MISO	28	SPI: Master In Slave Out
SCLK	26	SPI: Clock input pin
CSB	29	SPI: Device chip select pin
INT	30	Interrupt output pin AND wake up event signalling in stop mode.
IN	23	Direct input for PWM control of High Side switches 1 and 2

Table 4-1.

5 GENERAL DESCRIPTION

The LIN SBC is an integrated circuit dedicated to automotive applications. It includes the following functions:

- One full protected voltage regulator with 50mA total output current capability available at Vdd external pin, with under voltage reset function.
- Programmable window watchdog function, INT output
- Wake up from Lx wake input and LIN bus
- LIN physical interface
- Two 150mA high side protected switches PWM capable for relay or lamp drive
- One 50mA high side protected switch for hall sensor or
- Current sense op amp

5.1 Device Supply

The device is supplied from the battery line through the Vs1 and VS2 pins. An external diode is required to protect against negative transients and reverse battery. It can operate from 4.5V and under the jump start condition at 27V DC. Device functionality is guaranteed down to 4.5V at VS1 and VS2 pins. This pin sustains standard automotive voltage conditions such as load dump at 40V.

5.2 Over and under voltage warning.

If the voltage at VS1 exceed 20V typical or falls below 6V typical, the device generates an INT. VSOV or VSUV bits are set in the SPI register. Information is latched until the bit is read AND the fault has disappeared. The interrupt is not maskable.

5.3 LIN physical interface:

The device contains an integrated LIN physical interface.

5.4 L1 and L2 inputs:

These pins are used to sense external switches and to wake up the device from sleep or stop mode. During normal mode the state of these pins can be read through SPI.

5.5 HS1 and HS2:

These are two high side switches to drive load such as relays or lamps. They are protected against over current and over temperature and include internal clamp circuitry for inductive load drive. Control is done through SPI. PWM capability is offered through the IN input.

If PWM control is required, the internal circuitry which drive the internal high side switch is an AND function between the SPI bit HS1 (or HS2) and the IN input. In order to have HS1 on, bit HS1 must be set and IN input must be tied to a micro controller PWM ouptut to generate the PWM control signal (HS1 on when IN is high, HS1 off when IN is low). Same for HS2 output.

If not PWM control is required, IN input must be connected to Vdd or to a high logic level, then the control of HS1 and HS2 is done through SPI only.

If over temperature occurs on any of the 3 switches, the faulty switch is turned off and latched off until HS1 (or HS2 or HS3) bit is set to 1 in the SPI register. The failure is reported through SPI by HSst bit.

5.6 HS3:

This high side switch can be used to drive small lamps, hall sensor or switch pull up resistors. Control is done through SPI

5.7 Sense amplifier:

E+, E- and OUT are the 3 terminations of the current sense amplifier. The amplifier is enable in normal mode only.

5.8 Mode of operation

Mode are controlled by the mode1 and mode 2 bits in the SPI register. 3 modes are available: sleep, stop and normal.

The operation modes and the associated functions are described in the table below.

Device Mode	Voltage Regulator	Wake up capabilities	Reset output	Watchdog function	HS1 HS2 HS3	LIN interface	Operational amplifier
Reset	Vdd: ON	N/A	Low for typ 1ms, then high (if Vdd above threshold)	Disable	OFF	Recessive only	Not active
Normal Request	Vdd: ON	N/A	- High. - Active low if Vdd under voltage occurs and if Normal Request timeout (if W/D enable)	150ms time out if W/D enabled.	ON or OFF	Transmit and Receive	Not active

Table 5-1.

Device Mode	Voltage Regulator	Wake up capabilities	Reset output	Watchdog function	HS1 HS2 HS3	LIN interface	Opera-tional amplifier
Normal	Vdd: ON	N/A	- High. - Active low if Vdd under voltage occurs or if W/D fail (if W/D enable)	Window WD if enabled.	ON or OFF	Transmit and Receive	Active
Stop	Vdd ON, limited current capability	LIN and state change on Lx inputs	- Normally high. - Active low if Vdd under voltage occurs	Disable	OFF	Recessive state with Wake capability	Not active
Sleep	Vdd OFF, (Set to 5V after wake up to enter Normal request)	LIN and state change on Lx inputs	- Low - Go to high after wake up and Vdd within spec	Disable	OFF	Recessive state with Wake capability	Not active

Table 5-1.

Sleep and stop mode enter:

To safely enter sleep or stop mode and to ensure that these modes are not entered by noise issue during SPI transmission, a dedicated sequence combining bit controlling the LIN bus and the device mode must be send twice.

Enter sleep mode: first and second SPI commands (with bit D6=1, D7=1, D5 =0 or 1, D1=0 and D0=0) 11x0_0000 must be sent.

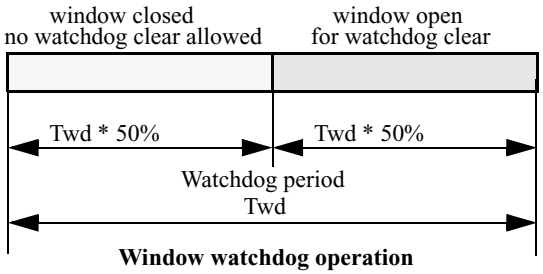
Enter stop mode: first and second SPI commands (with bit D6=1, D7=1, D5 =0 or 1, D1=0 and D0=1) 11x0_0001 must be sent.

Sleep or stop mode is entered after the second SPI command. D5 bit must be set accordingly.

5.9 Window watchdog.

The window watchdog is configurable using external resistor at Wdc pin. The W/D is cleared through mode1 and mode 2 bit is SPI register. If Wdc pin is left open a fixed watchdog period is selected (typ 150ms). If no watchdog function is required or to disable the watchdog, the Wdc pin must be connected to gnd. The watchdog period is calculated by the following formula:

Twd = 0.991 * R +0.648 (with R in kohms and Twd in ms).



Window watchdog operation

Watchdog clear:

The watchdog is cleared by SPI write command with following mode1 and mode2 bits.

Mode 2	Mode 1	Mode
0	0	Sleep mode (note 1)
0	1	Stop mode
1	0	Normal mode + W/D clear (note 2)
1	1	Normal mode

Note 1: Special SPI command and sequence is implemented in order to avoid to go into sleep or stop mode with a single 8 bit SPI command.

Note 2: When a zero is written to “Mode1” bit while “Mode2” bit is written as a one, after the SPI command is completed “Mode1” bit is set to one and SBC stays in normal mode. In order to set the SBC in sleep mode, both “Mode1” and “Mode2” bits must be written in the same 8 bits SPI command.

The W/D clear on normal request mode (150ms) has no window.

5.10 INT pin:

This pin is used to report fault to the MCU. Int pulse is generated in case of:

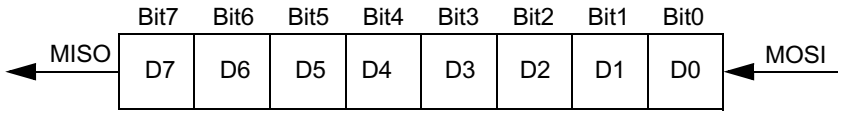
- Vdd regulator temperature pre warning
- high side switch 1, 2 or 3 thermal shutdown
- Vsup over voltage (20V typ)
- Vsup under voltage (6V typ).

If an INT is generated, when the next SPI read operation is performed bit D7 is set to 1. This mean that the bits (D6 to D0) report the interrupt source.

In case of wake up from stop mode, INT is set low in order to signal to the MCU wake up event from L1, L2 or LIN bus.

6 SPI INTERFACE AND REGISTER DESCRIPTION

6.1 Data format description



The SPI is an 8 bits SPI. All bits are data bytes. The MSB is send first. The minimum time between two rising edges on the CSB pin is 15us.

During an SPI communication the state of MISO reports the state of the SBC, at time of CSB high to low transitions. The status flag are latched at CSB high to low transitions.

Following tables describe the SPI register bit meaning, “reset value” and “bit reset condition”.

		D7	D6	D5	D4	D3	D2	D1	D0
	W	LINSL2	LINSL1	LIN-PU	HS3	HS2	HS1	Mode2	Mode1
	R	INT source	LINWU or LINFAIL	VSOV	VSUV BATFAIL (note1)	VddT	HSst	L2	L1
Write Reset value		0	0	0	0	0	0	-	-
Write Reset condition		POR, RESET	POR, RESET	POR	POR, RESET	POR, RESET	POR, RESET		

Note 1: The first SPI read, after reset, returns the BATFAIL flag state on bit D4.

D7 signals INT source. After INT occur, D7 read as a “1” means other bits report the INT source. D7 read as a “0” mean no INT occurred and other bit report real time status.

6.2 Write control bits:

6.2.1 Mode control bits:

Mode 2	Mode 1	Description
0	0	Sleep mode
0	1	Stop mode
1	0	Normal mode + W/D clear
1	1	Normal mode

6.2.2 High side switches control bits:

HS1	Description	HS2	Description	HS3	Description
0	HS1 off	0	HS2 off	0	HS3 off
1	HS1 on (if IN = 1)	1	HS2 on (if IN = 1)	1	HS3 on

6.2.3 LIN pull up termination control bits:

LIN-PU	Description
0	30k pull up connected in sleep and stop mode
1	30k pull up disconnected in sleep and stop mode

6.2.4 LIN slew rate control and device low power mode pre selection:

LINSL2	LINSL1	Description
0	0	Lin slew rate normal (baud rate up to 20kb/s)
0	1	Lin slew rate slow (baud rate up to 10kb/s)
1	0	Lin slew rate fast (for program download, baud rate up to 100kb/s)
1	1	Low power mode (sleep or stop mode) request, no change in LIN slew rate

6.3 Read control bits:

6.3.1 Switch input wake up and real time status:

L2	Description	L1	Description
0	L2 input low	0	L1 input low
1	L2 input high or wake up by L2 (first register read after wake up)	1	L1 input high or wake up by L1 (first register read after wake up)

6.3.2 High side switch, voltage regulator and device supply status

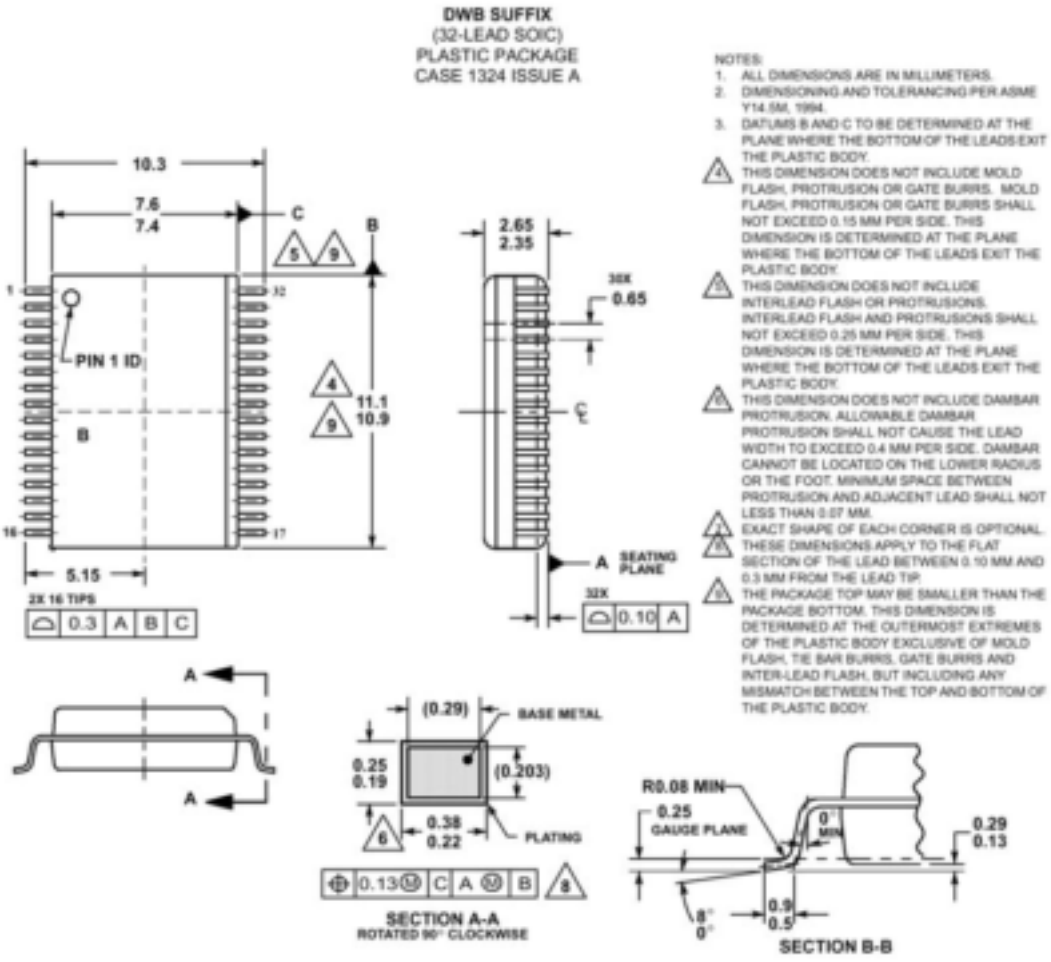
HSst	Description	VddT	Description	VSUV BATFAIL	Description	VSOV	Description
0	HS no over temp	0	No over temperature	0	Vsup above 6V	0	Vsup below 19V
1	HS1,2 or 3 OFF (over temp)	1	Vdd over temperature pre warning	1	Vsup below 6V	1	Vsup above 18V

6.3.3 LIN bus status

LINWU LINFAIL	Description
0	No LIN bus wake up of failure
1	LIN bus wake up occurred or LIN over current of over temperature

6.3.4 Interrupt status

INT mask	Description
0	SPI word read reflects the flag state
1	SPI word read reflects the interrupt or wake up source



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