



LIN System Basis Chip with High Side Drivers

The 33910G5/BAC is a Serial Peripheral Interface (SPI) controlled System Basis Chip (SBC), combining many frequently used functions in an MCU based system, plus a Local Interconnect Network (LIN) transceiver. The 33910 has a 5.0 V, 50 mA/60 mA low dropout regulator with full protection and reporting features. The device provides full SPI readable diagnostics and a selectable timing watchdog for detecting errant operation. The LIN Protocol Specification 2.0 and 2.1 compliant LIN transceiver has waveshaping circuitry that can be disabled for higher data rates.

Two 50 mA/60 mA high side switches with optional pulse-width modulated (PWM) are implemented to drive small loads. One high voltage input is available for use in contact monitoring, or as external wake-up input. This input can be used as high voltage Analog Input. The voltage on this pin is divided by a selectable ratio and available via an analog multiplexer.

The 33910 has three main operating modes: Normal (all functions available), Sleep (V_{DD} off, wake-up via LIN, wake-up inputs (L1), cyclic sense and forced wake-up), and Stop (V_{DD} on with limited current capability, wake-up via CS, LIN bus, wake-up inputs, cyclic sense, forced wake-up and external reset).

The 33910 is compatible with LIN Protocol Specification 2.0, 2.1, and SAEJ2602-2.

Features

- Full-duplex SPI interface at frequencies up to 4.0 MHz
- LIN transceiver capable of up to 100 kbps with wave shaping
- Two 50 mA/60 mA high side switches
- One high voltage analog/logic Input
- Configurable window watchdog
- 5.0 V low drop regulator with fault detection and low voltage reset (LVR) circuitry
- Switched/protected 5.0 V output (used for Hall sensors)
- Pb-free packaging designated by suffix code AC

33910

**SYSTEM BASIS CHIP WITH LIN
2ND GENERATION**



**AC SUFFIX (Pb-FREE)
98ASH70029A
32-PIN LQFP**

ORDERING INFORMATION

| Device | Temperature Range (T_A) | Package |
|----------------|-----------------------------|---------|
| MC33910G5AC/R2 | -40°C to 125°C | 32-LQFP |
| MC34910G5AC/R2 | -40°C to 85°C | |
| MC33910BAC/R2 | -40°C to 125°C | |
| MC34910BAC/R2 | -40°C to 85°C | |

* See Page 2 for Device Variations

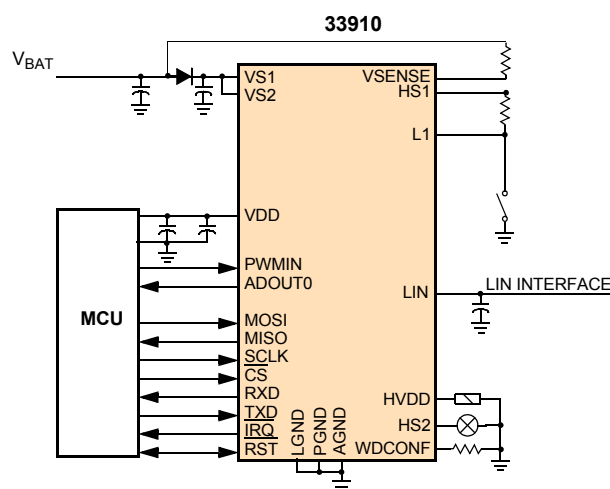


Figure 1. 33910 Simplified Application Diagram

* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

© Freescale Semiconductor, Inc., 2009 - 2010. All rights reserved.



DEVICE VARIATIONS

The 33910G5 data sheet is within [MC33910G5 Product Specifications Pages 3 to 46](#)

The 33910BAC data sheet is within [MC33911BAC Product Specifications Pages 47 to 86](#)

Table 1. This specification support the following products

| Device | Temperature | Generation | Changes |
|----------------|--------------|------------|--|
| MC33910G5AC/R2 | -40 to 125°C | 2.5 | 1. Increase ESD GUN IEC61000-4-2 (gun test contact with 150 pF, 330 Ω test conditions) performance to achieve ± 6.0 kV min on the LIN pin. 2. Immunity against ISO7637 pulse 3b 3. Reduce EMC emission level on LIN |
| MC34910G5AC/R2 | -40 to 85°C | 2.5 | 4. Improve EMC immunity against RF – target new specification including 3x68 pF 5. Comply with J2602 conformance test |
| MC33910BAC/R2 | -40 to 125°C | 2.0 | Initial release |
| MC34910BAC/R2 | -40 to 85°C | 2.0 | |

MC33910G5 PRODUCT SPECIFICATIONS PAGES 3 TO 46

INTERNAL BLOCK DIAGRAM

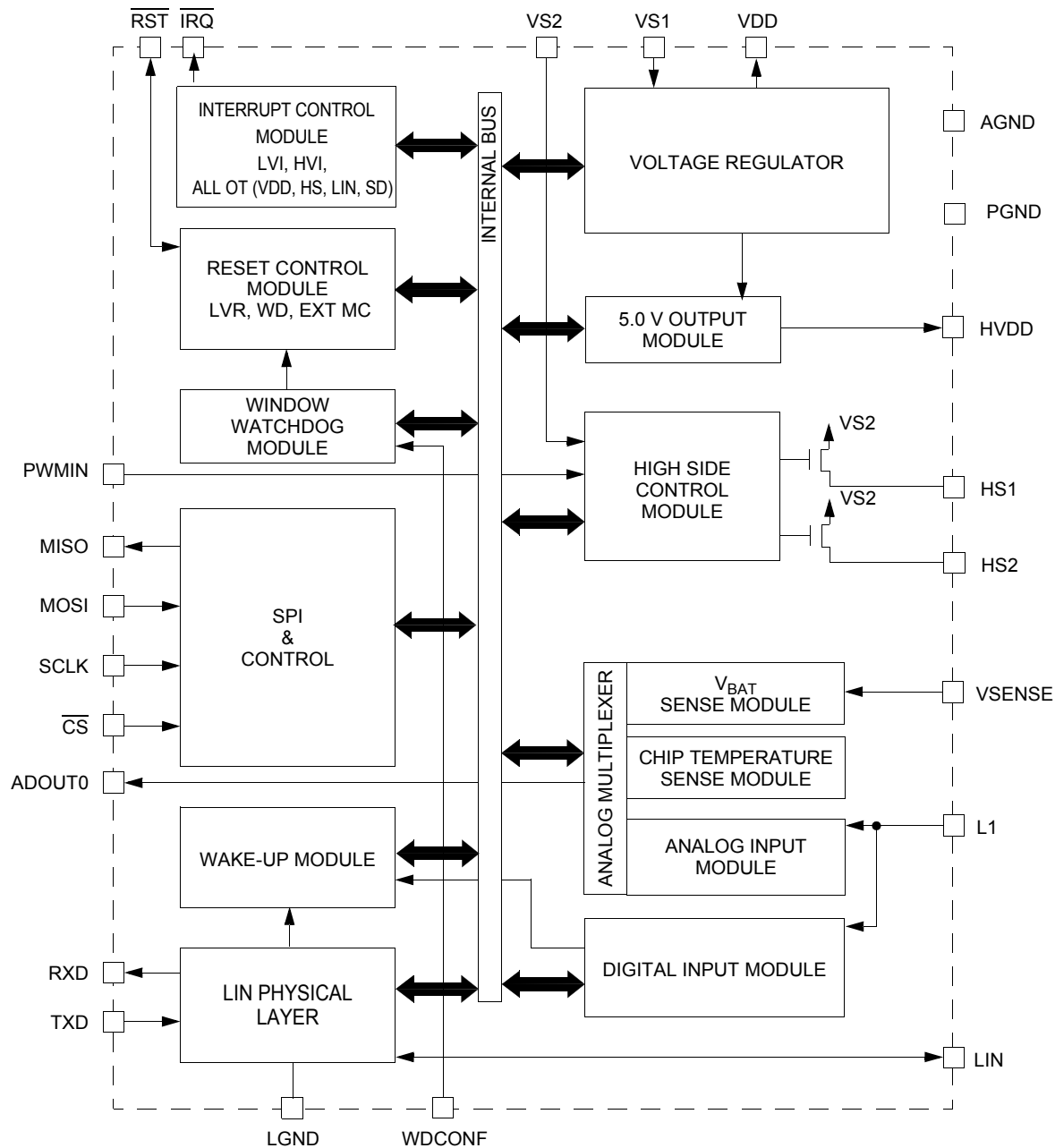
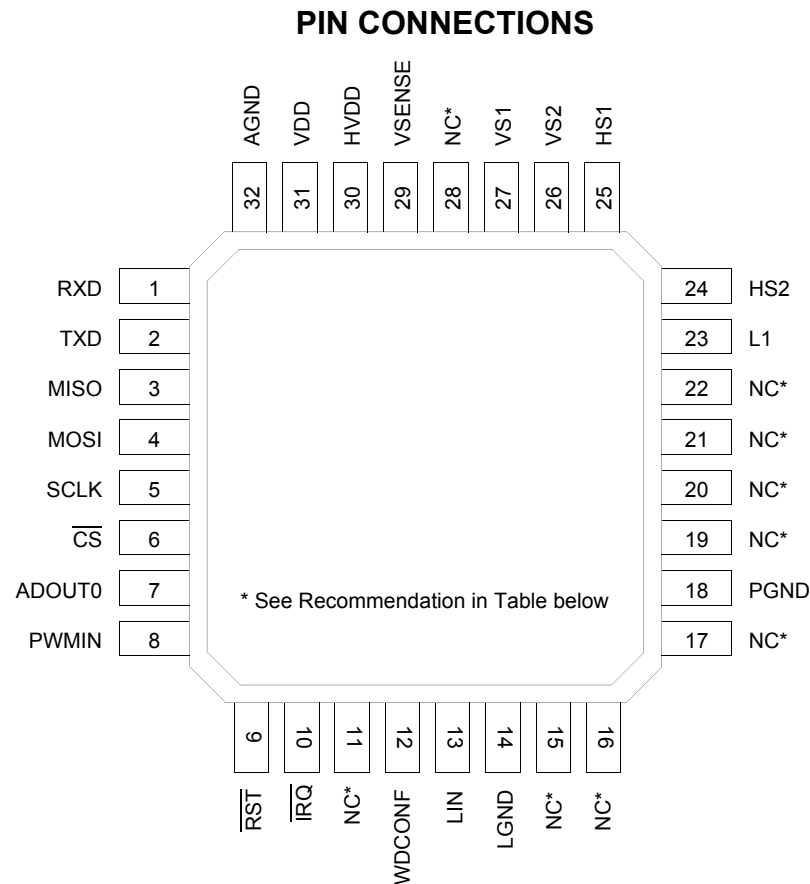


Figure 2. 33910 Simplified Internal Block Diagram

**Figure 3. 33910 Pin Connections****Table 2. 33910 Pin Definitions**

A functional description of each pin can be found in the [Functional Pin Description](#).

| Pin | Pin Name | Formal Name | Definition |
|-----|------------------|---------------------------|--|
| 1 | RXD | Receiver Output | This pin is the receiver output of the LIN interface which reports the state of the bus voltage to the MCU interface. |
| 2 | TXD | Transmitter Input | This pin is the transmitter input of the LIN interface which controls the state of the bus output. |
| 3 | MISO | SPI Output | SPI (Serial Peripheral Interface) data output. When \overline{CS} is high, pin is in the high-impedance state. |
| 4 | MOSI | SPI Input | SPI (Serial Peripheral Interface) data input. |
| 5 | SCLK | SPI Clock | SPI (Serial Peripheral Interface) clock Input. |
| 6 | \overline{CS} | SPI Chip Select | SPI (Serial Peripheral Interface) chip select input pin. \overline{CS} is active low. |
| 7 | ADOUT0 | Analog Output Pin 0 | Analog Multiplexer Output. |
| 8 | PWMIN | PWM Input | High Side Pulse Width Modulation Input. |
| 9 | \overline{RST} | Internal Reset I/O | Bidirectional Reset I/O pin - driven low when any internal reset source is asserted. \overline{RST} is active low. |
| 10 | \overline{IRQ} | Internal Interrupt Output | Interrupt output pin, indicating wake-up events from Stop modemode or events from Normal and Normal request modes. \overline{IRQ} is active low. |
| 11 | NC | Not Connected | This pin must not be connected. |

Table 2. 33910 Pin Definitions

A functional description of each pin can be found in the [Functional Pin Description](#).

| Pin | Pin Name | Formal Name | Definition |
|-----------------------------|------------|----------------------------|---|
| 12 | WDCONF | Watchdog Configuration Pin | This input pin is for configuration of the watchdog period and allows the disabling of the watchdog. |
| 13 | LIN | LIN Bus | This pin represents the single-wire bus transmitter and receiver. |
| 14 | LGND | LIN Ground Pin | This pin is the device LIN ground connection. It is internally connected to the PGND pin. |
| 15, 16, 17, 19, 20, 21 & 22 | NC | Not Connected | This pin must not be connected or connected to ground. |
| 18 | PGND | Power Ground Pin | This pin is the device low side ground connection. It is internally connected to the LGND pin. |
| 23 | L1 | Wake-up Input | This pin is the wake-up capable digital input ⁽¹⁾ . In addition, L1 input can be sensed analog via the analog multiplexer. |
| 24 25 | HS2 HS1 | High Side Outputs | High side switch outputs. |
| 26 27 | VS2 VS1 | Power Supply Pin | These pins are device battery level power supply pins. VS2 is supplying the HSx drivers while VS1 supplies the remaining blocks. ⁽²⁾ |
| 28 | NC | Not Connected | This pin can be left opening or connected to any potential ground or power supply |
| 29 | VSENSE | Voltage Sense Pin | Battery voltage sense input. ⁽³⁾ |
| 30 | HVDD | Hall Sensor Supply Output | +5.0 V switchable supply output pin. ⁽⁴⁾ |
| 31 | VDD | Voltage Regulator Output | +5.0 V main voltage regulator output pin. ⁽⁵⁾ |
| 32 | AGND | Analog Ground Pin | This pin is the device analog ground connection. |

Notes

1. When used as digital input, a series 33 k Ω resistor must be used to protect against automotive transients.
2. Reverse battery protection series diodes must be used externally to protect the internal circuitry.
3. This pin can be connected directly to the battery line for voltage measurements. The pin is self protected against reverse battery connections. It is strongly recommended to connect a 10 k Ω resistor in series with this pin for protection purposes.
4. External capacitor (1.0 μ F < C < 10 μ F; 0.1 Ω < ESR < 5.0 Ω) required.
5. External capacitor (2.0 μ F < C < 100 μ F; 0.1 Ω < ESR < 10 Ω) required.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings | Symbol | Value | Unit |
|---|--------------------------------|--------------------------------------|------|
| ELECTRICAL RATINGS | | | |
| Supply Voltage at VS1 and VS2 Normal Operation (DC) Transient Conditions (load dump) | $V_{SUP(SS)}$ $V_{SUP(PK)}$ | -0.3 to 27 -0.3 to 40 | V |
| Supply Voltage at VDD | V_{DD} | -0.3 to 5.5 | V |
| Input / Output Pins Voltage ⁽⁶⁾ \overline{CS} , \overline{RST} , SCLK, PWMIN, ADOUT0, MOSI, MISO, TXD, RXD, HVDD Interrupt Pin (\overline{IRQ}) ⁽⁷⁾ | V_{IN} $V_{IN(IRQ)}$ | -0.3 to $V_{DD} + 0.3$ -0.3 to 11 | V |
| HS1 and HS2 Pin Voltage (DC) | V_{HS} | -0.3 to $V_{SUP} + 0.3$ | V |
| L1 Pin Voltage Normal Operation with a series 33k resistor (DC) Transient input voltage with external component (according to ISO7637-2) (See Figure .) | V_{L1DC} V_{L1TR} | -18 to 40 ± 100 | V |
| VSENSE Pin Voltage (DC) | V_{VSENSE} | -27 to 40 | V |
| LIN Pin Voltage Normal Operation (DC) Transient input voltage with external component (according to ISO7637-2) (See Figure .) | V_{BUSDC} V_{BUSTR} | -18 to 40 -150 to 100 | V |
| VDD Output Current | I_{VDD} | Internally Limited | A |

Notes

- Exceeding voltage limits on specified pins may cause a malfunction or permanent damage to the device.
- Extended voltage range for programming purpose only.

ELECTRICAL CHARACTERISTICS
MAXIMUM RATINGS**Table 3. Maximum Ratings (continued)**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings | Symbol | Value | Unit |
|---|--------------|-------------|------|
| ESD Capability | | | V |
| AECQ100 | | | |
| Human Body Model - JESD22/A114 ($C_{ZAP} = 100 \text{ pF}$, $R_{ZAP} = 1500 \Omega$) | | | |
| LIN Pin | V_{ESD1-1} | $\pm 8.0k$ | |
| L1 | V_{ESD1-2} | $\pm 6.0k$ | |
| all other Pins | V_{ESD1-3} | ± 2000 | |
| Charge Device Model - JESD22/C101 ($C_{ZAP} = 4.0 \text{ pF}$) | | | |
| Corner Pins (Pins 1, 8, 9, 16, 17, 24, 25 and 32) | V_{ESD2-1} | ± 750 | |
| All other Pins (Pins 2-7, 10-15, 18-23, 26-31) | V_{ESD2-2} | ± 500 | |
| According to LIN Conformance Test Specification / LIN EMC Test Specification, August 2004 ($C_{ZAP} = 150 \text{ pF}$, $R_{ZAP} = 330 \Omega$) | | | |
| Contact Discharge, Unpowered | | | |
| LIN pin with 220 pF | V_{ESD3-1} | $\pm 20k$ | |
| LIN pin without capacitor | V_{ESD3-2} | $\pm 11k$ | |
| VS1/VS2 (100 nF to ground) | V_{ESD3-3} | $> \pm 12k$ | |
| L1 input (33 k Ω serial resistor) | V_{ESD3-4} | ± 6000 | |
| According to IEC 61000-4-2 ($C_{ZAP} = 150 \text{ pF}$, $R_{ZAP} = 330 \Omega$) | | | |
| Unpowered | | | |
| LIN pin with 220 pF and without capacitor | V_{ESD4-1} | ± 8000 | |
| VS1/VS2 (100 nF to ground) | V_{ESD4-2} | ± 8000 | |
| L1 input (33 k Ω serial resistor) | V_{ESD4-3} | ± 8000 | |

THERMAL RATINGS

| | | | |
|---|-----------------|------------|----------------------|
| Operating Ambient Temperature ⁽⁸⁾ | T_A | | $^{\circ}\text{C}$ |
| 33910 | | -40 to 125 | |
| 34910 | | -40 to 85 | |
| Operating Junction Temperature | T_J | -40 to 150 | $^{\circ}\text{C}$ |
| Storage Temperature | T_{STG} | -55 to 150 | $^{\circ}\text{C}$ |
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | | $^{\circ}\text{C/W}$ |
| Natural Convection, Single Layer board (1s) ^{(8), (9)} | | 85 | |
| Natural Convection, Four Layer board (2s2p) ^{(8), (10)} | | 56 | |
| Thermal Resistance, Junction to Case ⁽¹¹⁾ | $R_{\theta JC}$ | 23 | $^{\circ}\text{C/W}$ |
| Peak Package Reflow Temperature During Reflow ^{(12), (13)} | T_{PPRT} | Note 13 | $^{\circ}\text{C}$ |

Notes

- Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
- Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the 33910 and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---------------------------|------|-------|------|---------------|
| SUPPLY VOLTAGE RANGE (VS1, VS2) | | | | | |
| Nominal Operating Voltage | V_{SUP} | 5.5 | – | 18 | V |
| Functional Operating Voltage ⁽¹⁴⁾ | V_{SUPOP} | – | – | 27 | V |
| Load Dump | V_{SUPLD} | – | – | 40 | V |
| SUPPLY CURRENT RANGE ($V_{\text{SUP}} = 13.5\text{ V}$) | | | | | |
| Normal Mode (I_{OUT} at $V_{\text{DD}} = 10\text{ mA}$), LIN Recessive State ⁽¹⁵⁾ | I_{RUN} | – | 4.5 | 10 | mA |
| Stop Mode, VDD ON with $I_{\text{OUT}} = 100\text{ }\mu\text{A}$, LIN Recessive State ^{(15), (16), (17), (18)} | I_{STOP} | | | | μA |
| 5.5 V < $V_{\text{SUP}} < 12\text{ V}$ | | – | 47 | 80 | |
| $V_{\text{SUP}} = 13.5\text{ V}$ | | – | 62 | 90 | |
| $13.5\text{ V} < V_{\text{SUP}} < 18\text{ V}$ | | – | 180 | 400 | |
| Sleep Mode, VDD OFF, LIN Recessive State ^{(15), (17)} | I_{SLEEP} | | | | μA |
| 5.5 V < $V_{\text{SUP}} < 12\text{ V}$ | | – | 27 | 35 | |
| $V_{\text{SUP}} = 13.5\text{ V}$ | | – | 33 | 48 | |
| $13.5\text{ V} \leq V_{\text{SUP}} < 18\text{ V}$ | | – | 160 | 300 | |
| Cyclic Sense Supply Current Adder ⁽¹⁹⁾ | I_{CYCLIC} | – | 10 | – | μA |
| SUPPLY UNDER/OVER-VOLTAGE DETECTIONS | | | | | |
| Power-On Reset (BATFAIL) ⁽²⁰⁾ | | | | | V |
| Threshold (measured on VS1) ⁽¹⁹⁾ | V_{BATFAIL} | 1.5 | 3.0 | 3.9 | |
| Hysteresis (measured on VS1) ⁽¹⁹⁾ | $V_{\text{BATFAIL_HYS}}$ | – | 0.9 | – | |
| V_{SUP} under-voltage detection (VSUV Flag) (Normal and Normal Request Modes, Interrupt Generated) | | | | | V |
| Threshold (measured on VS1) | V_{SUV} | 5.55 | 6.0 | 6.6 | |
| Hysteresis (measured on VS1) | $V_{\text{SUV_HYS}}$ | – | 0.2 | – | |
| V_{SUP} over-voltage detection (VSOV Flag) (Normal and Normal Request Modes, Interrupt Generated) | | | | | V |
| Threshold (measured on VS1) | V_{SOV} | 18 | 19.25 | 20.5 | |
| Hysteresis (measured on VS1) | $V_{\text{SOV_HYS}}$ | – | 1.0 | – | |

Notes

14. Device is fully functional. All features are operating.
15. Total current ($I_{\text{VS1}} + I_{\text{VS2}}$) measured at GND pins excluding all loads, cyclic sense disabled.
16. Total I_{DD} current (including loads) below $100\text{ }\mu\text{A}$.
17. Stop and Sleep modes current will increase if V_{SUP} exceeds 13.5 V .
18. This parameter is guaranteed after 90 ms.
19. This parameter is guaranteed by process monitoring but not production tested.
20. The Flag is set during power up sequence. To clear the flag, a SPI read must be performed.

ELECTRICAL CHARACTERISTICS
STATIC ELECTRICAL CHARACTERISTICS**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the 33910 and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---|--------|--------|----------|------------------|
| VOLTAGE REGULATOR⁽²¹⁾ (VDD) | | | | | |
| Normal Mode Output Voltage $1.0\text{ mA} < I_{\text{VDD}} < 50\text{ mA}$; $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | V_{DDRUN} | 4.75 | 5.00 | 5.25 | V |
| Normal Mode Output Current Limitation | I_{VDDRUN} | 60 | 110 | 200 | mA |
| Dropout Voltage ⁽²²⁾ $I_{\text{VDD}} = 50\text{ mA}$ | V_{DDDROP} | – | 0.1 | 0.25 | V |
| Stop Mode Output Voltage $I_{\text{VDD}} < 5.0\text{ mA}$ | V_{DDSTOP} | 4.75 | 5.0 | 5.25 | V |
| Stop Mode Output Current Limitation | I_{VDDSTOP} | 6.0 | 13 | 36 | mA |
| Line Regulation Normal mode, $5.5\text{ V} < V_{\text{SUP}} < 18\text{ V}$; $I_{\text{VDD}} = 10\text{ mA}$ Stop mode, $5.5\text{ V} < V_{\text{SUP}} < 18\text{ V}$; $I_{\text{VDD}} = 1.0\text{ mA}$ | LR_{RUN} LR_{STOP} | – – | – – | 25 25 | mV |
| Load Regulation Normal mode, $1.0\text{ mA} < I_{\text{VDD}} < 50\text{ mA}$ Stop mode, $0.1\text{ mA} < I_{\text{VDD}} < 5.0\text{ mA}$ | LD_{RUN} LD_{STOP} | – – | – – | 80 50 | mV |
| Over-temperature Prewarning (Junction) ⁽²³⁾ Interrupt generated, VDDOT Bit Set | T_{PRE} | 90 | 115 | 140 | $^\circ\text{C}$ |
| Over-temperature Prewarning Hysteresis ⁽²³⁾ | $T_{\text{PRE_HYS}}$ | – | 13 | – | $^\circ\text{C}$ |
| Over-temperature Shutdown Temperature (Junction) ⁽²³⁾ | T_{SD} | 150 | 170 | 190 | $^\circ\text{C}$ |
| Over-temperature Shutdown Hysteresis ⁽²³⁾ | $T_{\text{SD_HYS}}$ | – | 13 | – | $^\circ\text{C}$ |
| HALL SENSOR SUPPLY OUTPUT⁽²⁴⁾ (HVDD) | | | | | |
| V_{DD} Voltage matching $H_{\text{VDDACC}} = (HVDD - VDD) / VDD * 100\%$ $I_{\text{HVDD}} = 15\text{ mA}$ | H_{VDDACC} | -2.0 | – | 2.0 | % |
| Current Limitation | I_{HVDD} | 20 | 35 | 50 | mA |
| Dropout Voltage $I_{\text{HVDD}} = 15\text{ mA}$; $I_{\text{VDD}} = 5.0\text{ mA}$ | H_{VDDDROP} | – | 160 | 300 | mV |
| Line Regulation $I_{\text{HVDD}} = 5.0\text{ mA}$; $I_{\text{VDD}} = 5.0\text{ mA}$ | LR_{HVDD} | – | – | 40 | mV |
| Load Regulation $1.0\text{ mA} > I_{\text{HVDD}} > 15\text{ mA}$; $I_{\text{VDD}} = 5.0\text{ mA}$ | LD_{HVDD} | – | – | 20 | mV |

Notes

21. Specification with external capacitor $2.0\text{ }\mu\text{F} < C < 100\text{ }\mu\text{F}$ and $100\text{ m}\Omega \leq \text{ESR} \leq 10\text{ }\Omega$.
22. Measured when voltage has dropped 250 mV below its nominal Value (5.0 V).
23. This parameter is guaranteed by process monitoring but not production tested.
24. Specification with external capacitor $1.0\text{ }\mu\text{F} < C < 10\text{ }\mu\text{F}$ and $100\text{ m}\Omega \leq \text{ESR} \leq 10\text{ }\Omega$.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the 33910 and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|----------------------|----------------------------|------|----------------------------|---------------|
| RST INPUT/OUTPUT PIN (RST) | | | | | |
| VDD Low Voltage Reset Threshold | V_{RSTTH} | 4.3 | 4.5 | 4.7 | V |
| Low-state Output Voltage $I_{\text{OUT}} = 1.5\text{ mA}$; $3.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$ | V_{OL} | 0.0 | – | 0.9 | V |
| High-state Output Current ($0\text{ V} < V_{\text{OUT}} < 3.5\text{ V}$) | I_{OH} | -150 | -250 | -350 | μA |
| Pull-down Current Limitation (internally limited) $V_{\text{OUT}} = V_{\text{DD}}$ | $I_{\text{PD_MAX}}$ | 1.5 | – | 8.0 | mA |
| Low-state Input Voltage | V_{IL} | -0.3 | – | $0.3 \times V_{\text{DD}}$ | V |
| High-state Input Voltage | V_{IH} | $0.7 \times V_{\text{DD}}$ | – | $V_{\text{DD}} + 0.3$ | V |
| MISO SPI OUTPUT PIN (MISO) | | | | | |
| Low-state Output Voltage $I_{\text{OUT}} = 1.5\text{ mA}$ | V_{OL} | 0.0 | – | 1.0 | V |
| High-state Output Voltage $I_{\text{OUT}} = -250\text{ }\mu\text{A}$ | V_{OH} | $V_{\text{DD}} - 0.9$ | – | V_{DD} | V |
| Tri-state Leakage Current $0\text{ V} \leq V_{\text{MISO}} \leq V_{\text{DD}}$ | I_{TRIMISO} | -10 | – | 10 | μA |
| SPI INPUT PINS (MOSI, SCLK, $\overline{\text{CS}}$) | | | | | |
| Low-state Input Voltage | V_{IL} | -0.3 | – | $0.3 \times V_{\text{DD}}$ | V |
| High-state Input Voltage | V_{IH} | $0.7 \times V_{\text{DD}}$ | – | $V_{\text{DD}} + 0.3$ | V |
| MOSI, SCLK Input Current $0\text{ V} \leq V_{\text{IN}} \leq V_{\text{DD}}$ | I_{IN} | -10 | – | 10 | μA |
| $\overline{\text{CS}}$ Pull-up Current $0\text{ V} < V_{\text{IN}} < 3.5\text{ V}$ | I_{PUCS} | 10 | 20 | 30 | μA |
| INTERRUPT OUTPUT PIN ($\overline{\text{IRQ}}$) | | | | | |
| Low-state Output Voltage $I_{\text{OUT}} = 1.5\text{ mA}$ | V_{OL} | 0.0 | – | 0.8 | V |
| High-state Output Voltage $I_{\text{OUT}} = -250\text{ }\mu\text{A}$ | V_{OH} | $V_{\text{DD}} - 0.8$ | – | V_{DD} | V |
| Leakage Current $V_{\text{DD}} \leq V_{\text{OUT}} \leq 10\text{ V}$ | I_{OUT} | – | – | 2.0 | mA |
| PULSE WIDTH MODULATION INPUT PIN (PWMIN) | | | | | |
| Low-state Input Voltage | V_{IL} | -0.3 | – | $0.3 \times V_{\text{DD}}$ | V |
| High-state Input Voltage | V_{IH} | $0.7 \times V_{\text{DD}}$ | – | $V_{\text{DD}} + 0.3$ | V |
| Pull-up current $0\text{ V} < V_{\text{IN}} < 3.5\text{ V}$ | I_{PUPWMIN} | 10 | 20 | 30 | μA |

ELECTRICAL CHARACTERISTICS
STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the 33910 and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|------------------------|------------------------|-----|-----------------|------------------|
| HIGH SIDE OUTPUTS HS1 AND HS2 PINS (HS1, HS2) | | | | | |
| Output Drain-to-Source On Resistance $T_J = 25^\circ\text{C}$, $I_{\text{LOAD}} = 50\text{ mA}$; $V_{\text{SUP}} > 9.0\text{ V}$ $T_J = 150^\circ\text{C}$, $I_{\text{LOAD}} = 50\text{ mA}$; $V_{\text{SUP}} > 9.0\text{ V}$ ⁽²⁵⁾ $T_J = 150^\circ\text{C}$, $I_{\text{LOAD}} = 30\text{ mA}$; $5.5\text{ V} < V_{\text{SUP}} < 9.0\text{ V}$ ⁽²⁵⁾ | $R_{\text{DS(ON)}}$ | – | – | 7.0 10 14 | Ω |
| Output Current Limitation ⁽²⁶⁾ $0\text{ V} < V_{\text{OUT}} < V_{\text{SUP}} - 2.0\text{ V}$ | I_{LIMHSX} | 60 | 90 | 250 | mA |
| Open Load Current Detection ⁽²⁷⁾ | I_{OLHSX} | – | 5.0 | 7.5 | mA |
| Leakage Current $-0.2\text{ V} < V_{\text{HSX}} < V_{\text{S2}} + 0.2\text{ V}$ | I_{LEAK} | – | – | 10 | μA |
| Short-circuit Detection Threshold ⁽²⁸⁾ $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | V_{THSC} | $V_{\text{SUP}} - 2.0$ | – | – | V |
| Over-temperature Shutdown ^{(29), (30)} | T_{HSSD} | 140 | 160 | 180 | $^\circ\text{C}$ |
| Over-temperature Shutdown Hysteresis ⁽³⁰⁾ | $T_{\text{HSSD_HYS}}$ | – | 10 | – | $^\circ\text{C}$ |

L1 INPUT PIN (L1)

| | | | | | |
|---|--|--------------|------------|--------------|------------------|
| Low Detection Threshold ⁽³¹⁾ $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | V_{THL} | 2.0 | 2.5 | 3.0 | V |
| High Detection Threshold ⁽³¹⁾ $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | V_{THH} | 3.0 | 3.5 | 4.0 | V |
| Hysteresis ⁽³¹⁾ $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | V_{HYS} | 0.4 | 0.8 | 1.4 | V |
| Input Current ⁽³²⁾ $-0.2\text{ V} < V_{\text{IN}} < V_{\text{S1}}$ | I_{IN} | -10 | – | 10 | μA |
| Analog Input Impedance ⁽³³⁾ | R_{L1IN} | 800 | 1300 | 2000 | $\text{k}\Omega$ |
| Analog Input Divider Ratio ($\text{RATIO}_{\text{L1}} = V_{\text{L1}} / V_{\text{ADOUT0}}$) L1DS (L1 Divider Select) = 0 L1DS (L1 Divider Select) = 1 | RATIO_{L1} | 0.95 3.42 | 1.0 3.6 | 1.05 3.78 | |
| Analog Output offset Ratio L1DS (L1 Divider Select) = 0 L1DS (L1 Divider Select) = 1 | $V_{\text{RATIO}_{\text{L1}}\text{-OFFSET}}$ | -80 -22 | 6.0 2.0 | 80 22 | mV |
| Analog Inputs Matching L1DS (L1 Divider Select) = 0 L1DS (L1 Divider Select) = 1 | $L1_{\text{MATCHING}}$ | 96 96 | 100 100 | 104 104 | % |

Notes

25. This parameter is production tested up to $T_A = 125^\circ\text{C}$, and guaranteed by process monitoring up to $T_J = 150^\circ\text{C}$.
26. When over-current occurs, the corresponding high side stays ON with limited current capability and the HSxCL flag is set in the HSSR.
27. When open load occurs, the flag (HSxOP) is set in the HSSR.
28. HS automatically shutdown if HSOT occurs or if the HVSE flag is enabled and an over-voltage occurs.
29. When over-temperature shutdown occurs, both high sides are turned off. All flags in HSSR are set.
30. Guaranteed by characterization but not production tested
31. If L1 pin is unused it must be connected to ground.
32. Analog multiplexer input disconnected from L1 input pin.
33. Analog multiplexer input connected to L1 input pin.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the 33910 and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-------------------|-----|-----|-----|------------------|
| WINDOW WATCHDOG CONFIGURATION PIN (WDCONF)⁽³⁴⁾ | | | | | |
| External Resistor Range | R_{EXT} | 20 | – | 200 | $\text{k}\Omega$ |
| Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy) ⁽³⁵⁾ | WD_{ACC} | -15 | – | 15 | % |

ANALOG MULTIPLEXER

| | | | | | |
|---|-------------------------------------|-------------------|----------|-------------------|------|
| Temperature Sense Analog Output Voltage $T_A = -40^\circ\text{C}$ $T_A = 25^\circ\text{C}$ $T_A = 125^\circ\text{C}$ | $V_{\text{ADOUT0_TEMP}}$ | 2.0 2.8 3.6 | – 3.0 | 2.8 3.6 4.6 | V |
| Temperature Sense Analog Output Voltage per characterization ⁽³⁶⁾ $T_A = 25^\circ\text{C}$ | $V_{\text{ADOUT0_25}}$ | 3.1 | 3.15 | 3.2 | V |
| Internal Chip Temperature Sense Gain | S_{TTOV} | 9.0 | 10.5 | 12 | mV/K |
| Internal Chip Temperature Sense Gain per characterization at 3 temperatures ⁽³⁶⁾ See Figure 16. Temperature Sense Gain | $S_{\text{TTOV_3T}}$ | 9.9 | 10.2 | 10.5 | mV/K |
| VSENSE Input Divider Ratio ($\text{RATIO}_{\text{VSENSE}} = V_{\text{VSENSE}} / V_{\text{ADOUT0}}$) $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | $\text{RATIO}_{\text{VSENSE}}$ | 5.0 | 5.25 | 5.5 | |
| VSENSE Input Divider Ratio ($\text{RATIO}_{\text{VSENSE}} = V_{\text{sense}} / V_{\text{adout0}}$) per characterization ⁽³⁶⁾ $5.5 < V_{\text{sup}} < 27\text{ V}$ | $\text{RATIO}_{\text{VSENSE_CZ}}$ | 5.15 | 5.25 | 5.35 | |
| VSENSE Output Related Offset | $\text{OFFSET}_{\text{VSENSE}}$ | -30 | -10 | 30 | mV |
| VSENSE Output Related Offset per characterization ⁽³⁶⁾ | $\text{OFFSET}_{\text{VSENSE_CZ}}$ | -30 | -12.6 | 0 | mV |

ANALOG OUTPUT (ADOUT0)

| | | | | | |
|--|-----------------------|------------------------|---|-----------------|---|
| Maximum Output Voltage $-5.0\text{ mA} < I_O < 5.0\text{ mA}$ | $V_{\text{OUT_MAX}}$ | $V_{\text{DD}} - 0.35$ | – | V_{DD} | V |
| Minimum Output Voltage $-5.0\text{ mA} < I_O < 5.0\text{ mA}$ | $V_{\text{OUT_MIN}}$ | 0.0 | – | 0.35 | V |

RXD OUTPUT PIN (LIN PHYSICAL LAYER) (RXD)

| | | | | | |
|---|-----------------|-----------------------|---|-----------------|---|
| Low-state Output Voltage $I_{\text{OUT}} = 1.5\text{ mA}$ | V_{OL} | 0.0 | – | 0.8 | V |
| High-state Output Voltage $I_{\text{OUT}} = -250\text{ }\mu\text{A}$ | V_{OH} | $V_{\text{DD}} - 0.8$ | – | V_{DD} | V |

Notes

34. For V_{SUP} 4.7 to 18 V

35. Watchdog timing period calculation formula: $t_{\text{PWD}} [\text{ms}] = [0.466 * (R_{\text{EXT}} - 20)] + 10$ with (R_{EXT} in $\text{k}\Omega$)

36. These limits have been defined after laboratory characterization on 3 lots and 30 samples. These tighten limits could not be guaranteed by production test.

ELECTRICAL CHARACTERISTICS
STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$ for the 33910 and $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 85^{\circ}\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---------------------------------|----------------------------|-----|----------------------------|------------------|
| TXD INPUT PIN (LIN PHYSICAL LAYER) (TXD) | | | | | |
| Low-state Input Voltage | V_{IL} | -0.3 | – | $0.3 \times V_{\text{DD}}$ | V |
| High-state Input Voltage | V_{IH} | $0.7 \times V_{\text{DD}}$ | – | $V_{\text{DD}} + 0.3$ | V |
| Pin Pull-up Current, $0\text{ V} < V_{\text{IN}} < 3.5\text{ V}$ | I_{PUIN} | 10 | 20 | 30 | μA |
| LIN PHYSICAL LAYER WITH J2602 FEATURE ENABLED (BIT DIS_J2602 = 0) | | | | | |
| LIN Under Voltage threshold Positive and Negative threshold (V_{THP} , V_{THN}) | $V_{\text{TH_UNDER_VOLTAGE}}$ | 5.0 | | 6.0 | V |
| Hysteresis ($V_{\text{THP}} - V_{\text{THN}}$) | $V_{\text{J2602_DEG}}$ | | 400 | | mV |
| LIN PHYSICAL LAYER, TRANSCEIVER (LIN)⁽³⁷⁾ | | | | | |
| Operating Voltage Range | V_{BAT} | 8.0 | | 18 | V |
| Supply Voltage Range | V_{SUP} | 7.0 | | 18 | V |
| Voltage Range within which the device is not destroyed | $V_{\text{SUP_NON_OP}}$ | -0.3 | | 40 | V |
| Current Limitation for Driver Dominant State Driver ON, $V_{\text{BUS}} = 18\text{ V}$ | $I_{\text{BUS_LIM}}$ | 40 | 90 | 200 | mA |
| Input Leakage Current at the receiver Driver off; $V_{\text{BUS}} = 0\text{ V}$; $V_{\text{BAT}} = 12\text{ V}$ | $I_{\text{BUS_PAS_DOM}}$ | -1.0 | – | – | mA |
| Leakage Output Current to GND Driver Off; $8.0\text{ V} < V_{\text{BAT}} < 18\text{ V}$; $8.0\text{ V} < V_{\text{BUS}} < 18\text{ V}$; $V_{\text{BUS}} \geq V_{\text{BAT}}$ | $I_{\text{BUS_PAS_REC}}$ | – | – | 20 | μA |
| Control unit disconnected from ground ⁽³⁸⁾ $\text{GND}_{\text{DEVICE}} = V_{\text{SUP}}$; $V_{\text{BAT}} = 12\text{ V}$; $0 < V_{\text{BUS}} < 18\text{ V}$ | $I_{\text{BUS_NO_GND}}$ | -1.0 | – | 1.0 | mA |
| V_{BAT} Disconnected; $V_{\text{SUP_DEVICE}} = \text{GND}$; $0\text{ V} < V_{\text{BUS}} < 18\text{ V}$ ⁽³⁹⁾ | $I_{\text{BUSNO_BAT}}$ | – | – | 100 | μA |
| Receiver Dominant State | V_{BUSDOM} | – | – | 0.4 | V_{SUP} |
| Receiver Recessive State | V_{BUSREC} | 0.6 | – | – | V_{SUP} |
| Receiver Threshold Center ($V_{\text{TH_DOM}} + V_{\text{TH_REC}}$)/2 | $V_{\text{BUS_CNT}}$ | 0.475 | 0.5 | 0.525 | V_{SUP} |
| Receiver Threshold Hysteresis ($V_{\text{TH_REC}} - V_{\text{TH_DOM}}$) | V_{HYS} | – | – | 0.175 | V_{SUP} |
| Voltage Drop at the serial Diode in pull-up path | V_{SERDIODE} | 0.4 | | 1.0 | V |
| $V_{\text{BAT_SHIFT}}$ | $V_{\text{SHIFT_BAT}}$ | 0 | | 11.5% | V_{BAT} |
| GND_SHIFT | $V_{\text{SHIFT_GND}}$ | 0 | | 11.5% | V_{BAT} |

Notes

37. Parameters guaranteed for $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$.
 38. Loss of local ground must not affect communication in the residual network.
 39. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$ for the 33910 and $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 85^{\circ}\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|--------------------------|-----|-----|-----|--------------------|
| LIN PHYSICAL LAYER, TRANSCEIVER (LIN) (CONTINUED) ⁽³⁷⁾ | | | | | |
| LIN Wake-up threshold from Stop or Sleep Mode ⁽⁴⁰⁾ | V_{BUSWU} | | 5.3 | 5.8 | V |
| LIN Pull-up Resistor to V_{SUP} | R_{SLAVE} | 20 | 30 | 60 | $\text{k}\Omega$ |
| Over-temperature Shutdown ⁽⁴¹⁾ | $T_{\text{LINS D}}$ | 140 | 160 | 180 | $^{\circ}\text{C}$ |
| Over-temperature Shutdown Hysteresis | $T_{\text{LINS D_HYS}}$ | – | 10 | – | $^{\circ}\text{C}$ |

Notes

40. This parameter is 100% tested on an Automatic Tester. However, since it has not been monitored during reliability stresses, Freescale does not guarantee this parameter during the product's life time.
41. When over-temperature shutdown occurs, the LIN bus goes in recessive state and the flag LINOT in LINSR is set.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$ for the 33910 and $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 85^{\circ}\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|------------------|-----------------|--------------------|------|
| SPI INTERFACE TIMING (SEE Figure 13) | | | | | |
| SPI Operating Frequency | f_{SPIOP} | – | – | 4.0 | MHz |
| SCLK Clock Period | t_{PSCLK} | 250 | – | N/A | ns |
| SCLK Clock High Time ⁽⁴²⁾ | t_{WSCLKH} | 110 | – | N/A | ns |
| SCLK Clock Low Time ⁽⁴²⁾ | t_{WSCLKL} | 110 | – | N/A | ns |
| Falling Edge of $\overline{\text{CS}}$ to Rising Edge of SCLK ⁽⁴²⁾ | t_{LEAD} | 100 | – | N/A | ns |
| Falling Edge of SCLK to $\overline{\text{CS}}$ Rising Edge ⁽⁴²⁾ | t_{LAG} | 100 | – | N/A | ns |
| MOSI to Falling Edge of SCLK ⁽⁴²⁾ | t_{SISU} | 40 | – | N/A | ns |
| Falling Edge of SCLK to MOSI ⁽⁴²⁾ | t_{SIH} | 40 | – | N/A | ns |
| MISO Rise Time ⁽⁴²⁾ $C_{\text{L}} = 220\text{ pF}$ | t_{RSO} | – | 40 | – | ns |
| MISO Fall Time ⁽⁴²⁾ $C_{\text{L}} = 220\text{ pF}$ | t_{FSO} | – | 40 | – | ns |
| Time from Falling or Rising Edges of $\overline{\text{CS}}$ to: ⁽⁴²⁾ - MISO Low-impedance - MISO High-impedance | t_{SOEN} t_{SODIS} | 0.0 0.0 | – – | 50 50 | ns |
| Time from Rising Edge of SCLK to MISO Data Valid ⁽⁴²⁾ $0.2 \times V_{\text{DD}} \leq \text{MISO} \leq 0.8 \times V_{\text{DD}}$, $C_{\text{L}} = 100\text{ pF}$ | t_{VALID} | 0.0 | – | 75 | ns |
| RST OUTPUT PIN | | | | | |
| Reset Low-level Duration After V_{DD} High (see Figure 12) | t_{RST} | 0.65 | 1.0 | 1.35 | ms |
| Reset Deglitch Filter Time | t_{RSTDF} | 350 | 480 | 900 | ns |
| WINDOW WATCHDOG CONFIGURATION PIN (WDCONF) | | | | | |
| Watchdog Time Period ⁽⁴³⁾ External Resistor $R_{\text{EXT}} = 20\text{ k}\Omega$ (1%) External Resistor $R_{\text{EXT}} = 200\text{ k}\Omega$ (1%) Without External Resistor R_{EXT} (WDCONF Pin Open) | t_{PWD} | 8.5 79 110 | 10 94 150 | 11.5 108 205 | ms |

Notes

42. This parameter is guaranteed by process monitoring but not production tested.
 43. Watchdog timing period calculation formula: $t_{\text{PWD}} [\text{ms}] = [0.466 * (R_{\text{EXT}} - 20)] + 10$ with (R_{EXT} in $\text{k}\Omega$)

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$ for the 33910 and $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 85^{\circ}\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---|-----------|---------|-----------|---------------|
| L1 INPUT | | | | | |
| L1 Filter Time Deglitcher ⁽⁴⁴⁾ | t_{WUF} | 8.0 | 20 | 38 | μs |
| STATE MACHINE TIMING | | | | | |
| Delay Between $\overline{\text{CS}}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop Mode Activation ⁽⁴⁴⁾ | t_{STOP} | — | — | 5.0 | μs |
| Normal Request Mode Timeout (see Figure 12) | t_{NRTOUT} | 110 | 150 | 205 | ms |
| Cyclic Sense ON Time from Stop and Sleep Mode ⁽⁴⁵⁾ | T_{ON} | 130 | 200 | 270 | μs |
| Cyclic Sense Accuracy ⁽⁴⁴⁾ | | -35 | | +35 | % |
| Delay Between SPI Command and HS Turn On ⁽⁴⁶⁾ $9.0\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | $t_{\text{S-ON}}$ | — | — | 10 | μs |
| Delay Between SPI Command and HS Turn Off ⁽⁴⁶⁾ $9.0\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | $t_{\text{S-OFF}}$ | — | — | 10 | μs |
| Delay Between Normal Request and Normal Mode After a Watchdog Trigger Command (Normal Request Mode) ⁽⁴⁴⁾ | t_{SNR2N} | — | — | 10 | μs |
| Delay Between $\overline{\text{CS}}$ Wake-up ($\overline{\text{CS}}$ LOW to HIGH) in Stop Mode and: Normal Request mode, VDD ON and $\overline{\text{RST}}$ HIGH First Accepted SPI Command | $t_{\text{WU}\overline{\text{CS}}}$ t_{WUSPI} | 9.0 90 | 15 — | 80 N/A | μs |
| Minimum Time Between Rising and Falling Edge on the $\overline{\text{CS}}$ | $t_{2\overline{\text{CS}}}$ | 4.0 | — | — | μs |
| J2602 DEGLITCHER | | | | | |
| V_{SUP} Deglitcher ⁽⁴⁷⁾ (DIS_J2602 = 0) | $t_{\text{J2602_DEG}}$ | 35 | 50 | 70 | μs |

Notes

44. This parameter is guaranteed by process monitoring but not production tested.
45. This parameter is 100% tested on an Automatic Tester. However, since it has not been monitored during reliability stresses, Freescale does not guarantee this parameter during the product's life time.
46. Delay between turn on or off command (rising edge on $\overline{\text{CS}}$) and HS ON or OFF, excluding rise or fall time due to external load.
47. This parameter has not been monitoring during operating life test.

ELECTRICAL CHARACTERISTICS
DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$ for the 33910 and $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 85^{\circ}\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|--------|-------|-----|-------|------|
| LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION^{(48), (49)} | | | | | |
| Duty Cycle 1: $TH_{\text{REC(MAX)}} = 0.744 * V_{\text{SUP}}$ $TH_{\text{DOM(MAX)}} = 0.581 * V_{\text{SUP}}$ $D1 = t_{\text{BUS_REC(MIN)}} / (2 * t_{\text{BIT}})$, $t_{\text{BIT}} = 50\text{ }\mu\text{s}$, $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ | D1 | 0.396 | — | — | |
| Duty Cycle 2: $TH_{\text{REC(MIN)}} = 0.422 * V_{\text{SUP}}$ $TH_{\text{DOM(MIN)}} = 0.284 * V_{\text{SUP}}$ $D2 = t_{\text{BUS_REC(MAX)}} / (2 * t_{\text{BIT}})$, $t_{\text{BIT}} = 50\text{ }\mu\text{s}$, $7.6\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ | D2 | — | — | 0.581 | |

LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR SLOW SLEW RATE - 10.4KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION^{(48), (50)}

| | | | | | |
|--|----|-------|---|-------|--|
| Duty Cycle 3: $TH_{\text{REC(MAX)}} = 0.778 * V_{\text{SUP}}$ $TH_{\text{DOM(MAX)}} = 0.616 * V_{\text{SUP}}$ $D3 = t_{\text{BUS_REC(MIN)}} / (2 * t_{\text{BIT}})$, $t_{\text{BIT}} = 96\text{ }\mu\text{s}$, $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ | D3 | 0.417 | — | — | |
| Duty Cycle 4: $TH_{\text{REC(MIN)}} = 0.389 * V_{\text{SUP}}$ $TH_{\text{DOM(MIN)}} = 0.251 * V_{\text{SUP}}$ $D4 = t_{\text{BUS_REC(MAX)}} / (2 * t_{\text{BIT}})$, $t_{\text{BIT}} = 96\text{ }\mu\text{s}$, $7.6\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ | D4 | — | — | 0.590 | |

Notes

48. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 k Ω , 6.8 nF / 660 Ω , 10 nF / 500 Ω . Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See [Figure 6](#).
49. See [Figure 7](#).
50. See [Figure 8](#).

Table 5. Dynamic Electrical Characteristics (continued)

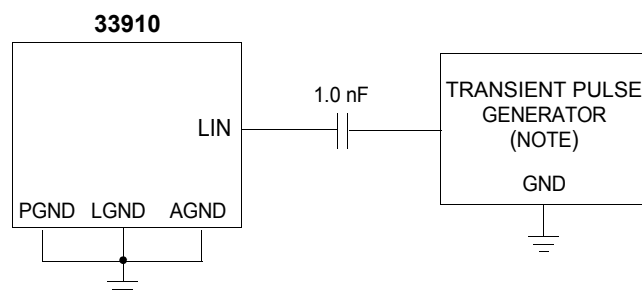
Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the 33910 and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|--------------------------|------|-----|------|------------------|
| LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR FAST SLEW RATE | | | | | |
| LIN Fast Slew Rate (Programming Mode) | SR _{FAST} | — | 20 | — | V/ μs |
| LIN PHYSICAL LAYER: CHARACTERISTICS AND WAKE-UP TIMINGS⁽⁵¹⁾ | | | | | |
| Propagation Delay and Symmetry ⁽⁵²⁾ | | | | | μs |
| Propagation Delay of Receiver, $t_{\text{REC_PD}} = \text{MAX}(t_{\text{REC_PDR}}, t_{\text{REC_PDF}})$ | $t_{\text{REC_PD}}$ | — | 4.2 | 6.0 | |
| Symmetry of Receiver Propagation Delay, $t_{\text{REC_PDF}} - t_{\text{REC_PDR}}$ | $t_{\text{REC_SYM}}$ | -2.0 | — | 2.0 | |
| Bus Wake-Up Deglitcher (Sleep and Stop modes) ^{(53)(57) (54)} | t_{PROPWL} | 42 | 70 | 95 | μs |
| Bus Wake-Up Event Reported | | | | | μs |
| From Sleep mode ⁽⁵⁵⁾ | $t_{\text{WAKE_SLEEP}}$ | — | — | 1500 | |
| From Stop mode ⁽⁵⁶⁾ | $t_{\text{WAKE_STOP}}$ | 9.0 | 27 | 35 | |
| TXD Permanent Dominant State Delay | t_{TXDDOM} | 0.65 | 1.0 | 1.35 | s |
| PULSE WIDTH MODULATION INPUT PIN (PWMIN) | | | | | |
| PWMIN pin ⁽⁵⁷⁾ | f_{PWMIN} | | | | kHz |
| Max. frequency to drive HS output pins | | | 10 | | |

Notes

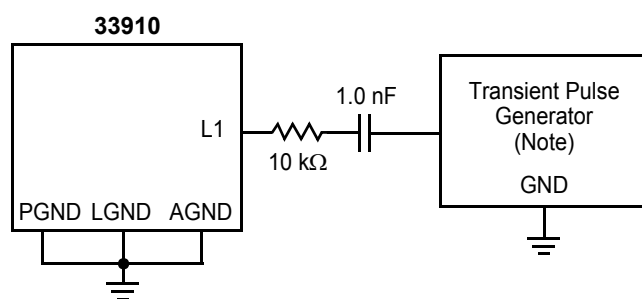
51. V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 k Ω , 6.8 nF / 660 Ω , 10 nF / 500 Ω . Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See [Figure 6](#).
52. See [Figure 9](#)
53. See [Figure 10](#), for Sleep and [Figure 11](#), for Stop mode.
54. This parameter is tested on automatic tester but has not been monitoring during operating life test.
55. The measurement is done with 1.0 μF capacitor and 0 mA current load on V_{DD} . The value takes into account the delay to charge the capacitor. The delay is measured between the bus wake-up threshold (V_{BUSWU}) rising edge of the LIN bus and when V_{DD} reaches 3.0 V. See [Figure 10](#). The delay depends of the load and capacitor on V_{DD} .
56. In Stop mode, the delay is measured between the bus wake-up threshold (V_{BUSWU}) and the falling edge of the $\overline{\text{IRQ}}$ pin. See [Figure 11](#).
57. This parameter is guaranteed by process monitoring but not production tested.

TIMING DIAGRAMS



Note Waveform per ISO 7637-2. Test Pulses 1, 2, 3a, 3b.

Figure 4. Test Circuit for Transient Test Pulses (LIN)



Note Waveform per ISO 7637-2. Test Pulses 1, 2, 3a, 3b,.

Figure 5. Test Circuit for Transient Test Pulses (L1)

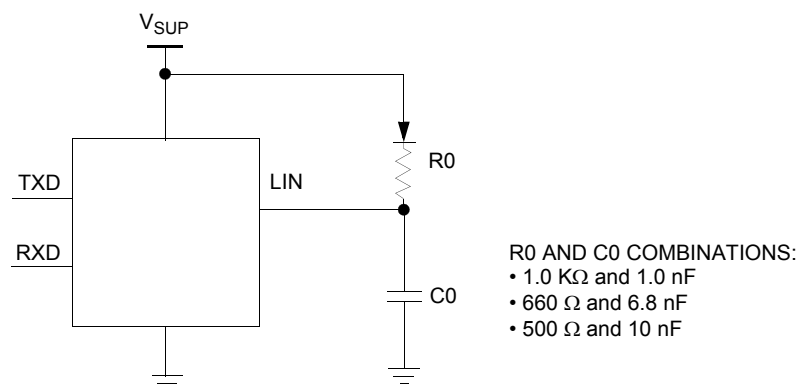


Figure 6. Test Circuit for LIN Timing Measurements

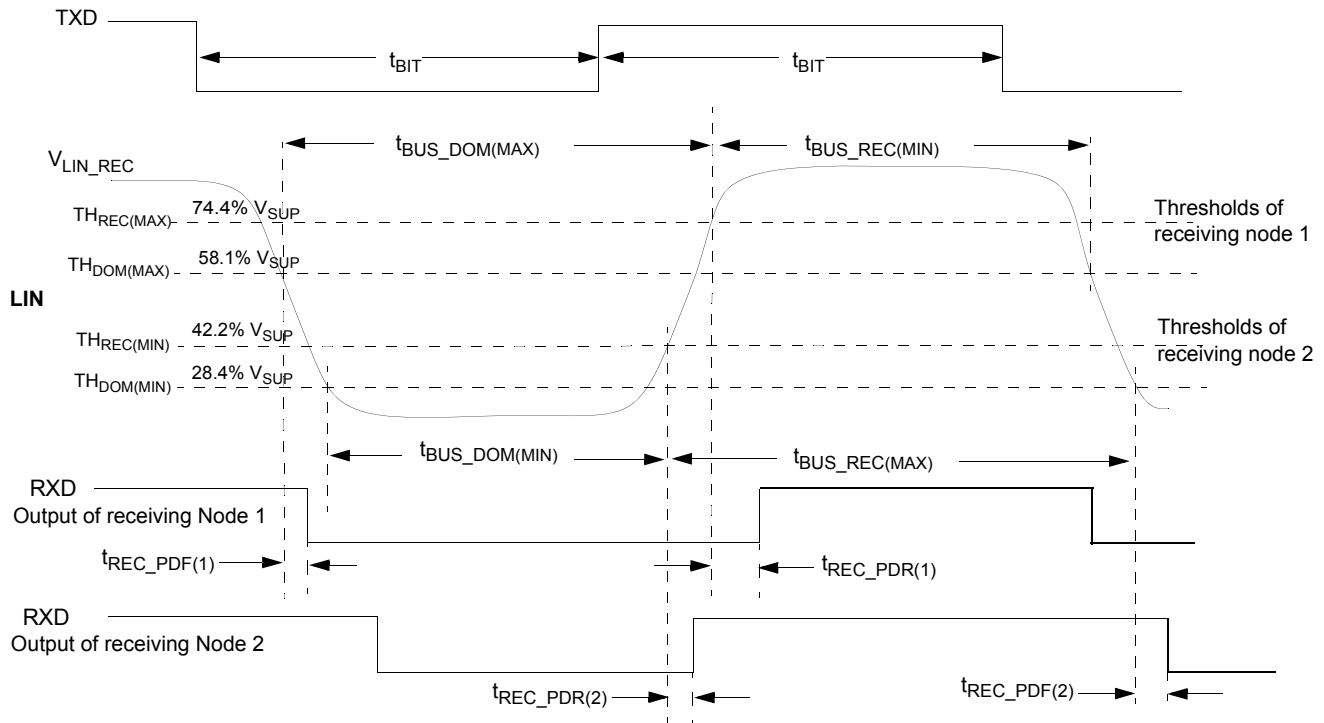


Figure 7. LIN Timing Measurements for Normal Slew Rate

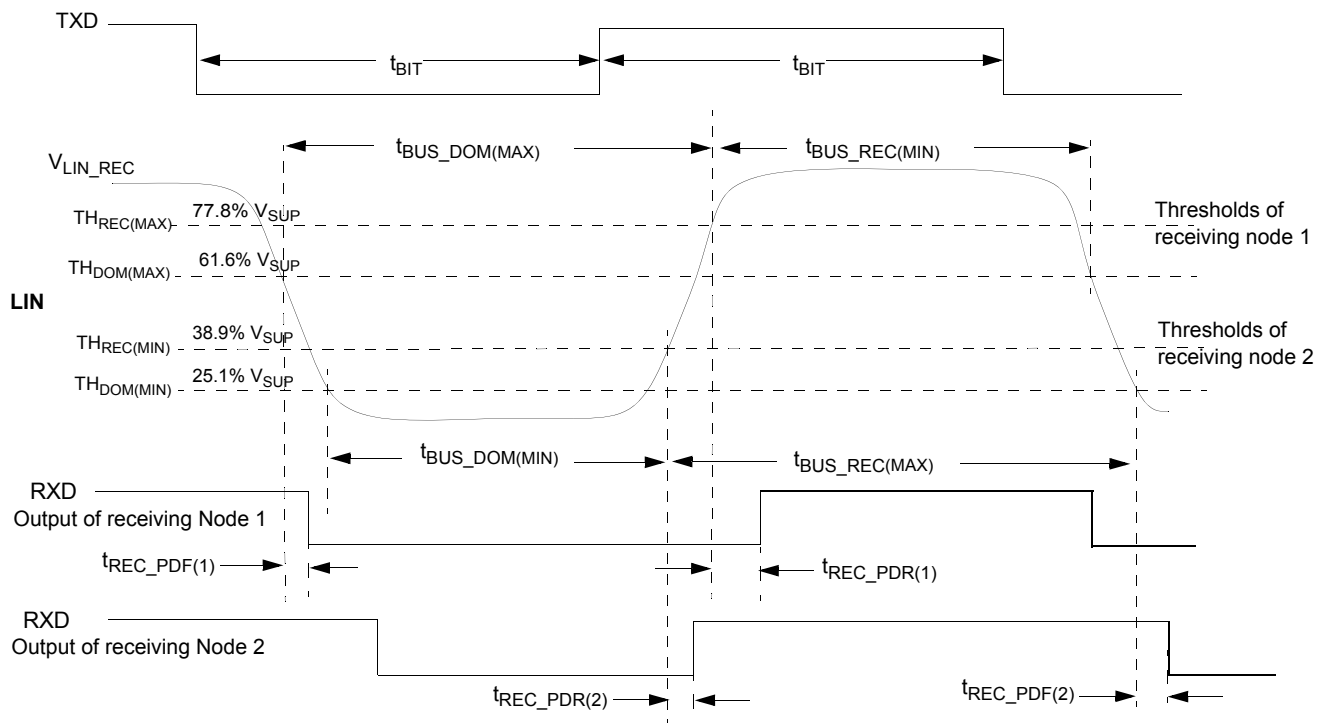


Figure 8. LIN Timing Measurements for Slow Slew Rate

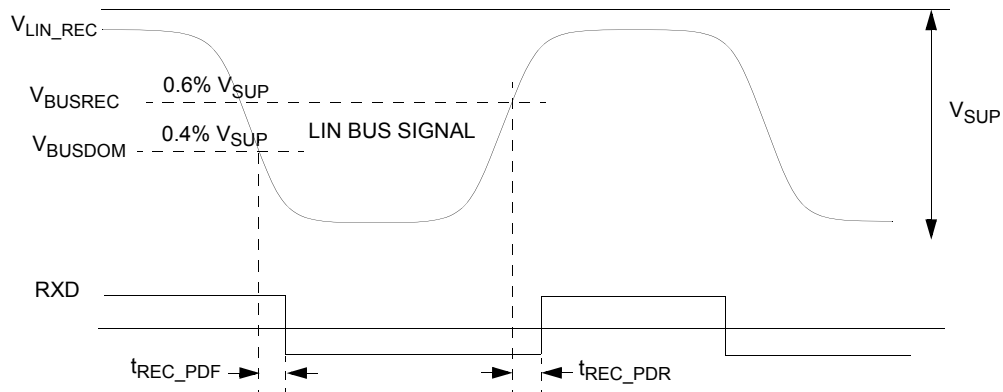


Figure 9. LIN Receiver Timing

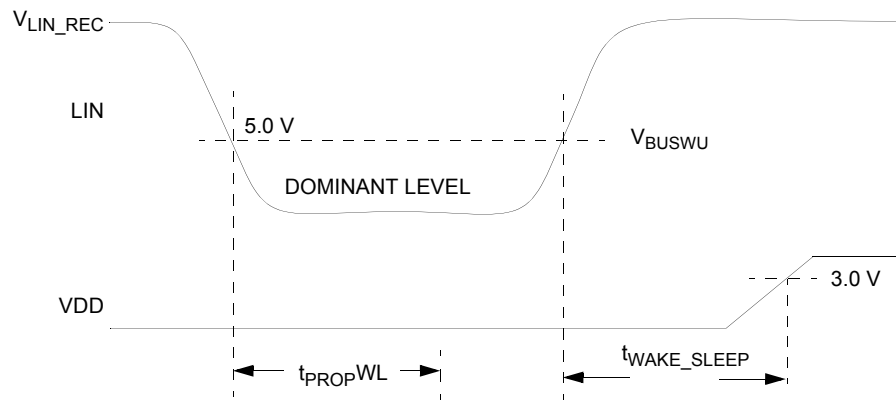


Figure 10. LIN Wake-up Sleep Mode Timing

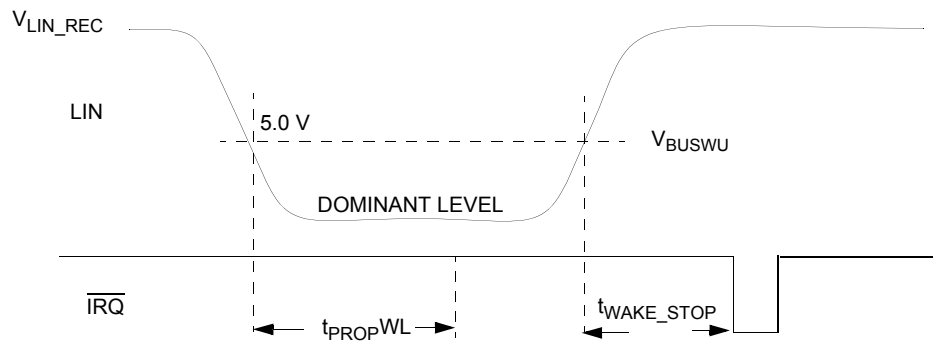


Figure 11. LIN Wake-up Stop Mode Timing

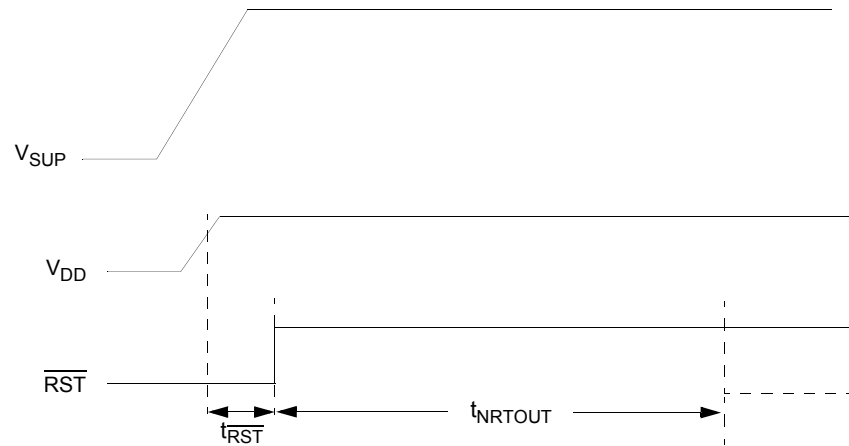


Figure 12. Power On Reset and Normal Request Timeout Timing

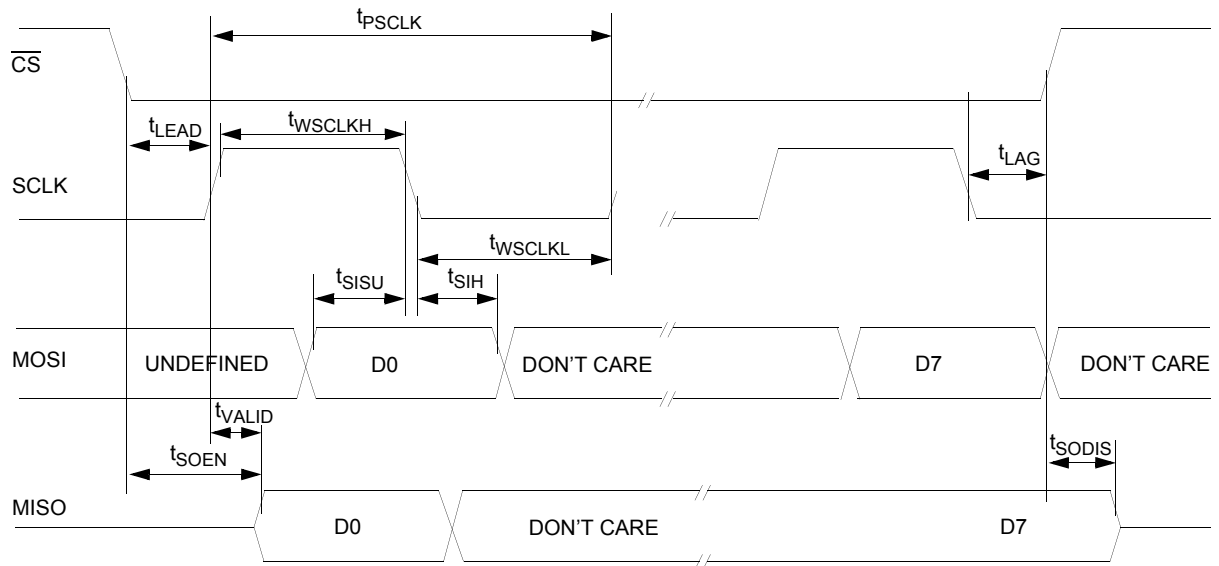


Figure 13. SPI Timing Characteristics

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33910 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 33910 is well suited to perform keypad applications via the LIN bus.

Power switches are provided on the device configured as high side outputs. Other ports are also provided, which

include a Hall Sensor port supply, and one wake-up capable pin. An internal voltage regulator provides power to a MCU device.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

FUNCTIONAL PIN DESCRIPTION

See [Figure 1, 33910 Simplified Application Diagram](#), for a graphic representation of the various pins referred to in the following paragraphs. Also, see [Pin Connections](#) for a description of the pin locations in the package.

RECEIVER OUTPUT PIN (RXD)

The RXD pin is a digital output. It is the receiver output of the LIN interface and reports the state of the bus voltage: RXD Low when LIN bus is dominant, RXD High when LIN bus is recessive.

TRANSMITTER INPUT PIN (TXD)

The TXD pin is a digital input. It is the transmitter input of the LIN interface and controls the state of the bus output (dominant when TXD is Low, recessive when TXD is High).

This pin has an internal pull-up to force recessive state in case the input is left floating.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is compliant to the LIN bus specification 2.0, 2.1, and SAE J2602-2.

The LIN interface is only active during Normal mode. See [Table 6, Operating Modes Overview](#).

SERIAL DATA CLOCK PIN (SCLK)

The SCLK pin is the SPI clock input. MISO data changes on the positive transition of the SCLK. MOSI is sampled on the negative edge of the SCLK.

MASTER OUT SLAVE IN PIN (MOSI)

The MOSI digital pin receives SPI data from the MCU. This data input is sampled on the negative edge of SCLK.

MASTER IN SLAVE OUT PIN (MISO)

The MISO pin sends data to an SPI-enabled MCU. It is a digital tri-state output used to shift serial data to the microcontroller. Data on this output pin changes on the positive edge of the SCLK. When CS is High, this pin will remain in the high-impedance state.

CHIP SELECT PIN ($\overline{\text{CS}}$)

$\overline{\text{CS}}$ is an active low digital input. It must remain low during a valid SPI communication and allow for several devices to be connected in the same SPI bus without contention. A rising edge on $\overline{\text{CS}}$ signals the end of the transmission and the moment the data shifted in is latched. A valid transmission must consist of 8 bits only.

While in STOP mode, a low-to-high level transition on this pin will generate a wake-up condition for the 33910.

ANALOG MULTIPLEXER PIN (ADOUT0)

The ADOUT0 pin can be configured via the SPI to allow the MCU A/D converter to read the several inputs of the Analog Multiplexer, including the VSENSE and L1 input voltages, and the internal junction temperature.

PWM INPUT CONTROL PIN (PWMIN)

This digital input can control the high sides drivers in Normal Request and Normal mode.

To enable PWM control, the MCU must perform a write operation to the High Side Control Register (HSCR).

This pin has an internal 20 μA current pull-up.

RESET PIN ($\overline{\text{RST}}$)

This bidirectional pin is used to reset the MCU in case the 33910 detects a reset condition, or to inform the 33910 that the MCU has just been reset. After release of the $\overline{\text{RST}}$ pin, Normal Request mode is entered.

The $\overline{\text{RST}}$ pin is an active low filtered input and output formed by a weak pull-up and a switchable pull-down structure which allows this pin to be shorted either to V_{DD} or to GND during software development, without the risk of destroying the driver.

INTERRUPT PIN ($\overline{\text{IRQ}}$)

The $\overline{\text{IRQ}}$ pin is a digital output used to signal events or faults to the MCU while in Normal and Normal Request mode or to signal a wake-up from Stop mode. This active low output will transition to high only after the interrupt is acknowledged by a SPI read of the respective status bits.

WATCHDOG CONFIGURATION PIN (WDCONF)

The WDCONF pin is the configuration pin for the internal watchdog. A resistor can be connected to this pin to configure the window watchdog period. When connected directly to ground, the watchdog will be disabled. When this pin is left open, the watchdog period is fixed to its lower precision internal default value (150 ms typical).

GROUND CONNECTION PINS (AGND, PGND, LGND)

The AGND, PGND and LGND pins are the Analog and Power ground pins.

The AGND pin is the ground reference of the voltage regulator module.

The PGND and LGND pins are used for high current load return as in the LIN interface pin.

Note: PGND, AGND and LGND pins must be connected together.

DIGITAL/ANALOG PIN (L1)

The L1 pin is multi purpose input. It can be used as a digital input, which can be sampled by reading the SPI and used for wake-up when 33910 is in low power mode or used as analog

input for the analog multiplexer. When used to sense voltage outside the module, a 33 kohm series resistor must be used on the input.

When used as wake-up input L1 can be configured to operate in cyclic-sense mode. In this mode one or both of the high side switches are configured to be periodically turned on and sample the wake-up input. If a state change is detected between two cycles a wake-up is initiated. The 33910 can also wake-up from Stop or Sleep by a simple state change on L1.

When used as analog input, the voltage present on the L1 pin is scaled down by an selectable internal voltage divider and can be routed to the ADOUT0 output through the analog multiplexer.

Note: If L1 input is selected in the analog multiplexer, it will be disabled as digital input and remains disabled in low power mode. No wake-up feature is available in that condition.

When the L1 input is not selected in the analog multiplexer, the voltage divider is disconnected from that input.

HIGH SIDE OUTPUT PINS (HS1 AND HS2)

These two high side switches are able to drive loads such as relays or lamps. Their structures are connected to the VS2 supply pin. The pins are short-circuit protected and both outputs are also protected against overheating.

HS1 and HS2 are controlled by SPI and can respond to a signal applied to the PWMIN input pin.

HS1 and HS2 outputs can also be used during low-power mode for the cyclic-sense of the wake inputs.

POWER SUPPLY PINS (VS1 AND VS2)

Those are the battery level voltage supply pins. In an application, VS1 and VS2 pins must be protected against reverse battery connection and negative transient voltages with external components. These pins sustain standard automotive voltage conditions such as a load dump at 40 V.

The high side switches (HS1 and HS2) are supplied by the VS2 pin. All other internal blocks are supplied by the VS1 pin.

VOLTAGE SENSE PIN (VSENSE)

This input can be connected directly to the battery line. It is protected against battery reverse connection. The voltage present in this input is scaled down by an internal voltage divider, and can be routed to the ADOUT0 output pin and used by the MCU to read the battery voltage.

The ESD structure on this pin allows for excursion up to +40 V and down to -27 V, allowing this pin to be connected directly to the battery line. It is strongly recommended to connect a 10 kohm resistor in series with this pin for protection purposes.

HALL SENSOR SWITCHABLE SUPPLY PIN (HVDD)

This pin provides a switchable supply for external hall sensors. While in Normal mode, this current limited output can be controlled through the SPI.

The HVDD pin needs to be connected to an external capacitor to stabilize the regulated output voltage.

+5.0 V MAIN REGULATOR OUTPUT PIN (VDD)

An external capacitor has to be placed on the VDD pin to stabilize the regulated output voltage. The VDD pin is intended to supply a microcontroller. The pin is current limited against shorts to GND and over-temperature protected.

During Stop mode, the voltage regulator does not operate with its full drive capabilities and the output current is limited.

During Sleep mode, the regulator output is completely shut down.

FUNCTIONAL DEVICE OPERATIONS

OPERATIONAL MODES

INTRODUCTION

The 33910 offers three main operating modes: Normal (Run), Stop, and Sleep (Low Power). In Normal mode, the device is active and is operating under normal application conditions. The Stop and Sleep modes are low power modes with wake-up capabilities.

In Stop mode, the voltage regulator still supplies the MCU with V_{DD} (limited current capability), while in Sleep mode the voltage regulator is turned off ($V_{DD} = 0$ V).

Wake-up from Stop mode is initiated by a wake-up interrupt. Wake-up from Sleep mode is done by a reset and the voltage regulator is turned back on.

The selection of the different modes is controlled by the MOD1:2 bits in the Mode Control Register (MCR).

[Figure 14](#) describes how transitions are done between the different operating modes. [Table 6](#) gives an overview of the operating modes.

RESET MODE

The 33910 enters the Reset mode after a power up. In this mode, the \overline{RST} pin is low for 1.0 ms (typical value). After this delay, it enters the Normal Request mode and the \overline{RST} pin is driven high.

The Reset mode is entered if a reset condition occurs (V_{DD} low, watchdog trigger fail, after wake-up from Sleep mode, Normal Request mode timeout occurs).

NORMAL REQUEST MODE

This is a temporary mode automatically accessed by the device after the Reset mode, or after a wake-up from Stop mode.

In Normal Request mode, the VDD regulator is ON, the RESET pin is High, and the LIN is operating in RX Only mode.

As soon as the device enters in the Normal Request mode an internal timer is started for 150 ms (typical value). During these 150 ms, the MCU must configure the Timing Control Register (TIMCR) and the Mode Control Register (MCR) with MOD2 and MOD1 bits set = 0, to enter the Normal mode. If within the 150 ms timeout, the MCU does not command the 33910 to Normal mode, it will enter in Reset mode. If the WDCONF pin is grounded in order to disable the watchdog function, it goes directly in Normal mode after the Reset mode.

NORMAL MODE

In Normal mode, all 33910 functions are active and can be controlled by the SPI interface and the PWMIN pin.

The VDD regulator is ON and delivers its full current capability.

If an external resistor is connected between the WDCONF pin and the Ground, the window watchdog function will be enabled.

The wake-up input (L1) can be read as digital input or have its voltage routed through the analog-multiplexer.

The LIN interface has slew rate and timing compatible with the LIN protocol specification 2.0, 2.1 and SAEJ2602. The LIN bus can transmit and receive information.

The high side switches are active and have PWM capability according to the SPI configuration.

The interrupts are generated to report failures for V_{SUP} over/under-voltage, thermal shutdown, or thermal shutdown prewarning on the main regulator.

SLEEP MODE

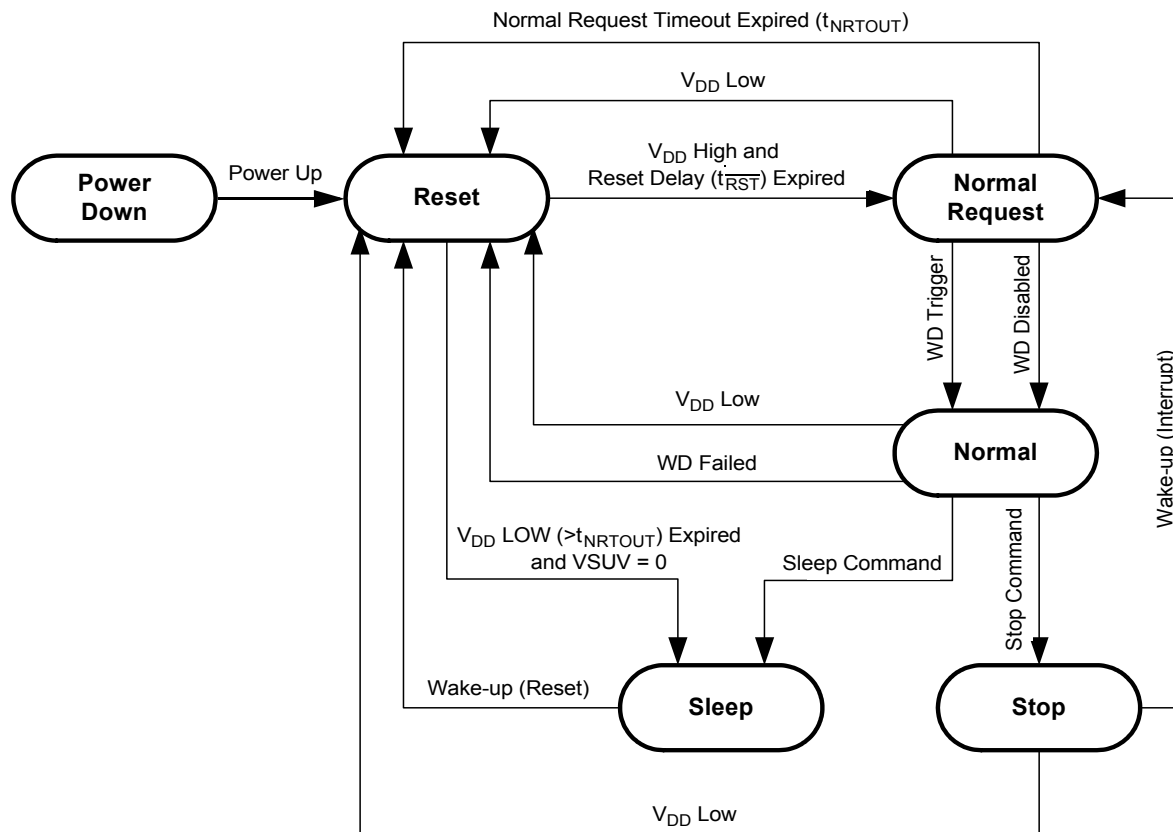
The Sleep mode is a low power mode. From Normal mode, the device enters into Sleep mode by sending one SPI command through the Mode Control Register (MCR), or (V_{DD} low > 150 ms) with $V_{SUUV} = 0$. When in Reset mode, a V_{DD} under-voltage condition with no V_{SUP} under-voltage ($V_{SUUV} = 0$) will send the device to Sleep mode. All blocks are in their lowest power consumption condition. Only some wake-up sources (wake-up input with or without cyclic sense, forced wake-up and LIN receiver) are active. The 5.0 V regulator is OFF. The internal low-power oscillator may be active if the IC is configured for cyclic-sense. In this condition, one of the high side switches is turned on periodically and the wake-up input is sampled.

Wake-up from Sleep mode is similar to a power-up. The device goes in Reset mode except that the SPI will report the wake-up source and the BATFAIL flag is not set.

STOP MODE

The Stop mode is the second low power mode, but in this case the 5.0 V regulator is ON with limited current drive capability. The application MCU is always supplied while the 33910 is operating in Stop mode.

The device can enter into Stop mode only by sending the SPI command. When the application is in this mode, it can wake-up from the 33910 side (for example: cyclic sense, force wake-up, LIN bus, wake inputs) or the MCU side (\overline{CS} , \overline{RST} pins). Wake-up from Stop mode will transition the 33910 to Normal Request mode and generates an interrupt except if the wake-up event is a low to high transition on the \overline{CS} pin or comes from the \overline{RST} pin.

**Legend**

WD: Watchdog

WD Disabled: Watchdog disabled (WDCONF pin connected to GND)

WD Trigger: Watchdog is triggered by SPI command

WD Failed: No watchdog trigger or trigger occurs in closed window

Stop Command: Stop command sent via SPI

Sleep Command: Sleep command sent via SPI

Wake-up from Stop mode: L1 state change, LIN bus wake-up, Periodic wake-up, \overline{CS} rising edge wake-up or \overline{RST} wake-up.

Wake-up from Sleep mode: L1 state change, LIN bus wake-up, Periodic wake-up.

Figure 14. Operating Modes and Transitions

Table 6. Operating Modes Overview

| Function | Reset Mode | Normal Request Mode | Normal Mode | Stop Mode | Sleep Mode |
|--------------------|-----------------------------------|-----------------------------------|-----------------------------------|----------------------|----------------------|
| VDD | Full | Full | Full | Stop | - |
| HVDD | - | SPI ⁽⁵⁸⁾ | SPI | - | - |
| HSx | - | SPI/PWM ⁽⁵⁹⁾ | SPI/PWM | Note ⁽⁶⁰⁾ | Note ⁽⁶¹⁾ |
| Analog Mux | - | SPI | SPI | - | - |
| L1 | - | Input | Input | Wake-up | Wake-up |
| LIN | - | Rx-Only | Full/Rx-Only | Rx-Only/Wake-up | Wake-up |
| Watchdog | - | 150 ms (typ.) timeout | On ⁽⁶²⁾ /Off | - | - |
| Voltage Monitoring | V _{SUP} /V _{DD} | V _{SUP} /V _{DD} | V _{SUP} /V _{DD} | V _{DD} | - |

Notes

58. Operation can be enabled/controlled by the SPI.
 59. Operation can be controlled by the PWMIN input.
 60. HSx switches can be configured for cyclic sense operation in Stop mode.
 61. HSx switches can be configured for cyclic sense operation in Sleep mode.
 62. Windowing operation when enabled by an external resistor.

INTERRUPTS

Interrupts are used to signal a microcontroller that a peripheral needs to be serviced. The interrupts which can be generated, change according to the operating mode. While in Normal and Normal Request modes, the 33910 signals through interrupts special conditions which may require a MCU software action. Interrupts are not generated until all pending wake-up sources are read in the Interrupt Source Register (ISR).

While in Stop mode, interrupts are used to signal wake-up events. Sleep mode does not use interrupts. Wake-up is performed by powering-up the MCU. In Normal and Normal Request mode the wake-up source can be read by SPI.

The interrupts are signaled to the MCU by a low logic level of the $\overline{\text{IRQ}}$ pin, which will remain low until the interrupt is acknowledged by a SPI read command of the ISR register. The $\overline{\text{IRQ}}$ pin will then be driven high.

Interrupts are only asserted while in Normal, Normal Request and Stop mode. Interrupts are not generated while the RST pin is low.

The following is a list of the interrupt sources in Normal and Normal Request modes. Some of these can be masked by writing to the SPI - Interrupt Mask Register (IMR).

Low-voltage Interrupt:

Signals when the supply line (VS1) voltage drops below the VSUV threshold (V_{SUV}).

High-voltage Interrupt:

Signals when the supply line (VS1) voltage increases above the VSOV threshold (V_{SOV}).

Over-temperature Prewarning:

Signals when the 33910 temperature has reached the pre-shutdown warning threshold. It is used to warn the MCU that an over-temperature shutdown in the main 5.0 V regulator is imminent.

LIN Over-temperature Shutdown / TXD Stuck At Dominant / RXD Short-circuit:

These signal fault conditions within the LIN interface will cause the LIN driver to be disabled. In order to restart the operation, the fault must be removed and TXD must go recessive.

High Side Over-temperature Shutdown:

Signals a shutdown in the high side outputs.

RESET

To reset a MCU the 33910 drives the $\overline{\text{RST}}$ pin low for the time the reset condition lasts.

After the reset source is removed, the state machine will drive the $\overline{\text{RST}}$ output low for at least 1.0 ms (typical value) before driving it high.

In the 33910, four main reset sources exist:

5.0 V Regulator Low-voltage-Reset ($\overline{\text{V}_{\text{RSTTH}}}$)

The 5.0 V regulator output V_{DD} is continuously monitored against brown outs. If the supply monitor detects that the voltage at the V_{DD} pin has dropped below the reset threshold $\overline{\text{V}_{\text{RSTTH}}}$ the 33910 will issue a reset. In case of over-temperature, the voltage regulator will be disabled and the voltage monitoring will issue a V_{DDOT} Flag independently of the V_{DD} voltage.

Window Watchdog Overflow

If the watchdog counter is not properly serviced while its window is open, the 33910 will detect an MCU software run-away and will reset the microcontroller.

Wake-up From Sleep Mode

During Sleep mode, the 5.0 V regulator is not active, hence all wake-up requests from Sleep mode require a power-up/reset sequence.

External Reset

The 33910 has a bidirectional reset pin which drives the device to a safe state (same as Reset mode) for as long as this pin is held low. The $\overline{\text{RST}}$ pin must be held low long enough to pass the internal glitch filter and get recognized by the internal reset circuit. This functionality is also active in Stop mode.

After the $\overline{\text{RST}}$ pin is released, there is no extra $t_{\overline{\text{RST}}}$ to be considered.

WAKE-UP CAPABILITIES

Once entered into one of the low-power modes (Sleep or Stop) only wake-up sources can bring the device into Normal mode operation.

In Stop mode, a wake-up is signaled to the MCU as an interrupt, while in Sleep mode the wake-up is performed by activating the 5.0 V regulator and resetting the MCU. In both cases the MCU can detect the wake-up source by accessing the SPI registers and reading the Interrupt Source Register. There is no specific SPI register bit to signal a $\overline{\text{CS}}$ wake-up or external reset. If necessary this condition is detected by excluding all other possible wake-up sources.

Wake-up from Wake-up input (L1) with cyclic sense disabled

The wake-up line is dedicated to sense state changes of external switch and wake-up the MCU (in Sleep or Stop mode).

In order to select and activate direct wake-up from L1 input, the Wake-up Control Register (WUCR) must be configured with appropriate L1WE input enabled or disabled. The wake-up input's state is read through the Wake-up Status Register (WUSR).

L1 input is also used to perform cyclic-sense wake-up.

Note: Selecting an L1 input in the analog multiplexer before entering low power mode will disable the wake-up capability of the L1 input

Wake-up from Wake-up input (L1) with cyclic sense timer enabled

The SBCLIN can wake-up at the end of a cyclic sense period if on the wake-up input line (L1) a state change occurs. One or both HSx switch can be activated in Sleep or Stop modes from an internal timer. Cyclic sense and force wake-up are exclusive. If cyclic sense is enabled, the force wake-up can not be enabled.

In order to select and activate the cyclic sense wake-up from the L1 input, before entering in low power modes (Stop or Sleep modes), the following SPI set-up has to be performed:

In WUCR: select the L1 input to WU-enable.

In HSCR: enable the desired HSx.

- In TIMCR: select the $\overline{\text{CS/WD}}$ bit and determine the cyclic sense period with CYSTx bits.
- Perform Goto Sleep/Stop command.

Forced Wake-up

The 33910 can wake-up automatically after a predetermined time spent in Sleep or Stop mode. Cyclic sense and Forced wake-up are exclusive. If Forced wake-up is enabled, the Cyclic Sense can not be enabled.

To determine the wake-up period, the following SPI set-up has to be sent before entering in low power modes:

- In TIMCR: select the $\overline{\text{CS/WD}}$ bit and determine the low power mode period with CYSTx bits.
- In HSCR: all HSx bits must be disabled.

$\overline{\text{CS}}$ Wake-up

While in Stop mode, a rising edge on the $\overline{\text{CS}}$ will cause a wake-up. The $\overline{\text{CS}}$ wake-up does not generate an interrupt, and is not reported on SPI.

LIN Wake-up

While in the low-power mode, the 33910 monitors the activity on the LIN bus. A dominant pulse larger than t_{PROPWL} followed by a dominant to recessive transition will cause a LIN wake-up. This behavior protects the system from a short to ground bus condition. The bit $\text{RXONLY} = 1$ from LINCR Register disables the LIN wake-up from Stop mode.

RST Wake-up

While in Stop mode, the 33910 can wake-up when the $\overline{\text{RST}}$ pin is held low long enough to pass the internal glitch filter. Then, the 33910 will change to Normal Request or Normal modes depending on the WDCONF pin configuration. The $\overline{\text{RST}}$ wake-up does not generate an interrupt and is not reported via SPI.

From Stop mode, the following wake-up events can be configured:

- Wake-up from L1 input without cyclic sense
- Cyclic sense wake-up inputs
- Force wake-up
- $\overline{\text{CS}}$ wake-up
- LIN wake-up
- $\overline{\text{RST}}$ wake-up

From Sleep mode, the following wake-up events can be configured:

- Wake-up from L1 input without cyclic sense
- Cyclic sense wake-up inputs
- Force wake-up
- LIN wake-up

WINDOW WATCHDOG

The 33910 includes a configurable window watchdog which is active in Normal mode. The watchdog can be configured by an external resistor connected to the WDCONF pin. The resistor is used to achieve higher precision in the timebase used for the watchdog.

SPI clears are performed by writing through the SPI in the MOD bits of the Mode Control Register (MCR).

During the first half of the SPI timeout, watchdog clears are not allowed, but after the first half of the SPI timeout window, the clear operation opens. If a clear operation is performed outside the window, the 33910 will reset the MCU, in the same way as when the watchdog overflows.

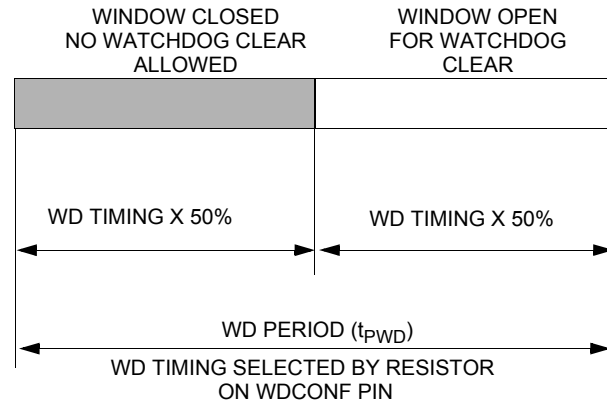


Figure 15. Window Watchdog Operation

To disable the watchdog function in Normal mode the user must connect the WDCONF pin to ground. This measure effectively disables Normal Request mode. The WDOFF bit in the Watchdog Status Register (WDSR) will be set. This condition is only detected during Reset mode.

If neither a resistor nor a connection to ground is detected, the watchdog falls back to the internal lower precision timebase of 150 ms (typ.) and signals the faulty condition through the Watchdog Status Register (WDSR).

The watchdog timebase can be further divided by a prescaler which can be configured by the Timing Control Register (TIMCR). During Normal Request mode, the window watchdog is not active but there is a 150 ms (typ.) timeout for leaving the Normal Request mode. In case of a timeout, the 33910 will enter into Reset mode, resetting the microcontroller before entering again into Normal Request mode.

FAULTS DETECTION MANAGEMENT

The 33910 has the capability to detect faults like an over or under-voltage on VS1, TxD in permanent Dominant State, Over-temperature on HS, LIN. It is able to take corrective actions accordingly. Most of faults are monitoring through SPI and the Interrupt pin. The microcontroller can also take actions.

The following table summarizes all fault sources the device is able to detect with associated conditions. The status for a device recovery and the SPI or pins monitoring are also described.

Table 7. Fault Detection Management Conditions

| BLOCK | FAULT | MODE | CONDITION | FALLOUT | RECOVERY | MONITORING ⁽⁶⁴⁾ | |
|--------------|------------------------------------|----------------------------|---|---|---|--|--------------------------------------|
| | | | | | | REG (FLAG, BIT) | INTERRUPT |
| Power Supply | BATTERY FAIL | All modes | V _{SUP} <3.0 V (typ) then power-up | - | Condition gone | VSR (BATFAIL, 0) | - |
| | VSUP OVER-VOLTAGE | Normal, Normal Request | V _{SUP} > 19.25 V (typ) | In Normal mode, HS shutdown if bit HVSE=1 (reg MCR) | Condition gone, to re-enable HS write to HSCR registers | VSR (VSOV,3) | IRQ low + ISR (0101) ⁽⁶⁵⁾ |
| | VSUP UNDER-VOLTAGE | | V _{SUP} < 6.0 V (typ) | - | Condition gone | VSR (VSUV,2) | IRQ low + ISR (0101) |
| | VDD UNDER-VOLTAGE | All except Sleep | V _{DD} < 4.5 V (typ) | Reset ⁽⁶³⁾ | | - | - |
| | VDD OVER-TEMP PREWARNING | All except Low Power modes | Temperature > 115°C (typ) | - | | VSR (VDDOT,1) | IRQ low + ISR (0101) |
| | VDD OVER-TEMPERATURE | | Temperature > 170°C (typ) | VDD shutdown, Reset then Sleep | | - | - |
| LIN | RXD PIN SHORT CIRCUIT | Normal, Normal Request | RXD pin shorted to GND or 5 V | LIN trans shutdown | LIN transmitter re-enabled once the condition is gone and TXD is high | LINSR, (RXSHORT,3) | IRQ low + ISR (0100) ⁽⁶⁵⁾ |
| | TXD PIN PERMANENT DOMINANT | | TXD pin low for more than 1s (typ) | LIN transmitter shutdown | | LINSR (TXDOM,2) | |
| | LIN DRIVER OVER-TEMPERATURE | | Temperature > 160°C (typ) | | | LINSR (LINOT,1) | |
| High Side | HIGH SIDE DRIVERS OVER-TEMPERATURE | Normal, Normal Request | Temperature > 160°C (typ) | Both HS thermal shutdown | Condition gone, to re-enable HS write to HSCR reg | All flags in HSSR are set | IRQ low + ISR (0010) ⁽⁶⁵⁾ |
| | HS1 OPEN-LOAD DETECTION | | Current through HSx < 5.0 mA (typ) | - | Condition gone | HSSR (HS1OP,1) | - |
| | HS2 OPEN-LOAD DETECTION | | | | | HSSR (HS2OP,3) | |
| | HS1 OVER-CURRENT | | Current through HSx tends to rise above the current limit 60 mA (min) | HSx on with limited current capability 60 mA (min) | | HSSR (HS1CL,0) | |
| | HS2 OVER-CURRENT | | | | | HSSR (HS2CL,2) | |
| Watchdog | NORMAL REQUEST TIME-OUT EXPIRED | Normal Request | The MCU did not command the device to Normal mode within the 150 ms timeout after reset | Reset | - | - | - |
| | WATCHDOG TIMEOUT | Normal | WD timeout or WD clear within the window closed | Reset | | WDSR (WDTO, 3) | |
| | WATCHDOG ERROR | Normal | WDCONF pin is floating | WD internal lower precision timebase 150 ms (typ) | | Connect WDCONF to a resistor or to GND | |

Notes

63. When in Reset mode a VDD under-voltage condition combined with no V_{SUP} under-voltage ($VSUV=0$) will send the device to Sleep mode.
64. Registers to be read when back in Normal Request or Normal mode depending on the fault. Interrupts only generated in Normal, Normal Request and Stop modes
65. Unless masked, If masked IRQ remains high and the ISR flags are not set.

TEMPERATURE SENSE GAIN

The analog multiplexer can be configured via SPI to allow the ADOUT0 pin to deliver the internal junction temperature of the device.

The graph below illustrates the internal chip temp sense obtained per characterization at 3 temperatures with 3 different lots and 30 samples.

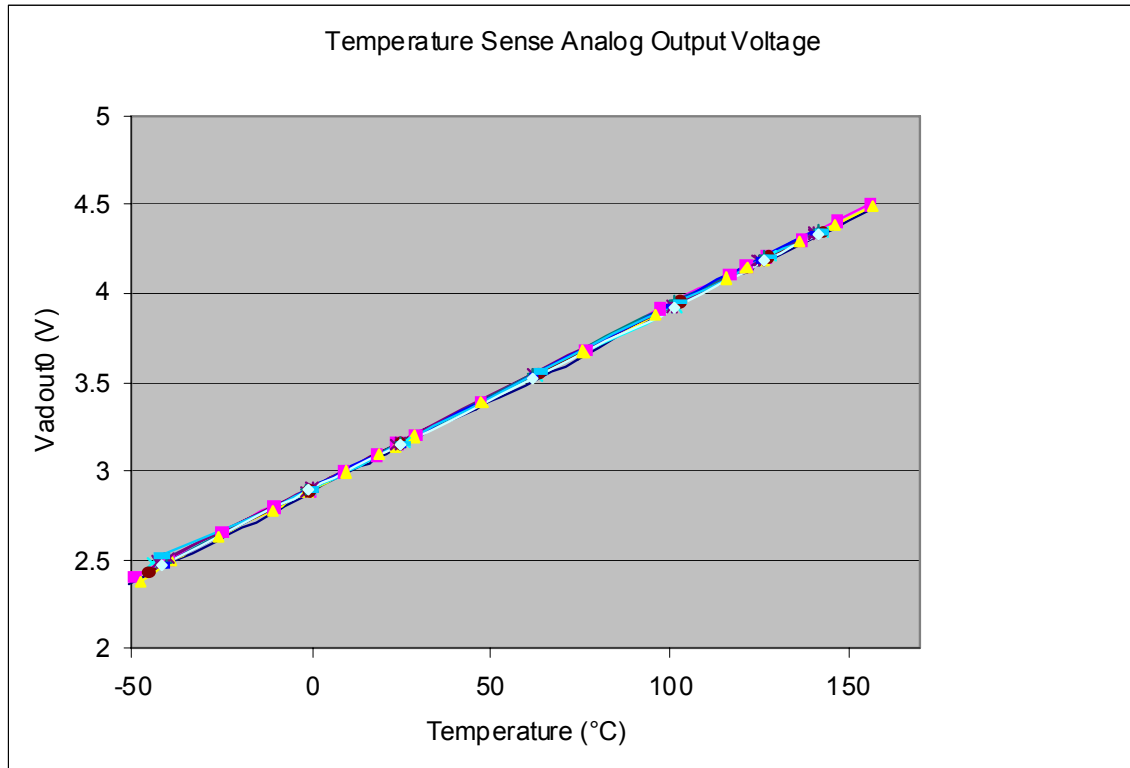


Figure 16. Temperature Sense Gain

HIGH SIDE OUTPUT PINS HS1 AND HS2

These outputs are two high side drivers intended to drive small resistive loads or LEDs incorporating the following features:

- PWM capability (software maskable)
- Open load detection
- Current limitation
- Over-temperature shutdown (with maskable interrupt)
- High-voltage shutdown (software maskable)
- Cyclic sense

The high side switches are controlled by the bits HS1:2 in the High Side Control Register (HSCR).

PWM Capability (direct access)

Each high side driver offers additional (to the SPI control) direct control via the PWMIN pin.

If both the bits HS1 and PWMHS1 are set in the High Side Control Register (HSCR), then the HS1 driver is turned on if the PWMIN pin is high and turned off if the PWMIN pin is low. This applies to HS2 configuring HS2 and PWMHS2 bits.

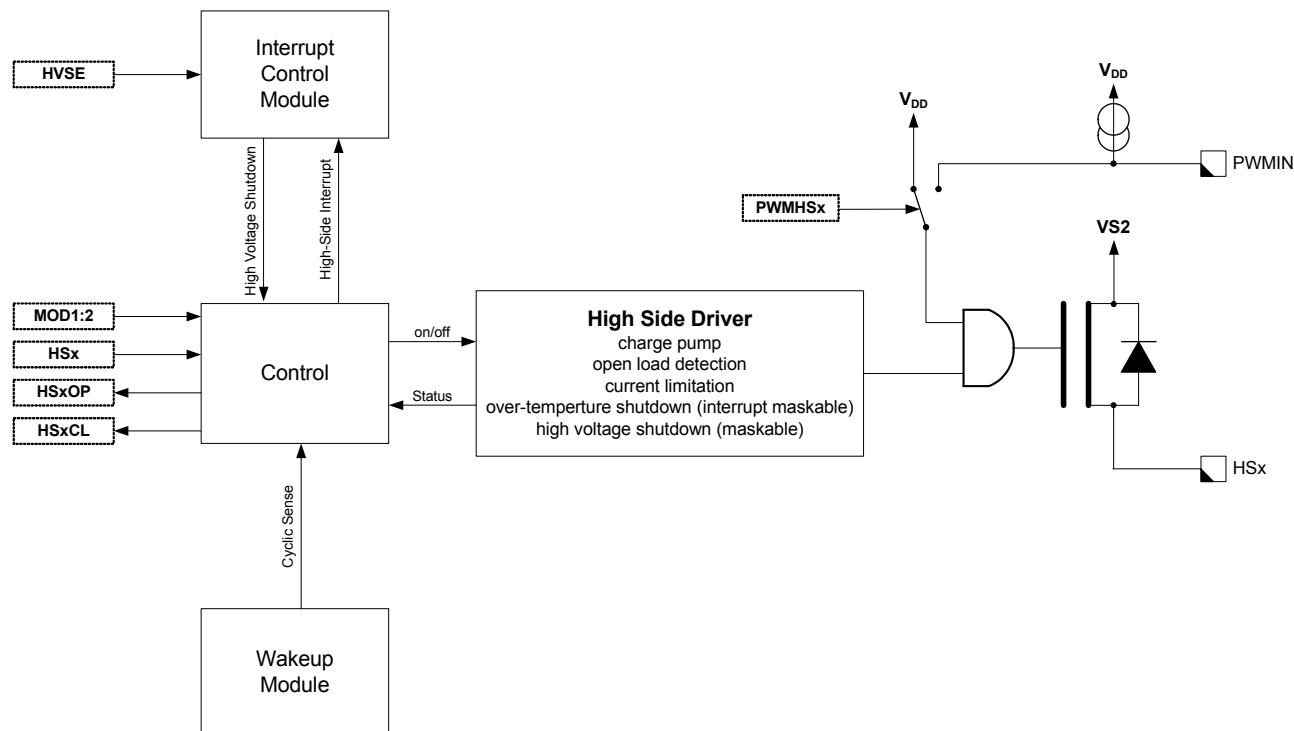


Figure 17. High Side Drivers HS1 and HS2

Open Load Detection

Each high side driver signals an open load condition if the current through the high side is below the open load current threshold.

The open load condition is indicated with the bits HS1OP and HS2OP in the High Side Status Register (HSSR).

Current Limitation

Each high side driver has an output current limitation. In combination with the over-temperature shutdown the high-side drivers are protected against over-current and short-circuit failures.

When the driver operates in the current limitation area, it is indicated with the bits HS1CL and HS2CL in the HSSR.

Note: If the driver is operating in current limitation mode, excessive power might be dissipated.

Over-temperature Protection (HS Interrupt)

Both high side drivers are protected against over-temperature. In case of an over-temperature condition both high side drivers are shut down and the event is latched in the Interrupt Control Module. The shutdown is indicated as HS Interrupt in the Interrupt Source Register (ISR).

A thermal shutdown of the high side drivers is indicated by setting all HSxOP and HSxCL bits simultaneously.

If the bit HSM is set in the Interrupt Mask Register (IMR), then an interrupt (IRQ) is generated.

A write to the High Side Control Register (HSCR), when the over-temperature condition is gone, will re-enable the high side drivers.

High-voltage Shutdown

In case of a high voltage condition and if the high voltage shutdown is enabled (bit HVSE in the Mode Control Register (MCR) is set both high side drivers are shut down.

A write to the High Side Control Register (HSCR), when the high voltage condition is gone, will re-enable the high side drivers.

Sleep And Stop Mode

The high side drivers can be enabled to operate in Sleep and Stop mode for cyclic sensing. Also see [Table 6. Operating Modes Overview](#).

LIN PHYSICAL LAYER

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification and has the following features:

- LIN physical layer 2.0, 2.1 and SAEJ2602 compliant
- Slew rate selection
- Over-temperature shutdown
- Advanced diagnostics

The LIN driver is a low side MOSFET with thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are

required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slopes is guaranteed.

LIN Pin

The LIN pin offers a high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

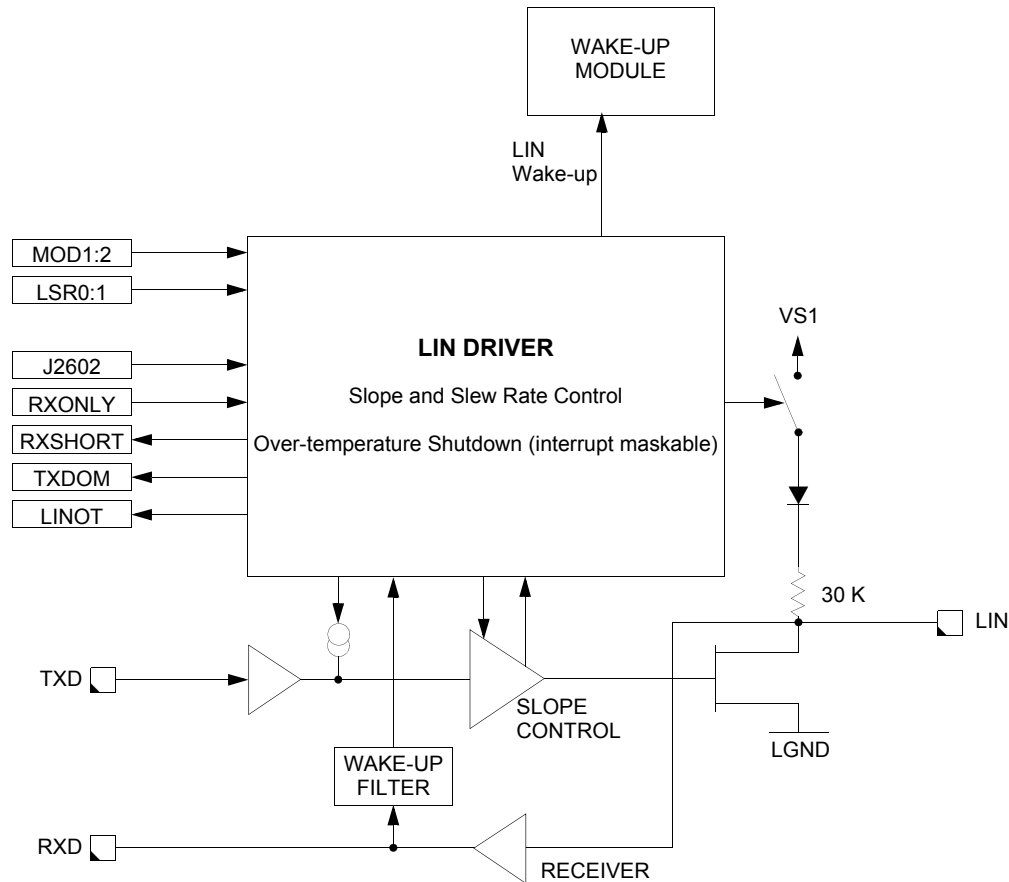


Figure 18. LIN Interface

Slew Rate Selection

The slew rate can be selected for optimized operation at 10.4 and 20 kBit/s as well as a fast baud rate for test and programming. The slew rate can be adapted with the bits LSR1:0 in the LIN Control Register (LINCR). The initial slew rate is optimized for 20 kBit/s.

J2602 Conformance

To be compliant with the SAE J2602-2 specification, the J2602 feature has to be enabled in the LINCR Register (bit DIS_J2602 sets to 0). The LIN transmitter is disabled in case of a V_{SUP} under-voltage condition occurs and TXD is in Recessive State: the LIN bus goes in Recessive State and RXD goes high. The LIN transmitter is not disabled if TXD is in Dominant State. A deglitcher on V_{SUP} (t_{J2602_DEG}) is implemented to avoid false switching.

If the (DIS_J2602) bit is set to 1, the J2602 feature is disabled and the communication TXD-LIN-RXD works for

V_{SUP} down to 4.6 V (typical value) and then the communication is interrupted.

The (DIS_J2602) bit is set per default to 0.

Over-temperature Shutdown (LIN Interrupt)

The output low side FET is protected against over-temperature conditions. In case of an over-temperature condition, the transmitter will be shut down and the LINOT bit in the LIN Status Register (LINSR) is set.

If the LINM bit is set in the Interrupt Mask Register (IMR), an Interrupt IRQ will be generated.

The transmitter is automatically re-enabled once the condition is gone and TXD is high.

RXD Short-circuit Detection (LIN Interrupt)

The LIN transceiver has a short-circuit detection for the RXD output pin. If the device transmits and in case of a short-circuit condition, either 5.0 V or Ground, the RXSHORT bit in

the LIN Status Register (LINSR) is set and the transmitter is shut down.

If the LINM bit is set in the Interrupt Mask Register (IMR), an Interrupt $\overline{\text{IRQ}}$ will be generated.

The transmitter is automatically re-enabled once the condition is gone (transition on RXD) and TXD is high.

A read of the LIN Status Register (LINSR) without the RXD pin short-circuit condition will clear the bit RXSHORT.

TXD Dominant Detection (LIN Interrupt)

The LIN transceiver monitors the TXD input pin to detect a stuck in dominant (0 V) condition. In case of a stuck condition (TXD pin 0 V for more than 1 second (typ.)), the transmitter is shut down and the TXDOM bit in the LIN Status Register (LINSR) is set.

If the LINM bit is set in the IMR, an Interrupt $\overline{\text{IRQ}}$ will be generated.

The transmitter is automatically re-enabled once TXD is high.

A read of the LIN Status Register (LINSR) with the TXD pin at 5.0 V will clear the bit TXDOM.

LIN Receiver Operation Only

While in Normal mode, the activation of the RXONLY bit disables the LIN TXD driver. In case of a LIN error condition, this bit is automatically set. If Stop mode is selected with this bit set, the LIN wake-up functionality is disabled and the RXD pin will reflect the state of the LIN bus.

STOP Mode And Wake-up Feature

During Stop mode operation, the transmitter of the physical layer is disabled. The receiver is still active and able to detect wake-up events on the LIN bus line.

A dominant level longer than T_{PROPWL} followed by a rising edge will generate a wake-up interrupt, and will be reported in the Interrupt Source Register (ISR). Also see [Figure 11](#).

SLEEP Mode And Wake-up Feature

During Sleep mode operation, the transmitter of the physical layer is disabled. The receiver must be active to detect wake-up events on the LIN bus line.

A dominant level longer than T_{PROPWL} followed by a rising edge will generate a system wake-up (Reset), and will be reported in the Interrupt Source Register (ISR). Also see [Figure 10](#).

LOGIC COMMANDS AND REGISTERS**33910 SPI INTERFACE AND CONFIGURATION**

The serial peripheral interface creates the communication link between a microcontroller (master) and the 33910.

The interface consists of four pins (see [Figure 19](#)):

- $\overline{\text{CS}}$ —Chip Select
- MOSI—Master-out Slave-in

- MISO—Master-in Slave-out
- SCLK—Serial Clock

A complete data transfer via the SPI consists of 1 byte. The master sends 4 bits of address (A3:A0) + 4 bits of control information (C3:C0) and the slave replies with 4 system status bits (VMS,LINS,HSS,n.d.) + 4 bits of status information (S3:S0).

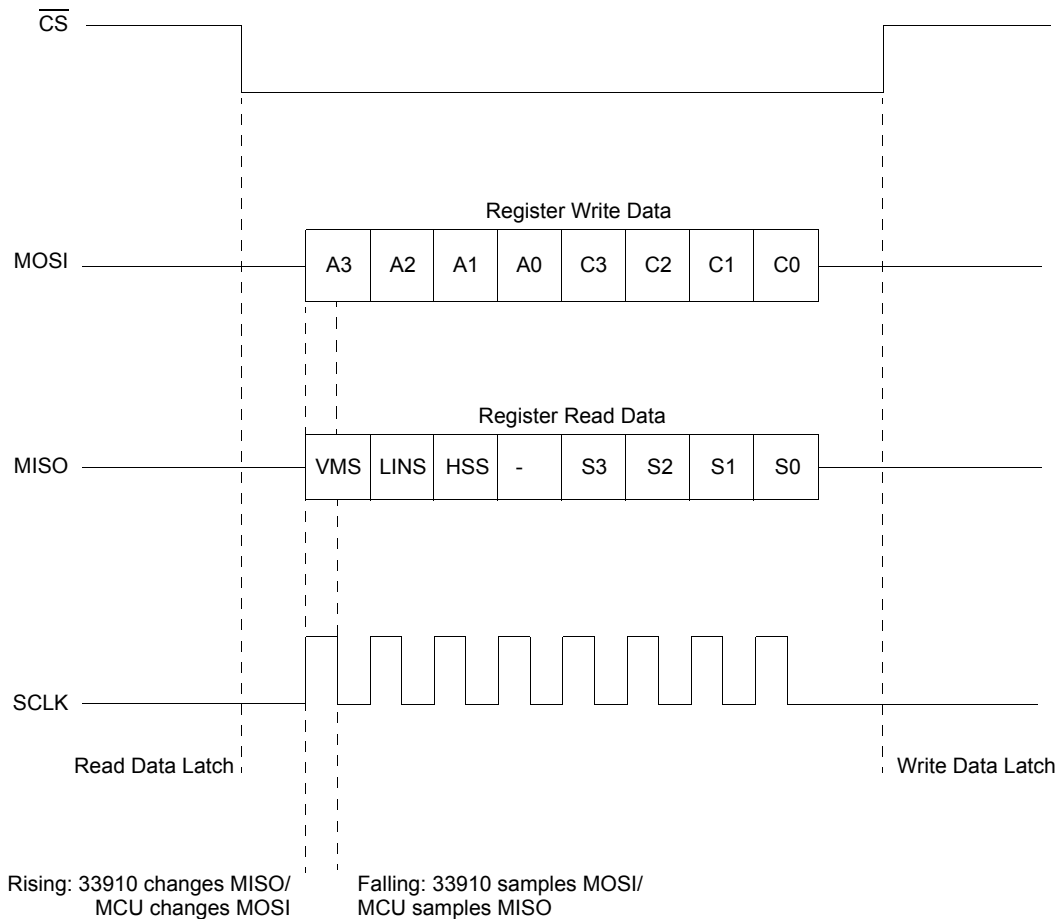


Figure 19. SPI Protocol

During the inactive phase of the $\overline{\text{CS}}$ (HIGH), the new data transfer is prepared.

The falling edge of the $\overline{\text{CS}}$ indicates the start of a new data transfer and puts the MISO in the low-impedance state and latches the analog status data (Register read data).

With the rising edge of the SPI clock (SCLK), the data is moved to MISO/MOSI pins. With the falling edge of the SPI clock (SCLK), the data is sampled by the receiver.

The data transfer is only valid if exactly 8 sample clock edges are present during the active (low) phase of $\overline{\text{CS}}$.

The rising edge of the Chip Select $\overline{\text{CS}}$ indicates the end of the transfer and latches the write data (MOSI) into the register. The $\overline{\text{CS}}$ high forces MISO to the high-impedance state.

Register reset values are described along with the reset condition. Reset condition is the condition causing the bit to be set to its reset value. The main reset conditions are:

- Power-On Reset (POR): the level at which the logic is reset and BATFAIL flag sets.
- Reset mode
- Reset done by the $\overline{\text{RST}}$ pin (ext_reset)

SPI REGISTER OVERVIEW

Table 8. System Status Register

| Adress(A3:A0) | Register Name / Read/Write Information | | BIT | | | |
|---------------|--|---|-----|------|-----|---|
| | | | 7 | 6 | 5 | 4 |
| \$0 - \$F | SYSSR - System Status Register | R | VMS | LINS | HSS | - |

[Table 9](#) summarizes the SPI Register content for Control Information (C3:C0)=W and status information (S3:S0) = R.

Table 9. SPI Register Overview

| Adress(A3:A0) | Register Name / Read/Write Information | | BIT | | | |
|---------------|--|---|-----------|--------|-------|---------|
| | | | 3 | 2 | 1 | 0 |
| \$0 | MCR - Mode Control Register | W | HVSE | 0 | MOD2 | MOD1 |
| | VSR - Voltage Status Register | R | VSOV | VSUV | VDDOT | BATFAIL |
| \$1 | VSR - Voltage Status Register | R | VSOV | VSUV | VDDOT | BATFAIL |
| \$2 | WUCR - Wake-up Control Register | W | 0 | 0 | 0 | L1WE |
| | WUSR - Wake-up Status Register | R | - | - | - | L1 |
| \$3 | WUSR - Wake-up Status Register | R | - | - | - | L1 |
| \$4 | LINCR - LIN Control Register | W | DIS_J2602 | RXONLY | LSR1 | LSR0 |
| | LINSR - LIN Status Register | R | RXSHORT | TXDOM | LINOT | 0 |
| \$5 | LINSR - LIN Status Register | R | RXSHORT | TXDOM | LINOT | 0 |
| \$6 | HSCR - High Side Control Register | W | PWMHS2 | PWMHS1 | HS2 | HS1 |
| | HSSR - High Side Status Register | R | HS2OP | HS2CL | HS1OP | HS1CL |
| \$7 | HSSR - High Side Status Register | R | HS2OP | HS2CL | HS1OP | HS1CL |
| \$A | TIMCR - Timing Control Register | W | CS/WD | WD2 | WD1 | WD0 |
| | WDSR - Watchdog Status Register | R | | CYST2 | CYST1 | CYST0 |
| \$B | WDSR - Watchdog Status Register | R | WDTO | WDERR | WDOFF | WDWO |
| \$C | AMUXCR - Analog Multiplexer Control Register | W | L1DS | MX2 | MX1 | MX0 |
| \$D | CFR - Configuration Register | W | HVDD | CYSX8 | 0 | 0 |
| \$E | IMR - Interrupt Mask Register | W | HSM | 0 | LINM | VMM |
| | ISR - Interrupt Source Register | R | ISR3 | ISR2 | ISR1 | ISR0 |
| \$F | ISR - Interrupt Source Register | R | ISR3 | ISR2 | ISR1 | ISR0 |

REGISTER DEFINITIONS

System Status Register - SYSSR

The System Status Register (SYSSR) is always transferred with every SPI transmission and gives a quick system status overview. It summarizes the status of the Voltage Monitor Status (VMS), LIN Status (LINS) and High Side Status (HSS).

Table 10. System Status Register

| | S7 | S6 | S5 | S4 |
|------|-----|------|-----|----|
| Read | VMS | LINS | HSS | - |

VMS - Voltage Monitor Status

This read-only bit indicates that one or more bits in the VSR are set.

1 = Voltage Monitor bit set

0 = None

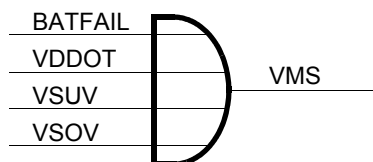


Figure 20. Voltage Monitor Status

LINS - LIN Status

This read-only bit indicates that one or more bits in the LINSR are set.

1 = LIN Status bit set

0 = None

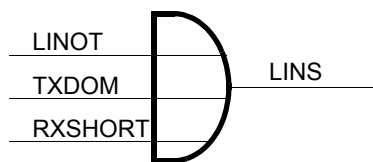


Figure 21. LIN Status

HSS - High Side Switch Status

This read-only bit indicates that one or more bits in the HSSR are set.

1 = High Side Status bit set

0 = None

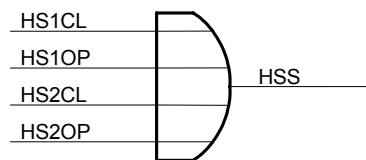


Figure 22. High Side Status

Mode Control Register - MCR

The Mode Control Register (MCR) allows switching between the operation modes and to configure the 33910. Writing the MCR will return the VSR.

Table 11. Mode Control Register - \$0

| | C3 | C2 | C1 | C0 |
|-----------------|------|-----|------|------|
| Write | HVSE | 0 | MOD2 | MOD1 |
| Reset Value | 1 | 0 | - | - |
| Reset Condition | POR | POR | - | - |

HVSE - High-Voltage Shutdown Enable

This write-only bit enables/disables automatic shutdown of the high side drivers during a high-voltage VSOV condition.

1 = automatic shutdown enabled

0 = automatic shutdown disabled

MOD2, MOD1 - Mode Control Bits

These write-only bits select the operating mode and allow clearing the watchdog in accordance with [Table 8](#), Mode Control Bits.

Table 12. Mode Control Bits

| MOD2 | MOD1 | Description |
|------|------|------------------------------|
| 0 | 0 | Normal Mode |
| 0 | 1 | Stop Mode |
| 1 | 0 | Sleep Mode |
| 1 | 1 | Normal Mode + Watchdog Clear |

Voltage Status Register - VSR

Returns the status of the several voltage monitors. This register is also returned when writing to the Mode Control Register (MCR).

Table 13. Voltage Status Register - \$0/\$1

| | S3 | S2 | S1 | S0 |
|------|------|------|-------|---------|
| Read | VSOV | VSUV | VDDOT | BATFAIL |

VSOV - V_{SUP} Over-voltage

This read-only bit indicates an over-voltage condition on the VS1 pin.

1 = Over-voltage condition.

0 = Normal condition.

VSUV - V_{SUP} Under-voltage

This read-only bit indicates an under-voltage condition on the VS1 pin.

1 = Under-voltage condition.

0 = Normal condition.

VDDOT - Main Voltage Regulator Over-temperature Warning

This read-only bit indicates that the main voltage regulator temperature reached the Over-temperature Prewarning Threshold.

1 = Over-temperature Prewarning

0 = Normal

BATFAIL - Battery Fail Flag.

This read-only bit is set during power-up and indicates that the 33910 had a Power-On-Reset (POR).

Any access to the MCR or VSR will clear the BATFAIL flag.

1 = POR Reset has occurred

0 = POR Reset has not occurred

Wake-up Control Register - WUCR

This register is used to control the digital wake-up input. Writing the WUCR will return the Wake-Up Status Register (WUSR).

Table 14. Wake-up Control Register - \$2

| | C3 | C2 | C1 | C0 |
|-----------------|------------------------------|----|----|------|
| Write | 0 | 0 | 0 | L1WE |
| Reset Value | 1 | 1 | 1 | 1 |
| Reset Condition | POR, Reset mode or ext_reset | | | |

L1WE - Wake-up Input Enable

This write-only bit enables/disables the L1 input. In Stop and Sleep mode the L1WE bit activates the L1 input for wake-up. If the L1 input is selected on the analog multiplexer, the L1WE is masked to 0.

1 = Wake-up Input enabled.

0 = Wake-up Input disabled.

Wake-up Status Register - WUSR

This register is used to monitor the digital wake-up input and is also returned when writing to the WUCR.

Table 15. Wake-up Status Register - \$2/\$3

| | S3 | S2 | S1 | S0 |
|------|----|----|----|----|
| Read | - | - | - | L1 |

L1 - Wake-up input 1

This read-only bit indicates the status of the L1 input. If the L1 input is not enabled, then the Wake-up status will return 0.

After a wake-up from Stop or Sleep mode this bit also allows to verify the L1 input has caused the wake-up, by first reading the Interrupt Status Register (ISR) and then reading the WUSR. The source of the wake-up is only reported on the first WUCR or WUSR access.

1 = L1 pin high, or L1 is the source of the wake-up.

0 = L1 pin low, disabled or selected as an analog input.

LIN Control Register - LINCR

This register controls the LIN physical interface block. Writing the LIN Control Register (LINCR) returns the LIN Status Register (LINSR).

Table 16. LIN Control Register - \$4

| | C3 | C2 | C1 | C0 |
|-----------------|-----------|---|------|------|
| Write | DIS_J2602 | RXONLY | LSR1 | LSR0 |
| Reset Value | 0 | 0 | 0 | 0 |
| Reset Condition | POR | POR, Reset mode, ext_reset or LIN failure gone* | POR | |

* LIN failure gone: if LIN failure (overtemp, TXD/RXD short) was set, the flag resets automatically when the failure is gone.

J2602 - LIN Dominant Voltage Select

This write-only bit controls the J2602 circuitry. If the circuitry is enabled (bit sets to 0), the TXD-LIN-RXD communication works down to the battery under-voltage condition is detected. Below, the bus is in recessive state. If the circuitry is disabled (bit sets to 1), the communication TXD-LIN-RXD works down to 4.6 V (typical value).

0 = Enabled J2602 feature.

1 = Disabled J2602 feature.

RXONLY - LIN Receiver Operation Only

This write-only bit controls the behavior of the LIN transmitter.

In Normal mode, the activation of the RXONLY bit disables the LIN transmitter. In case of a LIN error condition, this bit is automatically set.

In Stop mode this bit disables the LIN wake-up functionality, and the RXD pin will reflect the state of the LIN bus.

1 = only LIN receiver active (Normal mode) or LIN wake-up disabled (Stop mode).

0 = LIN fully enabled.

LSRx - LIN Slew-Rate

This write-only bit controls the LIN driver slew-rate in accordance with [Table 18](#).

Table 17. LIN Slew Rate Control

| LSR1 | LSR0 | Description |
|------|------|----------------------------------|
| 0 | 0 | Normal Slew Rate (up to 20 kb/s) |
| 0 | 1 | Slow Slew Rate (up to 10 kb/s) |
| 1 | 0 | Fast Slew Rate (up to 100 kb/s) |
| 1 | 1 | Reserved |

LIN Status Register - LINSR

This register returns the status of the LIN physical interface block and is also returned when writing to the LINCR.

Table 18. LIN Status Register - \$4/\$5

| | S3 | S2 | S1 | S0 |
|------|---------|-------|-------|----|
| Read | RXSHORT | TXDOM | LINOT | 0 |

RXSHORT - RXD Pin Short-circuit

This read-only bit indicates a short-circuit condition on the RXD pin (shorted either to 5.0 V or to Ground). The short-circuit delay must be a worst case of 8.0 μ s to be detected and to shut down the driver. To clear this bit, it must be read after the condition is gone (transition detected on RXD pin). The LIN driver is automatically re-enabled once the condition is gone and TXD is high.

1 = RXD short-circuit condition.

0 = None.

TXDOM - TXD Permanent Dominant

This read-only bit signals the detection of a TXD pin stuck at dominant (Ground) condition and the resultant shutdown in the LIN transmitter. This condition is detected after the TXD pin remains in dominant state for more than 1 second (typical value).

To clear this bit, it must be read after TXD has gone high. The LIN driver is automatically re-enabled once TXD goes High.

1 = TXD stuck at dominant fault detected.

0 = None.

LINOT - LIN Driver Over-temperature

This read-only bit signals that the LIN transceiver was shutdown due to over-temperature. The transmitter is automatically re-enabled after the over-temperature condition is gone and TXD is high. The LINOT bit is cleared after SPI read once the condition is gone.

1 = LIN over-temperature shutdown

0 = None

High Side Control Register - HSCR

This register controls the operation of the high side drivers. Writing to this register returns the High Side Status Register (HSSR).

Table 19. High Side Control Register - \$6

| | C3 | C2 | C1 | C0 |
|-----------------|--------|--------|--|-----|
| Write | PWMHS2 | PWMHS1 | HS2 | HS1 |
| Reset Value | 0 | 0 | 0 | 0 |
| Reset Condition | POR | | POR, Reset mode, ext_reset, HSx over-temp or (VSOV & HVSE) | |

PWMHSx - PWM Input Control Enable.

This write-only bit enables/disables the PWMIN input pin to control the respective high side switch. The corresponding high side switch must be enabled (HSx bit).

1 = PWMIN input controls HSx output.

0 = HSx is controlled only by SPI.

HSx - HSx Switch Control.

This write-only bit enables/disables the corresponding high side switch.

1 = HSx switch on.

0 = HSx switch off.

High Side Status Register - HSSR

This register returns the status of the high side switches and is also returned when writing to the HSCR.

Table 20. High Side Status Register - \$6/\$7

| | S3 | S2 | S1 | S0 |
|------|-------|-------|-------|-------|
| Read | HS2OP | HS2CL | HS1OP | HS1CL |

High Side thermal shutdown

A thermal shutdown of the high side drivers is indicated by setting all HSxOP and HSxCL bits simultaneously.

HSxOP - High Side Switch Open-Load Detection

This read-only bit signals that the high side switches are conducting current below a certain threshold indicating possible load disconnection.

1 = HSx Open Load detected (or thermal shutdown)

0 = Normal

HSxCL - High Side Current Limitation

This read-only bit indicates that the respective high side switch is operating in current limitation mode.

1 = HSx in current limitation (or thermal shutdown)

0 = Normal

Timing Control Register - TIMCR

This register allows to configure the watchdog, the cyclic sense and Forced Wake-up periods. Writing to the Timing Control Register (TIMCR) will also return the Watchdog Status Register (WDSR).

Table 21. Timing Control Register - \$A

| | C3 | C2 | C1 | C0 |
|-----------------|---------------------|-------|-------|-------|
| Write | CS/ \overline{WD} | WD2 | WD1 | WD0 |
| | | CYST2 | CYST1 | CYST0 |
| Reset Value | - | 0 | 0 | 0 |
| Reset Condition | - | POR | | |

 $\overline{CS}/\overline{WD}$ - Cyclic Sense or Watchdog prescaler select

This write-only bit selects which prescaler is being written to, the Cyclic Sense/Forced Wake-up prescaler or the Watchdog prescaler.

1 = Cyclic Sense/Forced Wake-up Prescaler selected

0 = Watchdog Prescaler select

WDx - Watchdog Prescaler

This write-only bits selects the divider for the watchdog prescaler and therefore selects the watchdog period in accordance with [Table 22](#). This configuration is valid only if windowing watchdog is active.

Table 22. Watchdog Prescaler

| WD2 | WD1 | WD0 | Prescaler Divider |
|-----|-----|-----|-------------------|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 6 |
| 1 | 0 | 0 | 8 |
| 1 | 0 | 1 | 10 |
| 1 | 1 | 0 | 12 |
| 1 | 1 | 1 | 14 |

CYSTx - Cyclic Sense Period Prescaler Select

This write-only bits selects the interval for the wake-up cyclic sensing together with the bit CYSX8 in the Configuration Register (CFR) (see page [44](#)).

This option is only active if one of the high side switches is enabled when entering in Stop or Sleep mode. Otherwise, a timed wake-up is performed after the period shown in [Table 23](#).

Table 23. Cyclic Sense and Force Wake-up Interval

| CYSX8 ⁽⁶⁶⁾ | CYST2 | CYST1 | CYST0 | Interval |
|-----------------------|-------|-------|-------|---------------------------------|
| X | 0 | 0 | 0 | No cyclic sense ⁽⁶⁷⁾ |
| 0 | 0 | 0 | 1 | 20 ms |
| 0 | 0 | 1 | 0 | 40 ms |
| 0 | 0 | 1 | 1 | 60 ms |
| 0 | 1 | 0 | 0 | 80 ms |
| 0 | 1 | 0 | 1 | 100 ms |
| 0 | 1 | 1 | 0 | 120 ms |
| 0 | 1 | 1 | 1 | 140 ms |
| 1 | 0 | 0 | 1 | 160 ms |
| 1 | 0 | 1 | 0 | 320 ms |
| 1 | 0 | 1 | 1 | 480 ms |
| 1 | 1 | 0 | 0 | 640 ms |
| 1 | 1 | 0 | 1 | 800 ms |
| 1 | 1 | 1 | 0 | 960 ms |
| 1 | 1 | 1 | 1 | 1120 ms |

Notes

66. bit CYSX8 is located in Configuration Register (CFR)
 67. No Cyclic Sense and no Force Wake-up available.

Watchdog Status Register - WDSR

This register returns the Watchdog status information and is also returned when writing to the TIMCR.

Table 24. Watchdog Status Register - \$A/\$B

| | S3 | S2 | S1 | S0 |
|------|------|-------|-------|------|
| Read | WDTO | WDERR | WDOFF | WDWO |

WDTO - Watchdog Timeout

This read-only bit signals the last reset was caused by either a watchdog timeout or by an attempt to clear the Watchdog within the window closed.

Any access to this register or the Timing Control Register (TIMCR) will clear the WDTO bit.

- 1 = Last reset caused by watchdog timeout
 0 = None

WDERR - Watchdog Error

This read-only bit signals the detection of a missing watchdog resistor. In this condition the watchdog is using the internal, lower precision timebase. The Windowing function is disabled.

- 1 = WDCONF pin resistor missing
 0 = WDCONF pin resistor not floating

WDOFF - Watchdog Off

This read-only bit signals that the watchdog pin connected to Ground and therefore disabled. In this case watchdog

timeouts are disabled and the device automatically enters Normal mode out of Reset. This might be necessary for software debugging and for programming the Flash memory.

- 1 = Watchdog is disabled
 0 = Watchdog is enabled

WDWO - Watchdog Window Open

This read-only bit signals when the watchdog window is open for clears. The purpose of this bit is for testing. Should be ignored in case WDERR is High.

- 1 = Watchdog window open
 0 = Watchdog window closed

Analog Multiplexer Control Register - MUXCR

This register controls the analog multiplexer and selects the divider ration for the L1 input divider.

Table 25. Analog Multiplexer Control Register - \$C

| | C3 | C2 | C1 | C0 |
|-----------------|------|------------------------------|-----|-----|
| Write | L1DS | MX2 | MX1 | MX0 |
| Reset Value | 1 | 0 | 0 | 0 |
| Reset Condition | POR | POR, Reset mode or ext_reset | | |

L1DS - L1 Analog Input Divider Select

This write-only bit selects the resistor divider for the L1 analog input. Voltage is internally clamped to VDD.

- 0 = L1 Analog divider: 1
 1 = L1 Analog divider: 3.6 (typ.)

MXx - Analog Multiplexer Input Select

These write-only bits selects which analog input is multiplexed to the ADOUT0 pin according to [Table 26](#).

When disabled or when in Stop or Sleep mode, the output buffer is not powered and the ADOUT0 output is left floating to achieve lower current consumption.

Table 26. Analog Multiplexer Channel Select

| MX2 | MX1 | MX0 | Meaning |
|-----|-----|-----|------------------------|
| 0 | 0 | 0 | Disabled |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Die Temperature Sensor |
| 0 | 1 | 1 | VSENSE input |
| 1 | 0 | 0 | L1 input |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

Configuration Register - CFR

This register controls the Hall Sensor Supply enable/disable and the cyclic sense timing multiplier.

Table 27. Configuration Register - \$D

| | C3 | C2 | C1 | C0 |
|-----------------|------------------------------|-------|-----|-----|
| Write | HVDD | CYSX8 | 0 | 0 |
| Reset Value | 0 | 0 | 0 | 0 |
| Reset Condition | POR, Reset mode or ext_reset | POR | POR | POR |

HVDD - Hall Sensor Supply Enable

This write-only bit enables/disables the state of the hall sensor supply.

1 = HVDD on

0 = HVDD off

CYSX8 - Cyclic Sense Timing x 8.

This write-only bit influences the cyclic sense and Forced Wake-up period as shown in [Table 23](#).

1 = Multiplier enabled

0 = None

Interrupt Mask Register - IMR

This register allows masking of some of the interrupt sources. No interrupt will be generated to the MCU and no flag will be set in the ISR register. The 5.0V Regulator over-temperature prewarning interrupt and Under-voltage (VSUV) interrupts can not be masked and will always cause an interrupt.

Writing to the IMR will return the ISR.

Table 28. Interrupt Mask Register - \$E

| | C3 | C2 | C1 | C0 |
|-----------------|-----|----|------|-----|
| Write | HSM | 0 | LINM | VMM |
| Reset Value | 1 | 1 | 1 | 1 |
| Reset Condition | POR | | | |

HSM - High Side Interrupt Mask

This write-only bit enables/disables interrupts generated in the high side block.

1 = HS Interrupts Enabled

0 = HS Interrupts Disabled

LINM - LIN Interrupts Mask

This write-only bit enables/disables interrupts generated in the LIN block.

1 = LIN Interrupts Enabled

0 = LIN Interrupts Disabled

VMM - Voltage Monitor Interrupt Mask

This write-only bit enables/disables interrupts generated in the Voltage Monitor block. The only maskable interrupt in the Voltage Monitor Block is the V_{SUP} over-voltage interrupt.

1 = Interrupts Enabled

0 = Interrupts Disabled

Interrupt Source Register - ISR

This register allows the MCU to determine the source of the last interrupt or wake-up respectively. A read of the register acknowledges the interrupt and leads IRQ pin to high, in case there are no other pending interrupts. If there are pending interrupts, IRQ will be driven high for 10 μ s and then be driven low again.

This register is also returned when writing to the Interrupt Mask Register (IMR).

Table 29. Interrupt Source Register - \$E/\$F

| | S3 | S2 | S1 | S0 |
|------|------|------|------|------|
| Read | ISR3 | ISR2 | ISR1 | ISR0 |

ISR_x - Interrupt Source Register

These read-only bits indicate the interrupt source following [Table 30](#). If no interrupt is pending then all bits are 0.

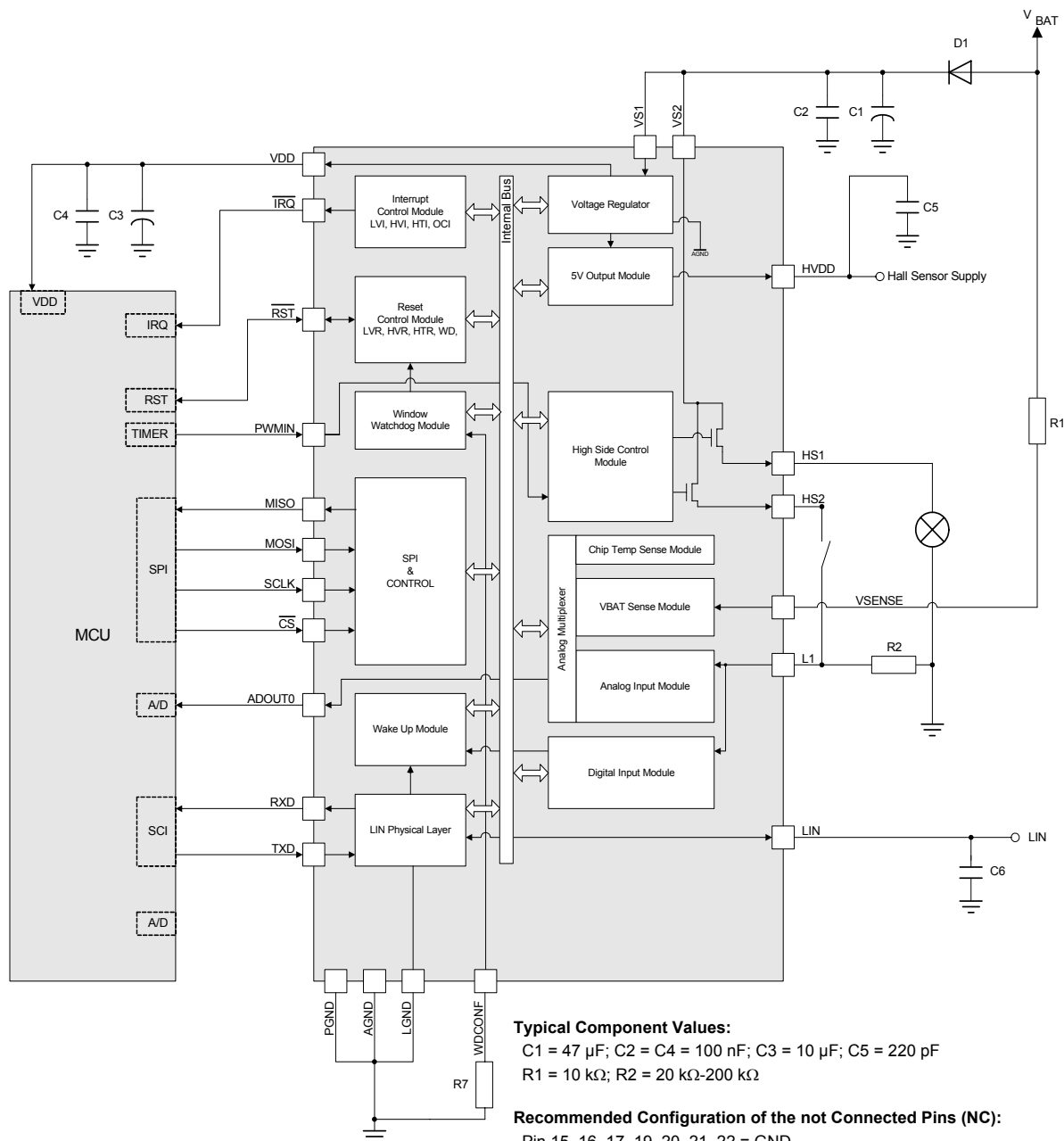
In case more than one interrupt is pending, the interrupt sources are handled sequentially multiplex.

Table 30. Interrupt Sources

| ISR3 | ISR2 | ISR1 | ISR0 | Interrupt Source | | Priority |
|------|------|------|------|---|---|----------|
| | | | | none maskable | maskable | |
| 0 | 0 | 0 | 0 | no interrupt | no interrupt | none |
| 0 | 0 | 0 | 1 | L1 Wake-up from Stop and Sleep mode | - | highest |
| 0 | 0 | 1 | 0 | - | HS Interrupt (Over-temperature) | |
| 0 | 0 | 1 | 1 | - | Reserved | |
| 0 | 1 | 0 | 0 | LIN Wake-up | LIN Interrupt (RXSHORT, TXDOM, LIN OT) | |
| 0 | 1 | 0 | 1 | Voltage Monitor Interrupt (Low Voltage and VDD over-temperature) | Voltage Monitor Interrupt (High Voltage) | |
| 0 | 1 | 1 | 0 | Forced Wake-up | - | lowest |

TYPICAL APPLICATION

The 33910 can be configured in several applications. The figure below shows the 33910 in the typical Slave Node Application.



MC33911BAC PRODUCT SPECIFICATIONS PAGES 47 TO 86

INTERNAL BLOCK DIAGRAM

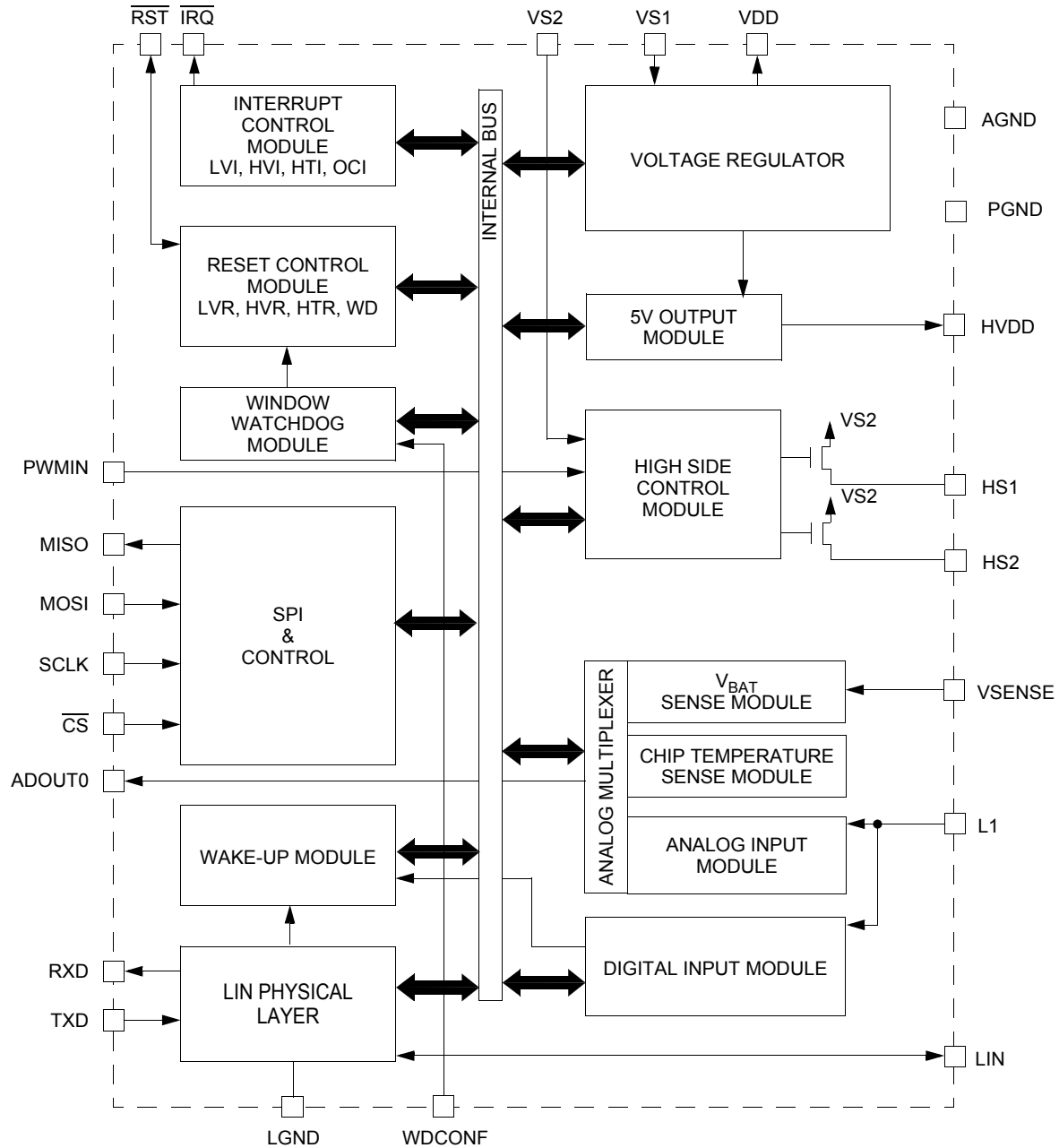


Figure 23. 33910 Simplified Internal Block Diagram

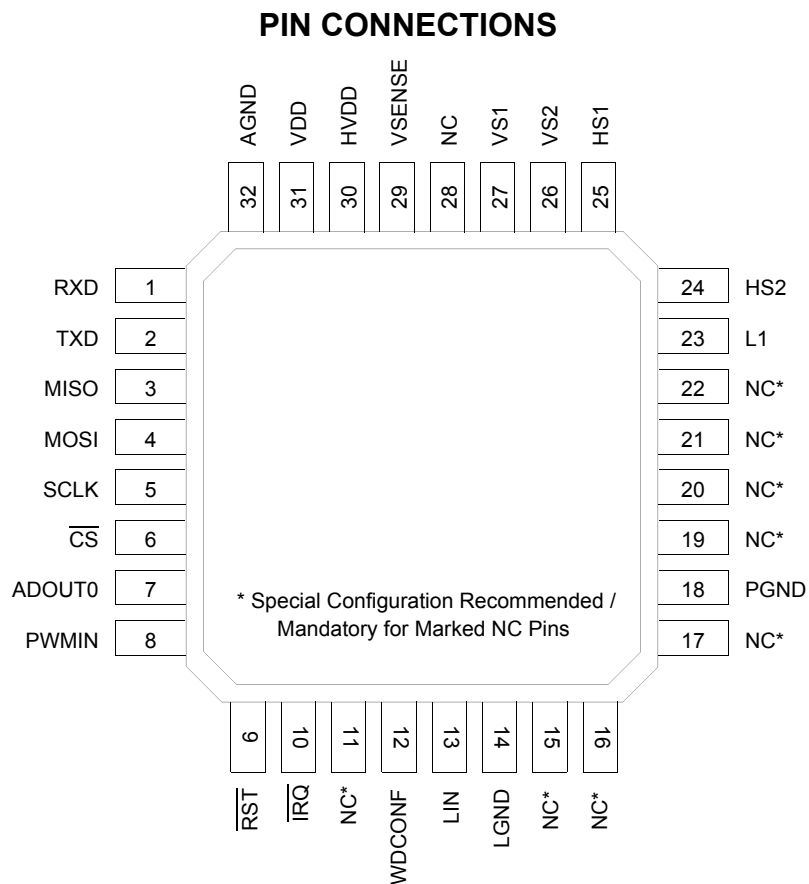


Figure 24. 33910 Pin Connections

Table 31. 33910 Pin Definitions

A functional description of each pin can be found in the [Functional Pin Description](#).

| Pin | Pin Name | Formal Name | Definition |
|----------------------|------------------|---------------------------|--|
| 1 | RXD | Receiver Output | This pin is the receiver output of the LIN interface which reports the state of the bus voltage to the MCU interface. |
| 2 | TXD | Transmitter Input | This pin is the transmitter input of the LIN interface which controls the state of the bus output. |
| 3 | MISO | SPI Output | SPI data output. When \overline{CS} is high, the pin is in the high-impedance state. |
| 4 | MOSI | SPI Input | SPI data input. |
| 5 | SCLK | SPI Clock | SPI clock Input. |
| 6 | \overline{CS} | SPI Chip Select | SPI chip select input pin. \overline{CS} is active low. |
| 7 | ADOUT0 | Analog Output Pin 0 | Analog multiplexer output. |
| 8 | PWMIN | PWM Input | High side pulse width modulation input. |
| 9 | \overline{RST} | Internal Reset I/O | Bidirectional reset I/O pin - driven low when any internal reset source is asserted. \overline{RST} is active low. |
| 10 | \overline{IRQ} | Internal Interrupt Output | Interrupt output pin, indicating wake-up events from Stop mode or events from Normal and Normal Request modes. \overline{IRQ} is active low. |
| 11, 15-17, 19-22, 28 | NC | | No connect |

Table 31. 33910 Pin Definitions

A functional description of each pin can be found in the [Functional Pin Description](#).

| Pin | Pin Name | Formal Name | Definition |
|--------|----------|----------------------------|---|
| 12 | WDCONF | Watchdog Configuration Pin | This input pin is for configuration of the watchdog period and allows the disabling of the watchdog. |
| 13 | LIN | LIN Bus | This pin represents the single-wire bus transmitter and receiver. |
| 14 | LGND | LIN Ground Pin | This pin is the device LIN ground connection. It is internally connected to the PGND pin. |
| 18 | PGND | Power Ground Pin | This pin is the device power ground connection. It is internally connected to the LGND pin. |
| 23 | L1 | Wake-up Input | This pin is a wake-up capable digital input ⁽⁶⁸⁾ . In addition, L1 can be sensed analog via the analog multiplexer. |
| 24, 25 | HS2, HS1 | High Side Outputs | High side switch outputs. |
| 26, 27 | VS2, VS1 | Power Supply Pin | These pins are device battery level power supply pins. VS2 is supplying the HS1 driver while VS1 supplies the remaining blocks. ⁽⁶⁹⁾ |
| 29 | VSENSE | Voltage Sense Pin | Battery voltage sense input. ⁽⁷⁰⁾ |
| 30 | HVDD | Hall Sensor Supply Output | +5.0 V switchable supply output pin. ⁽⁷¹⁾ |
| 31 | VDD | Voltage Regulator Output | +5.0 V main voltage regulator output pin. ⁽⁷²⁾ |
| 32 | AGND | Analog Ground Pin | This pin is the device analog ground connection. |

Notes

- 68. When used as digital input, a series 33k Ω resistor must be used to protect against automotive transients.
- 69. Reverse battery protection series diodes must be used externally to protect the internal circuitry.
- 70. This pin can be connected directly to the battery line for voltage measurements. The pin is self protected against reverse battery connections. It is strongly recommended to connect a 10k Ω resistor in series with this pin for protection purposes.
- 71. External capacitor (1.0 μ F < C < 10 μ F; 0.1 Ω < ESR < 5.0 Ω) required.
- 72. External capacitor (2.0 μ F < C < 100 μ F; 0.1 Ω < ESR < 10 Ω) required.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 32. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings | Symbol | Value | Unit |
|---|--|---|------|
| ELECTRICAL RATINGS | | | |
| Supply Voltage at VS1 and VS2 Normal Operation (DC) Transient Conditions (load dump) | $V_{SUP(SS)}$ $V_{SUP(PK)}$ | -0.3 to 27 -0.3 to 40 | V |
| Supply Voltage at VDD | V_{DD} | -0.3 to 5.5 | V |
| Input / Output Pins Voltage ⁽⁷³⁾ \overline{CS} , \overline{RST} , SCLK, PwMIN, ADOUT0, MOSI, MISO, TXD, RXD Interrupt Pin (\overline{IRQ}) ⁽⁷⁴⁾ | V_{IN} $V_{IN(IRQ)}$ | -0.3 to $V_{DD}+0.3$ -0.3 to 11 | V |
| HS1 Pin Voltage (DC) | V_{HS1} | -0.3 to $V_{SUP}+0.3$ | V |
| HS2 Pin Voltage (DC) | V_{HS2} | -0.3 to $V_{SUP}+0.3$ | V |
| L1 Pin Voltage Normal Operation with a series 33 k Ω resistor (DC) Transient input voltage with external component (according to ISO7637-2) (See Figure 26) | V_{L1DC} V_{L1TR} | -18 to 40 ± 100 | V |
| VSENSE Pin Voltage (DC) | V_{VSENSE} | -27 to 40 | V |
| LIN Pin Voltage Normal Operation (DC) Transient input voltage with external component (according to ISO7637-2) (See Figure) | V_{BUSDC} V_{BUSTR} | -18 to 40 -150 to 100 | V |
| VDD output current | I_{VDD} | Internally Limited | A |
| ESD Voltage ⁽⁷⁵⁾ Human Body Model - LIN Pin Human Body Model - all other Pins Machine Model Charge Device Model Corner Pins (Pins 1, 8, 9, 16, 17, 24, 25 and 32) All other Pins (Pins 2-7, 10-15, 18-23, 26-31) | V_{ESD1-1} V_{ESD1-2} V_{ESD2} V_{ESD3-1} V_{ESD3-2} | ± 8000 ± 2000 ± 150 ± 750 ± 500 | V |
| NC Pin Voltage (NC pins 11, 15, 16, 17, 19, 20, 21, 22, and 28) ⁽⁷⁶⁾ | V_{NC} | Note 76 | |

Notes

73. Exceeding voltage limits on specified pins may cause a malfunction or permanent damage to the device.
74. Extended voltage range for programming purpose only.
75. Testing is performed in accordance with the Human Body Model ($C_{ZAP} = 100$ pF, $R_{ZAP} = 1500$ Ω), the Machine Model ($C_{ZAP} = 200$ pF, $R_{ZAP} = 0$ Ω), and the Charge Device Model, Robotic ($C_{ZAP} = 4.0$ pF).
76. Special configuration recommended / mandatory for marked NC pins. Please refer to the typical application.

Table 32. Maximum Ratings (continued)

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings | Symbol | Value | Unit |
|---|-----------------|------------|------|
| THERMAL RATINGS | | | |
| Operating Ambient Temperature ⁽⁷⁷⁾ | T_A | -40 to 125 | °C |
| 33910 34910 | | -40 to 85 | |
| Operating Junction Temperature ⁽⁷⁷⁾ | T_J | -40 to 150 | °C |
| Storage Temperature | T_{STG} | -55 to 150 | °C |
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | | °C/W |
| Natural Convection, Single Layer board (1s) ^{(78), (79)} | | 85 | |
| Natural Convection, Four Layer board (2s2p) ^{(78), (80)} | | 56 | |
| Thermal Resistance, Junction to Case ⁽⁸¹⁾ | $R_{\theta JC}$ | 23 | °C/W |
| Peak Package Reflow Temperature During Reflow ^{(82), (83)} | T_{PPRT} | Note 83 | °C |

Notes

77. The limiting factor is junction temperature; taking into account the power dissipation, thermal resistance, and heat sinking.
78. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
79. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
80. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
81. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
82. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
83. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 33. Static Electrical Characteristics

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_{\text{A}} \leq 125^\circ\text{C}$ for the 33910 and $-40^\circ\text{C} \leq T_{\text{A}} \leq 85^\circ\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---------------------------|------|-------|------|---------------|
| SUPPLY VOLTAGE RANGE (VS1, VS2) | | | | | |
| Nominal Operating Voltage | V_{SUP} | 5.5 | – | 18 | V |
| Functional Operating Voltage ⁽⁸⁴⁾ | V_{SUPOP} | – | – | 27 | V |
| Load Dump | V_{SUPLD} | – | – | 40 | V |
| SUPPLY CURRENT RANGE ($V_{\text{SUP}} = 13.5\text{ V}$) | | | | | |
| Normal Mode (I_{OUT} at $V_{\text{DD}} = 10\text{ mA}$), LIN Recessive State ⁽⁸⁵⁾ | I_{RUN} | – | 4.5 | 10 | mA |
| Stop Mode, VDD ON with $I_{\text{OUT}} = 100\text{ }\mu\text{A}$, LIN Recessive State ^{(85), (86), (87)} $5.5\text{ V} < V_{\text{SUP}} < 12\text{ V}$ $V_{\text{SUP}} = 13.5\text{ V}$ | I_{STOP} | – | 48 | 80 | μA |
| | | – | 58 | 90 | |
| Sleep Mode, VDD OFF, LIN Recessive State ^{(85), (87)} $5.5\text{ V} < V_{\text{SUP}} < 12\text{ V}$ $12\text{ V} \leq V_{\text{SUP}} < 13.5\text{ V}$ | I_{SLEEP} | – | 27 | 35 | μA |
| | | – | 37 | 48 | |
| Cyclic Sense Supply Current Adder ⁽⁸⁸⁾ | I_{CYCLIC} | – | 10 | – | μA |
| SUPPLY UNDER/OVER-VOLTAGE DETECTIONS | | | | | |
| Power-On Reset (BATFAIL) ⁽⁸⁹⁾ Threshold (measured on VS1) ⁽⁸⁸⁾ Hysteresis (measured on VS1) ⁽⁸⁸⁾ | V_{BATFAIL} | 1.5 | 3.0 | 3.9 | V |
| | $V_{\text{BATFAIL_HYS}}$ | – | 0.9 | – | |
| | | | | | |
| V_{SUP} under-voltage detection (VSUV Flag) (Normal and Normal Request modes, Interrupt Generated) Threshold (measured on VS1) Hysteresis (measured on VS1) | V_{SUUV} | 5.55 | 6.0 | 6.6 | V |
| | $V_{\text{SUUV_HYS}}$ | – | 1.0 | – | |
| V_{SUP} over-voltage detection (VSOV Flag) (Normal and Normal Request modes, Interrupt Generated) Threshold (measured on VS1) Hysteresis (measured on VS1) | V_{SOV} | 18 | 19.25 | 20.5 | V |
| | $V_{\text{SOV_HYS}}$ | – | 1.0 | – | |

Notes

84. Device is fully functional. All features are operating.
85. Total current ($I_{\text{VS1}} + I_{\text{VS2}}$) measured at GND pins excluding all loads, Cyclic Sense disabled.
86. Total I_{DD} current (including loads) below $100\text{ }\mu\text{A}$.
87. Stop and Sleep mode currents will increase if V_{SUP} exceeds 13.5 V .
88. This parameter is guaranteed by process monitoring but, not production tested.
89. The flag is set during power up sequence. To clear the flag, a SPI read must be performed.

Table 33. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the 33910 and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---|--------|-----------|----------|------------------|
| VOLTAGE REGULATOR⁽⁹⁰⁾ (VDD) | | | | | |
| Normal Mode Output Voltage $1.0\text{ mA} < I_{\text{VDD}} < 50\text{ mA}$; $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | V_{DDRUN} | 4.75 | 5.00 | 5.25 | V |
| Normal Mode Output Current Limitation | I_{VDDRUN} | 60 | 110 | 200 | mA |
| Dropout Voltage ⁽⁹¹⁾ $I_{\text{VDD}} = 50\text{ mA}$ | V_{DDDROP} | – | 0.1 | 0.25 | V |
| Stop Mode Output Voltage $I_{\text{VDD}} < 5.0\text{ mA}$ | V_{DDSTOP} | 4.75 | 5.0 | 5.25 | V |
| Stop Mode Output Current Limitation | I_{VDDSTOP} | 6.0 | 12 | 36 | mA |
| Line Regulation Normal mode, $5.5\text{ V} < V_{\text{SUP}} < 18\text{ V}$; $I_{\text{VDD}} = 10\text{ mA}$ Stop mode, $5.5\text{ V} < V_{\text{SUP}} < 18\text{ V}$; $I_{\text{VDD}} = 1.0\text{ mA}$ | LR_{RUN} LR_{STOP} | – – | 20 5.0 | 25 25 | mV |
| Load Regulation Normal mode, $1.0\text{ mA} < I_{\text{VDD}} < 50\text{ mA}$ Stop mode, $0.1\text{ mA} < I_{\text{VDD}} < 5.0\text{ mA}$ | LD_{RUN} LD_{STOP} | – – | 15 10 | 80 50 | mV |
| Over-temperature Prewarning (Junction) ⁽⁹²⁾ Interrupt generated, Bit VDDOT Set | T_{PRE} | 110 | 125 | 140 | $^\circ\text{C}$ |
| Over-temperature Prewarning hysteresis ⁽⁹²⁾ | $T_{\text{PRE_HYS}}$ | – | 10 | – | $^\circ\text{C}$ |
| Over-temperature Shutdown Temperature (Junction) ⁽⁹²⁾ | T_{SD} | 155 | 170 | 185 | $^\circ\text{C}$ |
| Over-temperature Shutdown hysteresis ⁽⁹²⁾ | $T_{\text{SD_HYS}}$ | – | 10 | – | $^\circ\text{C}$ |
| HALL SENSOR SUPPLY OUTPUT⁽⁹³⁾ (HVDD) | | | | | |
| V_{DD} Voltage matching $H_{\text{VDDACC}} = (HVDD - VDD) / VDD * 100\%$ $I_{\text{HVDD}} = 15\text{ mA}$ | H_{VDDACC} | -2.0 | – | 2.0 | % |
| Current Limitation | I_{HVDD} | 20 | 30 | 50 | mA |
| Dropout Voltage $I_{\text{HVDD}} = 15\text{ mA}$; $I_{\text{VDD}} = 5.0\text{ mA}$ | H_{VDDDROP} | – | 160 | 300 | mV |
| Line Regulation $I_{\text{HVDD}} = 5.0\text{ mA}$; $I_{\text{VDD}} = 5.0\text{ mA}$ | LR_{HVDD} | – | 25 | 40 | mV |
| Load Regulation $1.0\text{ mA} > I_{\text{HVDD}} > 15\text{ mA}$; $I_{\text{VDD}} = 5.0\text{ mA}$ | LD_{HVDD} | – | 10 | 20 | mV |

Notes

90. Specification with external capacitor $2.0\text{ }\mu\text{F} < C < 100\text{ }\mu\text{F}$ and $100\text{ m}\Omega \leq \text{ESR} \leq 10\text{ }\Omega$.
 91. Measured when voltage has dropped 250 mV below its nominal Value (5.0 V).
 92. This parameter is guaranteed by process monitoring but, not production tested.
 93. Specification with external capacitor $1.0\text{ }\mu\text{F} < C < 10\text{ }\mu\text{F}$ and $100\text{ m}\Omega \leq \text{ESR} \leq 10\text{ }\Omega$.

ELECTRICAL CHARACTERISTICS
 STATIC ELECTRICAL CHARACTERISTICS

Table 33. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the 33910 and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------------------|----------------------------|------|----------------------------|---------------|
| RST INPUT/OUTPUT PIN ($\overline{\text{RST}}$) | | | | | |
| VDD Low Voltage Reset Threshold | V_{RSTTH} | 4.3 | 4.5 | 4.7 | V |
| Low-State Output Voltage $I_{\text{OUT}} = 1.5\text{ mA}$; $3.5\text{ V} \leq V_{\text{SUP}} \leq 27\text{ V}$ | V_{OL} | 0.0 | – | 0.9 | V |
| High-state Output Current ($0 < V_{\text{OUT}} < 3.5\text{ V}$) | I_{OH} | -150 | -250 | -350 | μA |
| Pull-down Current Limitation (internally limited) $V_{\text{OUT}} = V_{\text{DD}}$ | $I_{\text{PD_MAX}}$ | 1.5 | – | 8.0 | mA |
| Low-state Input Voltage | V_{IL} | -0.3 | – | $0.3 \times V_{\text{DD}}$ | V |
| High-state Input Voltage | V_{IH} | $0.7 \times V_{\text{DD}}$ | – | $V_{\text{DD}} + 0.3$ | V |
| MISO SPI OUTPUT PIN ($\overline{\text{MISO}}$) | | | | | |
| Low-state Output Voltage $I_{\text{OUT}} = 1.5\text{ mA}$ | V_{OL} | 0.0 | – | 1.0 | V |
| High-state Output Voltage $I_{\text{OUT}} = -250\text{ }\mu\text{A}$ | V_{OH} | $V_{\text{DD}} - 0.9$ | – | V_{DD} | V |
| Tri-state Leakage Current $0\text{ V} \leq V_{\text{MISO}} \leq V_{\text{DD}}$ | I_{TRIMISO} | -10 | – | 10 | μA |
| SPI INPUT PINS ($\overline{\text{MOSI}}$, $\overline{\text{SCLK}}$, $\overline{\text{CS}}$) | | | | | |
| Low-state Input Voltage | V_{IL} | -0.3 | – | $0.3 \times V_{\text{DD}}$ | V |
| High-state Input Voltage | V_{IH} | $0.7 \times V_{\text{DD}}$ | – | $V_{\text{DD}} + 0.3$ | V |
| $\overline{\text{MOSI}}$, $\overline{\text{SCLK}}$ Input Current $0\text{ V} \leq V_{\text{IN}} \leq V_{\text{DD}}$ | I_{IN} | -10 | – | 10 | μA |
| $\overline{\text{CS}}$ Pull-up current $0\text{ V} < V_{\text{IN}} < 3.5\text{ V}$ | I_{PUCS} | 10 | 20 | 30 | μA |
| INTERRUPT OUTPUT PIN ($\overline{\text{IRQ}}$) | | | | | |
| Low-state Output Voltage $I_{\text{OUT}} = 1.5\text{ mA}$ | V_{OL} | 0.0 | – | 0.8 | V |
| High-state Output Voltage $I_{\text{OUT}} = -250\text{ }\mu\text{A}$ | V_{OH} | $V_{\text{DD}} - 0.8$ | – | V_{DD} | V |
| Leakage current $V_{\text{DD}} \leq V_{\text{OUT}} \leq 10\text{ V}$ | V_{OH} | – | – | 2.0 | mA |
| PULSE WIDTH MODULATION INPUT PIN ($\overline{\text{PWMIN}}$) | | | | | |
| Low-state Input Voltage | V_{IL} | -0.3 | – | $0.3 \times V_{\text{DD}}$ | V |
| High-state Input Voltage | V_{IH} | $0.7 \times V_{\text{DD}}$ | – | $V_{\text{DD}} + 0.3$ | V |
| Pull-up current $0\text{ V} < V_{\text{IN}} < 3.5\text{ V}$ | I_{PUPWMIN} | 10 | 20 | 30 | μA |

Table 33. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the 33910 and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|------------------------|----------------------|-----|-----------------|------------------|
| HIGH SIDE OUTPUT HS1 AND HS2 PINS (HS1, HS2) | | | | | |
| Output Drain-to-Source On Resistance $T_J = 25^\circ\text{C}$, $I_{\text{LOAD}} = 50\text{ mA}$; $V_{\text{SUP}} > 9.0\text{ V}$ $T_J = 150^\circ\text{C}$, $I_{\text{LOAD}} = 50\text{ mA}$; $V_{\text{SUP}} > 9.0\text{ V}$ ⁽⁹⁴⁾ $T_J = 150^\circ\text{C}$, $I_{\text{LOAD}} = 30\text{ mA}$; $5.5\text{ V} < V_{\text{SUP}} < 9.0\text{ V}$ ⁽⁹⁴⁾ | $R_{\text{DS(ON)}}$ | – | – | 7.0 10 14 | Ω |
| Output Current Limitation ⁽⁹⁵⁾ $0\text{ V} < V_{\text{OUT}} < V_{\text{SUP}} - 2.0\text{ V}$ | I_{LIMHS1} | 60 | 120 | 250 | mA |
| Open Load Current Detection ⁽⁹⁶⁾ | I_{OLHSx} | – | 5.0 | 7.5 | mA |
| Leakage Current ($-0.2\text{ V} < V_{\text{HSx}} < V_{\text{S2}} + 0.2\text{ V}$) | I_{LEAK} | – | – | 10 | μA |
| Short Circuit Detection Threshold ⁽⁹⁷⁾ $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | V_{THSC} | $V_{\text{SUP}} - 2$ | – | – | V |
| Over-temperature Shutdown ^{(98), (99)} | T_{HSSD} | 150 | 165 | 180 | $^\circ\text{C}$ |
| Over-temperature Shutdown Hysteresis ⁽⁹⁹⁾ | $T_{\text{HSSD_HYS}}$ | – | 10 | – | $^\circ\text{C}$ |

L1 INPUT PIN (L1)

| | | | | | |
|---|-------------------------------|--------------|------------|--------------|------------------|
| Low Detection Threshold $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | V_{THL} | 2.0 | 2.5 | 3.0 | V |
| High Detection Threshold $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | V_{THH} | 3.0 | 3.5 | 4.0 | V |
| Hysteresis $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | V_{HYS} | 0.5 | 1.0 | 1.5 | V |
| Input Current ⁽¹⁰⁰⁾ $-0.2\text{ V} < V_{\text{IN}} < V_{\text{S1}}$ | I_{IN} | -10 | – | 10 | μA |
| Analog Input Impedance ⁽¹⁰¹⁾ | R_{L1IN} | 800 | 1550 | – | $\text{k}\Omega$ |
| Analog Input Divider Ratio ($\text{RATIO}_{\text{L1}} = V_{\text{L1}} / V_{\text{ADOUT0}}$) L1DS (L1 Divider Select) = 0 L1DS (L1 Divider Select) = 1 | RATIO_{L1} | 0.95 3.42 | 1.0 3.6 | 1.05 3.78 | |
| Analog Output Offset Ratio L1DS (L1 Divider Select) = 0 L1DS (L1 Divider Select) = 1 | $V_{\text{RATIO L1-OFFSET}}$ | -80 -22 | 0.0 0.0 | 80 22 | mV |
| Analog Inputs Matching L1DS (L1 Divider Select) = 0 L1DS (L1 Divider Select) = 1 | $\text{L1}_{\text{MATCHING}}$ | 96 96 | 100 100 | 104 104 | % |

Notes

94. This parameter is production tested up to $T_A = 125^\circ\text{C}$ and guaranteed by process monitoring up to $T_J = 150^\circ\text{C}$.
95. When over-current occurs, the high side stays ON with limited current capability and the HS1CL flag is set in the HSSR.
96. When open-load occurs, the flag (HS1OP) is set in the HSSR.
97. When short circuit occurs and if HVSE flag is enabled, HS1 automatic shutdown.
98. When over-temperature shutdown occurs, both high sides are turned off. All flags in HSSR are set.
99. Guaranteed by characterization but, not production tested
100. Analog multiplexer input disconnected from L1 input pin.
101. Analog multiplexer input connected to L1 input pin.

ELECTRICAL CHARACTERISTICS
STATIC ELECTRICAL CHARACTERISTICS**Table 33. Static Electrical Characteristics (continued)**

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the 33910 and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|----------------------------------|----------------------------|--------|----------------------------|------------------|
| WINDOW WATCHDOG CONFIGURATION PIN (WDCONF) | | | | | |
| External Resistor Range | R_{EXT} | 20 | – | 200 | $\text{k}\Omega$ |
| Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy) ⁽¹⁰²⁾ | WD_{ACC} | -15 | – | 15 | % |
| ANALOG MULTIPLEXER | | | | | |
| Internal Chip Temperature Sense Gain | S_{TTOV} | – | 10.5 | – | mV/K |
| VSENSE Input Divider Ratio ($\text{RATIO}_{\text{VSENSE}} = V_{\text{VSENSE}} / V_{\text{ADOUT0}}$) $5.5\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | $\text{RATIO}_{\text{VSENSE}}$ | 5.0 | 5.25 | 5.5 | |
| VSENSE Output Related Offset $-40^\circ\text{C} < T_A < -20^\circ\text{C}$ | $\text{OFFSET}_{\text{VSENS E}}$ | -30 -45 | – – | 30 45 | mV |
| ANALOG OUTPUT (ADOUT0) | | | | | |
| Maximum Output Voltage $-5.0\text{ mA} < I_O < 5.0\text{ mA}$ | $V_{\text{OUT_MAX}}$ | $V_{\text{DD}} - 0.35$ | – | V_{DD} | V |
| Minimum Output Voltage $-5.0\text{ mA} < I_O < 5.0\text{ mA}$ | $V_{\text{OUT_MIN}}$ | 0.0 | – | 0.35 | V |
| RXD OUTPUT PIN (LIN PHYSICAL LAYER) (RXD) | | | | | |
| Low-state Output Voltage $I_{\text{OUT}} = 1.5\text{ mA}$ | V_{OL} | 0.0 | – | 0.8 | V |
| High-state Output Voltage $I_{\text{OUT}} = -250\text{ }\mu\text{A}$ | V_{OH} | $V_{\text{DD}} - 0.8$ | – | V_{DD} | V |
| TXD INPUT PIN (LIN PHYSICAL LAYER) (TXD) | | | | | |
| Low-state Input Voltage | V_{IL} | -0.3 | – | $0.3 \times V_{\text{DD}}$ | V |
| High-state Input Voltage | V_{IH} | $0.7 \times V_{\text{DD}}$ | – | $V_{\text{DD}} + 0.3$ | V |
| Pin Pull-up Current, $0 < V_{\text{IN}} < 3.5\text{ V}$ | I_{PUIN} | 10 | 20 | 30 | μA |

Notes

102. Watchdog timing period calculation formula: $t_{\text{PWD}} [\text{ms}] = 0.466 * (R_{\text{EXT}} - 20) + 10$ (R_{EXT} in $\text{k}\Omega$)

Table 33. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the 33910 and $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------------------------|----------------------|-----|-------|------------------|
| LIN PHYSICAL LAYER, TRANSCEIVER (LIN)⁽¹⁰³⁾ | | | | | |
| Output Current Limitation Dominant State, $V_{\text{BUS}} = 18\text{ V}$ | I_{BUSLIM} | 40 | 120 | 200 | mA |
| Leakage Output Current to GND Dominant State; $V_{\text{BUS}} = 0\text{ V}$; $V_{\text{BAT}} = 12\text{ V}$ | $I_{\text{BUS_PAS_DOM}}$ | -1.0 | — | — | mA |
| Recessive State; $8.0\text{ V} < V_{\text{BAT}} < 18\text{ V}$; $8.0\text{ V} < V_{\text{BUS}} < 18\text{ V}$; $V_{\text{BUS}} \geq V_{\text{BAT}}$ | $I_{\text{BUS_PAS_REC}}$ | — | — | 20 | μA |
| GND Disconnected; $\text{GND}_{\text{DEVICE}} = V_{\text{SUP}}$; $V_{\text{BAT}} = 12\text{ V}$; $0 < V_{\text{BUS}} < 18\text{ V}$ | $I_{\text{BUS_NO_GND}}$ | -1.0 | — | 1.0 | mA |
| V_{BAT} disconnected; $V_{\text{SUP_DEVICE}} = \text{GND}$; $0 < V_{\text{BUS}} < 18\text{ V}$ | I_{BUS} | — | — | 100 | μA |
| Receiver Input Voltages Receiver Dominant State | V_{BUSDOM} | — | — | 0.4 | V_{SUP} |
| Receiver Recessive State | V_{BUSREC} | 0.6 | — | — | |
| Receiver Threshold Center $(V_{\text{TH_DOM}} + V_{\text{TH_REC}})/2$ | $V_{\text{BUS_CNT}}$ | 0.475 | 0.5 | 0.525 | |
| Receiver Threshold Hysteresis $(V_{\text{TH_REC}} - V_{\text{TH_DOM}})$ | V_{HYS} | — | — | 0.175 | |
| LIN Transceiver Output Voltage Recessive State, TXD HIGH, $I_{\text{OUT}} = 1.0\text{ }\mu\text{A}$ | $V_{\text{LIN_REC}}$ | $V_{\text{SUP}} - 1$ | — | — | V |
| Dominant State, TXD LOW, 500 Ω External Pull-up Resistor, LDVS = 0 | $V_{\text{LIN_DOM_0}}$ | — | 1.1 | 1.4 | |
| Dominant State, TXD LOW, 500 Ω External Pull-up Resistor, LDVS = 1 | $V_{\text{LIN_DOM_1}}$ | — | 1.7 | 2.0 | |
| LIN Pull-up Resistor to V_{SUP} | R_{SLAVE} | 20 | 30 | 60 | k Ω |
| Over-temperature Shutdown ⁽¹⁰⁴⁾ | $T_{\text{LINS D}}$ | 150 | 165 | 180 | $^\circ\text{C}$ |
| Over-temperature Shutdown Hysteresis | $T_{\text{LINS D_HYS}}$ | — | 10 | — | $^\circ\text{C}$ |

Notes

103. Parameters guaranteed for $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$.

104. When Over-temperature shutdown occurs, the LIN bus goes in recessive state and the flag LINOT in LINSR is set.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 34. Dynamic Electrical Characteristics

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$ for the 33910 and $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 85^{\circ}\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---|------------------|-----------------|--------------------|------|
| SPI INTERFACE TIMING (Figure 34) | | | | | |
| SPI Operating Frequency | f_{SPIOP} | – | – | 4.0 | MHz |
| SCLK Clock Period | t_{PSCLK} | 250 | – | N/A | ns |
| SCLK Clock High Time ⁽¹⁰⁵⁾ | t_{WSCLKH} | 110 | – | N/A | ns |
| SCLK Clock Low Time ⁽¹⁰⁵⁾ | t_{WSCLKL} | 110 | – | N/A | ns |
| Falling Edge of $\overline{\text{CS}}$ to Rising Edge of SCLK ⁽¹⁰⁵⁾ | t_{LEAD} | 100 | – | N/A | ns |
| Falling Edge of SCLK to $\overline{\text{CS}}$ Rising Edge ⁽¹⁰⁵⁾ | t_{LAG} | 100 | – | N/A | ns |
| MOSI to Falling Edge of SCLK ⁽¹⁰⁵⁾ | t_{SISU} | 40 | – | N/A | ns |
| Falling Edge of SCLK to MOSI ⁽¹⁰⁵⁾ | t_{SIH} | 40 | – | N/A | ns |
| MISO Rise Time ⁽¹⁰⁵⁾ $C_{\text{L}} = 220\text{ pF}$ | t_{RSO} | – | 40 | – | ns |
| MISO Fall Time ⁽¹⁰⁵⁾ $C_{\text{L}} = 220\text{ pF}$ | t_{FSO} | – | 40 | – | ns |
| Time from Falling or Rising Edges of $\overline{\text{CS}}$ to: ⁽¹⁰⁵⁾ - MISO Low-impedance - MISO High-impedance | t_{SOEN} t_{SODIS} | 0.0 0.0 | – – | 50 50 | ns |
| Time from Rising Edge of SCLK to MISO Data Valid ⁽¹⁰⁵⁾ $0.2 \times V_{\text{DD}} \leq \text{MISO} \leq 0.8 \times V_{\text{DD}}$, $C_{\text{L}} = 100\text{ pF}$ | t_{VALID} | 0.0 | – | 75 | ns |
| RST OUTPUT PIN | | | | | |
| Reset Low-level Duration after V_{DD} High (See Figure 33) | t_{RST} | 0.65 | 1.0 | 1.35 | ms |
| Reset Deglitch Filter Time | t_{RSTDF} | 350 | 600 | 900 | ns |
| WINDOW WATCHDOG CONFIGURATION PIN (WDCONF) | | | | | |
| Watchdog Time Period ⁽¹⁰⁶⁾ External Resistor $R_{\text{EXT}} = 20\text{ k}\Omega$ (1%) External Resistor $R_{\text{EXT}} = 200\text{ k}\Omega$ (1%) Without External Resistor R_{EXT} (WDCONF Pin Open) | t_{PWD} | 8.5 79 110 | 10 94 150 | 11.5 108 205 | ms |

Notes

105. This parameter is guaranteed by process monitoring but, not production tested.

106. Watchdog timing period calculation formula: $t_{\text{PWD}} [\text{ms}] = 0.466 * (R_{\text{EXT}} - 20) + 10$ (R_{EXT} in $\text{k}\Omega$)

Table 34. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$ for the 33910 and $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 85^{\circ}\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

L1 INPUT

| | | | | | |
|---------------------|------------------|-----|----|----|---------------|
| Wake-up Filter Time | t_{WUF} | 8.0 | 20 | 38 | μs |
|---------------------|------------------|-----|----|----|---------------|

STATE MACHINE TIMING

| | | | | | |
|--|---|-----------|---------|-----------|---------------|
| Delay Between $\overline{\text{CS}}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop Mode Activation ⁽¹⁰⁷⁾ | t_{STOP} | — | — | 5.0 | μs |
| Normal Request Mode Timeout (see Figure 33) | t_{NRTOUT} | 110 | 150 | 205 | ms |
| Delay Between SPI Command and HS Turn On ⁽¹⁰⁸⁾ $9.0\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | $t_{\text{S-ON}}$ | — | — | 10 | μs |
| Delay Between SPI Command and HS Turn Off ⁽¹⁰⁸⁾ $9.0\text{ V} < V_{\text{SUP}} < 27\text{ V}$ | $t_{\text{S-OFF}}$ | — | — | 10 | μs |
| Delay Between Normal Request and Normal Mode After a Watchdog Trigger Command (Normal Request mode) ⁽¹⁰⁷⁾ | t_{SNR2N} | — | — | 10 | μs |
| Delay Between $\overline{\text{CS}}$ Wake-up ($\overline{\text{CS}}$ LOW to HIGH) in Stop Mode and: Normal Request mode, VDD ON and $\overline{\text{RST}}$ HIGH First Accepted SPI Command | $t_{\text{WU}\overline{\text{CS}}}$ t_{WUSPI} | 9.0 90 | 15 — | 80 N/A | μs |
| Minimum Time Between Rising and Falling Edge on the $\overline{\text{CS}}$ | $t_{2\overline{\text{CS}}}$ | 4.0 | — | — | μs |

LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0 KBIT/SEC^{(109), (110)}

| | | | | | |
|---|----|-------|---|-------|--|
| Duty Cycle 1: $D1 = t_{\text{BUS_REC(MIN)}} / (2 \times t_{\text{BIT}})$, $t_{\text{BIT}} = 50\text{ }\mu\text{s}$ $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ | D1 | 0.396 | — | — | |
| Duty Cycle 2: $D2 = t_{\text{BUS_REC(MAX)}} / (2 \times t_{\text{BIT}})$, $t_{\text{BIT}} = 50\text{ }\mu\text{s}$ $7.6\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ | D2 | — | — | 0.581 | |

LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR SLOW SLEW RATE - 10.4 KBIT/SEC^{(109), (111)}

| | | | | | |
|---|----|-------|---|-------|---------------|
| Duty Cycle 3: $D3 = t_{\text{BUS_REC(MIN)}} / (2 \times t_{\text{BIT}})$, $t_{\text{BIT}} = 96\text{ }\mu\text{s}$ $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ | D3 | 0.417 | — | — | μs |
| Duty Cycle 4: $D4 = t_{\text{BUS_REC(MAX)}} / (2 \times t_{\text{BIT}})$, $t_{\text{BIT}} = 96\text{ }\mu\text{s}$ $7.6\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ | D4 | — | — | 0.590 | μs |

Notes

107. This parameter is guaranteed by process monitoring but, not production tested.
108. Delay between turn on or off command (rising edge on $\overline{\text{CS}}$) and HS ON or OFF, excluding rise or fall time due to external load.
109. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 k Ω , 6.8 nF / 660 Ω , 10 nF / 500 Ω . Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See [Figure 27](#).
110. See [Figure 28](#).
111. See [Figure 29](#).

ELECTRICAL CHARACTERISTICS
DYNAMIC ELECTRICAL CHARACTERISTICS

Table 34. Dynamic Electrical Characteristics (continued)

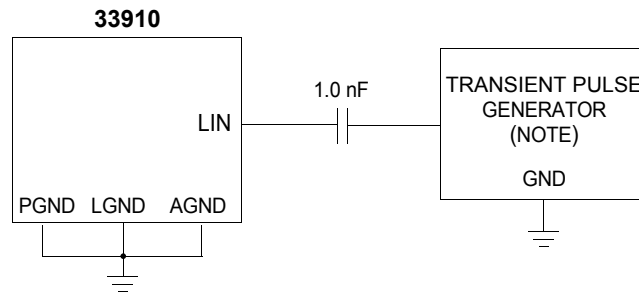
Characteristics noted under conditions $5.5\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$ for the 33910 and $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 85^{\circ}\text{C}$ for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_{\text{A}} = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-----------------------|------|-----|------|------------------|
| LIN PHYSICAL LAYER: DRIVER CHARACTERISTICS FOR FAST SLEW RATE | | | | | |
| LIN Fast Slew Rate (Programming mode) | SR _{FAST} | — | 20 | — | V/ μs |
| LIN PHYSICAL LAYER: CHARACTERISTICS AND WAKE-UP TIMINGS⁽¹¹²⁾ | | | | | |
| Propagation Delay and Symmetry ⁽¹¹³⁾ | | | | | μs |
| Propagation Delay Receiver, $t_{\text{REC_PD}} = \max(t_{\text{REC_PDR}}, t_{\text{REC_PDF}})$ | $t_{\text{REC_PD}}$ | — | 3.0 | 6.0 | |
| Symmetry of Receiver Propagation Delay $t_{\text{REC_PDF}} - t_{\text{REC_PDR}}$ | $t_{\text{REC_SYM}}$ | -2.0 | — | 2.0 | |
| Bus Wake-up Deglitcher (Sleep and Stop modes) ⁽¹¹⁴⁾ | t_{PROPWL} | 42 | 70 | 95 | μs |
| Bus Wake-up Event Reported | | | | | μs |
| From Sleep mode ⁽¹¹⁵⁾ | t_{WAKE} | — | — | 1500 | |
| From Stop mode ⁽¹¹⁶⁾ | t_{WAKE} | 9.0 | 13 | 17 | |
| TXD Permanent Dominant State Delay | t_{TXDDOM} | 0.65 | 1.0 | 1.35 | s |
| PULSE WIDTH MODULATION INPUT PIN (PWMIN) | | | | | |
| PWMIN pin ⁽¹¹⁷⁾ | f_{PWMIN} | — | 10 | — | kHz |
| Max. frequency to drive HS output pins | | | | | |

Notes

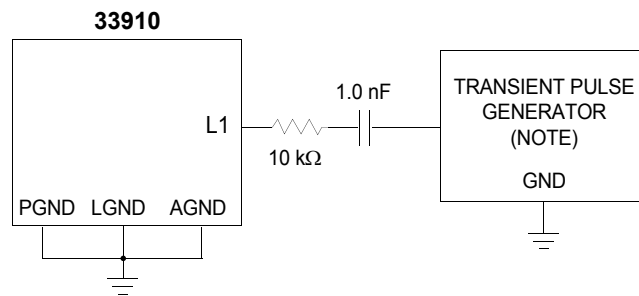
112. V_{SUP} from 7.0 V to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 k Ω , 6.8 nF / 660 Ω , 10 nF / 500 Ω . Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See [Figure 6](#).
113. See [Figure 9](#).
114. See [Figure 10](#), for Sleep and [Figure 11](#), for Stop mode.
115. The measurement is done with 1.0 μF capacitor and 0 mA current load on V_{DD} . The value takes into account the delay to charge the capacitor. The delay is measured between the bus wake-up threshold (V_{BUSWU}) rising edge of the LIN bus and when V_{DD} reaches 3.0 V. See [Figure 10](#). The delay depends of the load and capacitor on V_{DD} .
116. In Stop mode, the delay is measured between the bus wake-up threshold (V_{BUSWU}) and the falling edge of the $\overline{\text{IRQ}}$ pin. See [Figure 11](#).
117. This parameter is guaranteed by process monitoring but, not production tested.

TIMING DIAGRAMS



NOTE: Waveform Per ISO 7637-2. Test Pulses 1, 2, 3a, 3b.

Figure 25. Test Circuit for Transient Test Pulses (LIN)



NOTE: Waveform Per ISO 7637-2. Test Pulses 1, 2, 3a, 3b.

Figure 26. Test Circuit for Transient Test Pulses (L1)

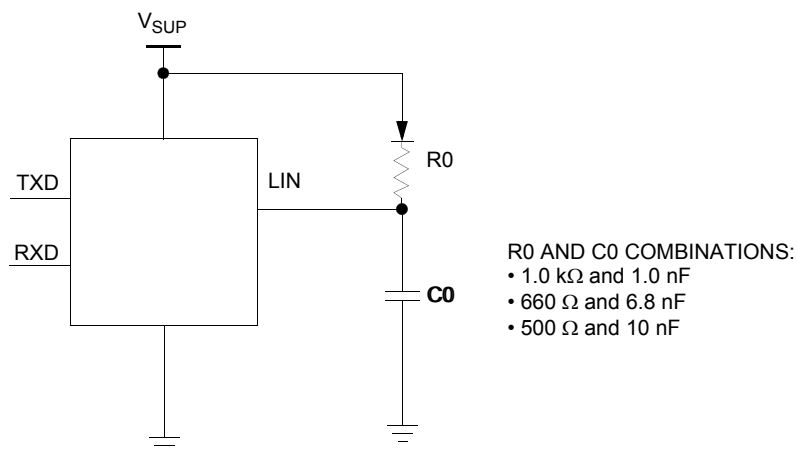


Figure 27. Test Circuit for LIN Timing Measurements

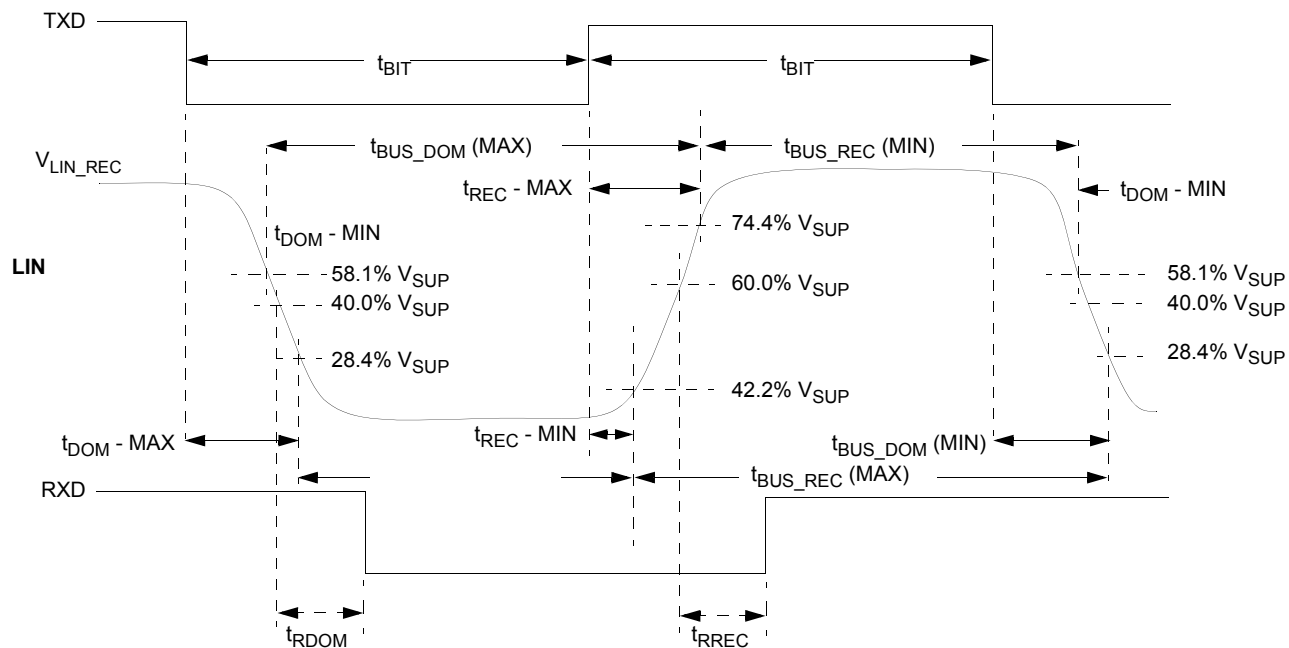
ELECTRICAL CHARACTERISTICS
TIMING DIAGRAMS

Figure 28. LIN Timing Measurements for Normal Slew Rate

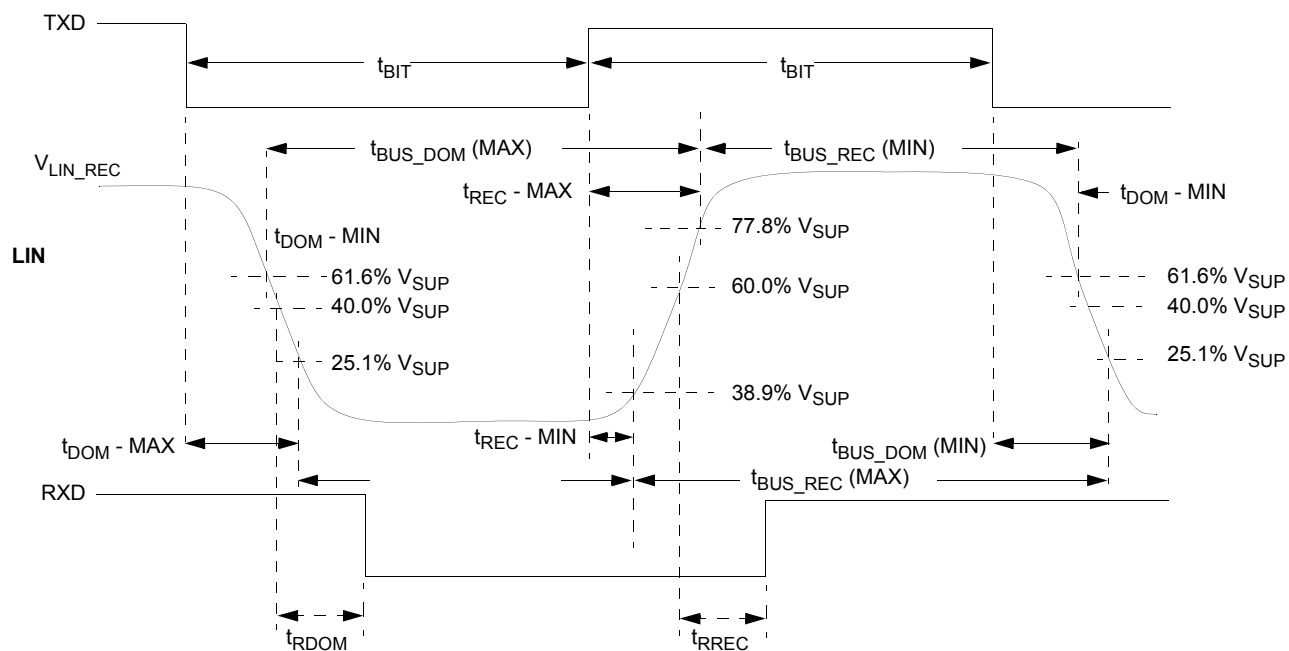


Figure 29. LIN Timing Measurements for Slow Slew Rate

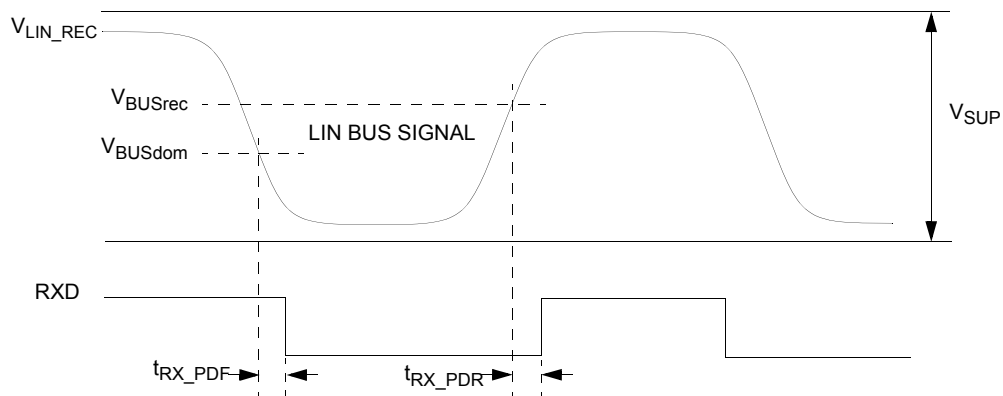


Figure 30. LIN Receiver Timing

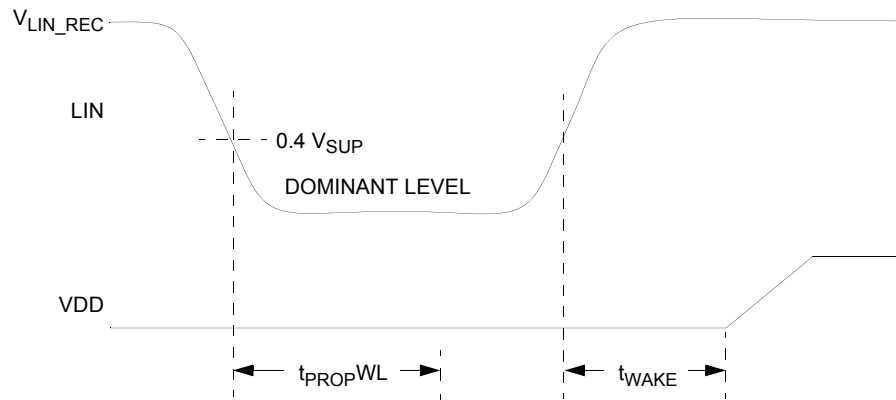


Figure 31. LIN Wake-up Sleep Mode Timing

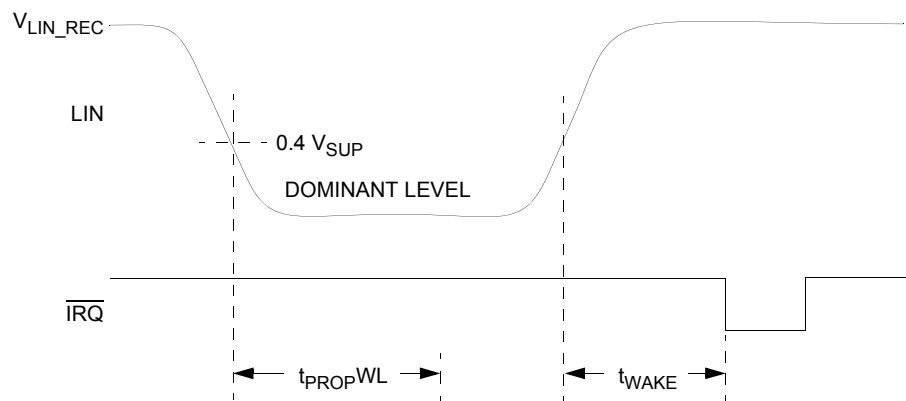


Figure 32. LIN Wake-up Stop Mode Timing

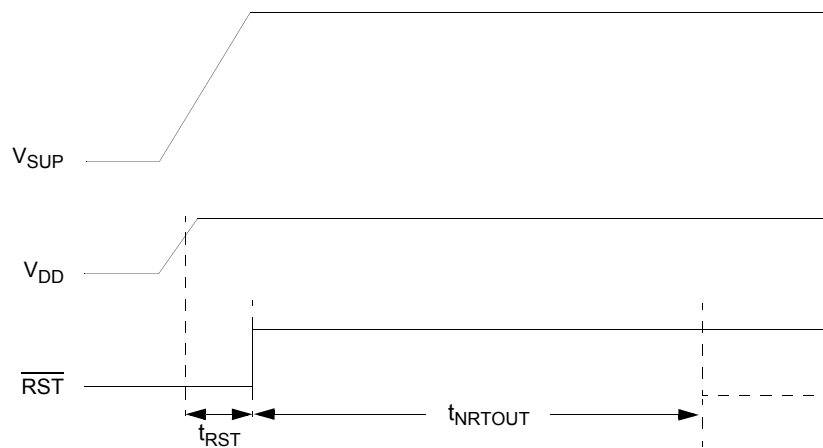


Figure 33. Power On Reset and Normal Request Timeout Timing

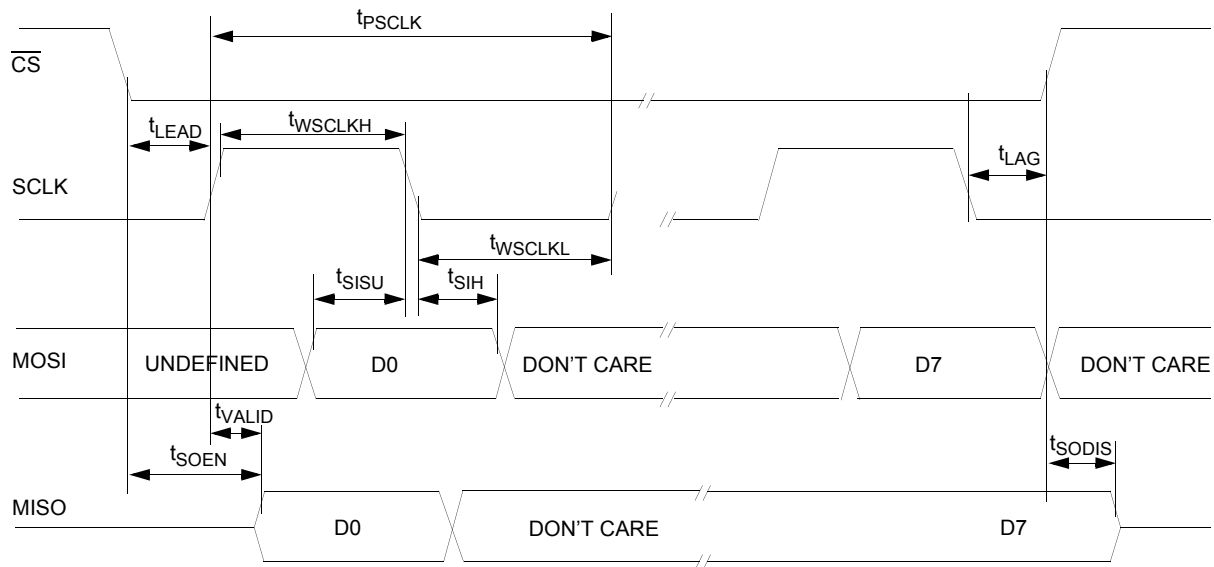


Figure 34. SPI Timing Characteristics

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33910 is designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 33910 is well suited to perform keypad applications via the LIN bus.

Two power switches are provided on the device configured as high side outputs. Other ports are also provided, which

include a wake-up capable pin and a Hall Sensor port supply. An internal voltage regulator provides power to a MCU device.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

FUNCTIONAL PIN DESCRIPTION

See [Table 1, 33910 Simplified Application Diagram](#), for a graphic representation of the various pins referred to in the following paragraphs. Also, see the [33910 Pin Connections](#) for a description of the pin locations in the package.

RECEIVER OUTPUT (RXD)

The RXD pin is a digital output. It is the receiver output of the LIN interface and reports the state of the bus voltage: RXD low when LIN bus is dominant, RXD high when LIN bus is recessive.

TRANSMITTER INPUT (TXD)

The TXD pin is a digital input. It is the transmitter input of the LIN interface and controls the state of the bus output (dominant when TXD is Low, recessive when TXD is High).

This pin has an internal pull-up to force recessive state in case the input is left floating.

LIN BUS (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is compliant to the LIN bus specification 2.0.

The LIN interface is only active during Normal and Normal Request modes.

SERIAL DATA CLOCK (SCLK)

The SCLK pin is the SPI clock input pin. MISO data changes on the negative transition of the SCLK. MOSI is sampled on the positive edge of the SCLK.

MASTER OUT SLAVE IN (MOSI)

The MOSI digital pin receives SPI data from the MCU. This data input is sampled on the positive edge of SCLK.

MASTER IN SLAVE OUT (MISO)

The MISO pin sends data to an SPI-enabled MCU. It is a digital tri-state output used to shift serial data to the

microcontroller. Data on this output pin changes on the negative edge of the SCLK. When \overline{CS} is High, this pin will remain in high-impedance state.

CHIP SELECT (\overline{CS})

\overline{CS} is a active low digital input. It must remain low during a valid SPI communication and allow for several devices to be connected in the same SPI bus without contention. A rising edge on \overline{CS} signals the end of the transmission and the moment the data shifted in is latched. A valid transmission must consist of 8 bits only.

While in STOP mode a low-to-high level transition on this pin will generate a wake-up condition for the 33910.

ANALOG MULTIPLEXER (ADOUT0)

The ADOUT0 pin can be configured via the SPI to allow the MCU A/D converter to read the several inputs of the Analog Multiplexer, including the L1 input voltage and the internal junction temperature.

PWM INPUT CONTROL (PWMIN)

This digital input can control the high sides in Normal Request and Normal mode.

To enable PWM control, the MCU must perform a write operation to the high side control register (HSCR).

This pin has an internal 20 μ A current pull-up.

RESET (\overline{RST})

This bidirectional pin is used to reset the MCU in case the 33910 detects a reset condition or to inform the 33910 that the MCU has just been reset. After release of the \overline{RST} pin Normal Request mode is entered.

The \overline{RST} pin is an active low filtered input and output formed by a weak pull-up and a switchable pull-down structure which allows this pin to be shorted either to V_{DD} or to GND during software development without the risk of destroying the driver.

INTERRUPT ($\overline{\text{IRQ}}$)

The $\overline{\text{IRQ}}$ pin is a digital output used to signal events or faults to the MCU while in Normal and Normal Request mode or to signal a wake-up from Stop mode. This active low output will transition to high, only after the interrupt is acknowledged by a SPI read of the respective status bits.

WATCHDOG CONFIGURATION (WDCONF)

The WDCONF pin is the configuration pin for the internal watchdog. A resistor can be connected to this pin to configure the window watchdog period. When connected directly to ground, the watchdog will be disabled. When this pin is left open, the watchdog period is fixed to its lower precision internal default value (150 ms typical).

GROUND CONNECTION (AGND, PGND, LGND)

The AGND, PGND and LGND pins are the Analog and Power ground pins.

The AGND pin is the ground reference of the voltage regulator.

The PGND and LGND pins are used for high current load return as in the LIN interface pin.

Note: PGND, AGND and LGND pins must be connected together.

DIGITAL/ANALOG (L1)

The L1 pin is a multi purpose input. It can be used as a digital input, which can be sampled by reading the SPI and used for wake-up when 33910 is in Low Power mode or used as analog inputs for the analog multiplexer. When used to sense voltage outside the module, a 33kohm series resistor must be used on each input.

When used as a wake-up input L1 can be configured to operate in Cyclic-Sense mode. In this mode, one of the high side switches is configured to be periodically turned on and sample the wake-up input. If a state change is detected between two cycles a wake-up is initiated. The 33910 can also wake-up from Stop or Sleep by a simple state change on L1.

When used as analog input, the voltage present on the L1 pins is scaled down by an selectable internal voltage divider and can be routed to the ADOUT0 output through the analog multiplexer.

Note: If L1 input is selected in the analog multiplexer, it will be disabled as digital input and remains disabled in low Power mode. No wake-up feature is available in that condition.

When the L1 input is not selected in the analog multiplexer, the voltage divider is disconnected from that input.

HIGH SIDE OUTPUTS (HS1 AND HS2)

These high side switches are able to drive loads such as relays or lamps. Their structure is connected to the VS2 supply pin. The pins are short-circuit protected and also protected against overheating.

HS1 and HS2 are controlled by SPI and can respond to a signal applied to the PWMIN input pin.

The HS1 and HS2 outputs can also be used during Low Power mode for the cyclic-sense of the wake input.

POWER SUPPLY (VS1 AND VS2)

Those are the battery level voltage supply pins. In an application, VS1 and VS2 pins must be protected against reverse battery connection and negative transient voltages, with external components. These pins sustain standard automotive voltage conditions such as load dump at 40 V.

The high side switches (HS1 and HS2) are supplied by the VS2 pin, all other internal blocks are supplied by VS1 pin.

VOLTAGE SENSE PIN (VSENSE)

This input can be connected directly to the battery line. It is protected against battery reverse connection. The voltage present in this input is scaled down by an internal voltage divider, and can be routed to the ADOUT0 output pin and used by the MCU to read the battery voltage.

The ESD structure on this pin allows for excursion up to +40 V, and down to -27 V, allowing this pin to be connected directly to the battery line. It is strongly recommended to connect a 10kohm resistor in series with this pin for protection purposes.

HALL SENSOR SWITCHABLE SUPPLY PIN (HVDD)

This pin provides a switchable supply for external hall sensors. While in Normal mode, this current limited output can be controlled through the SPI.

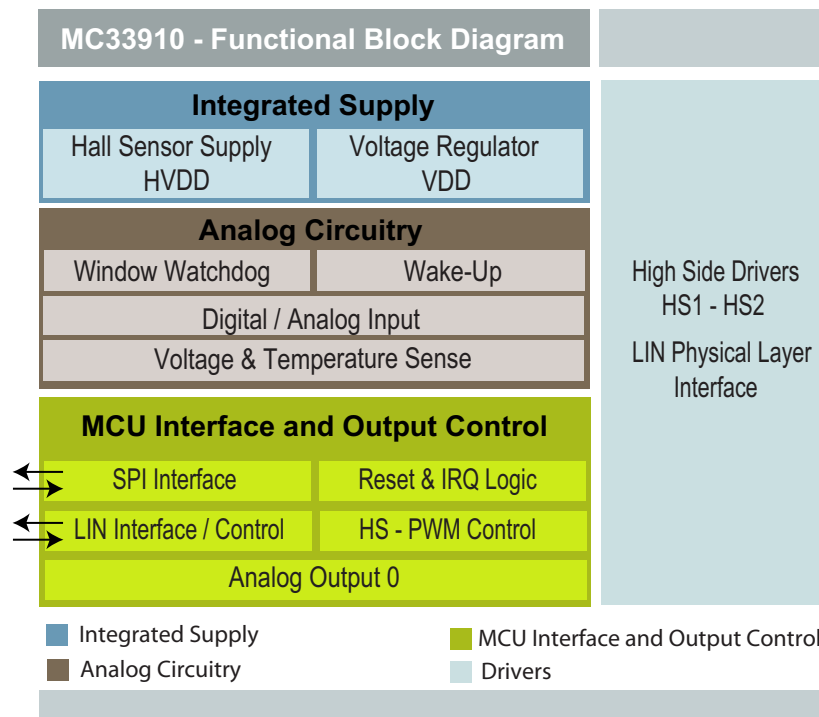
The HVDD pin needs to be connected to an external capacitor to stabilize the regulated output voltage.

+5V MAIN REGULATOR OUTPUT (VDD)

An external capacitor has to be placed on the VDD pin to stabilize the regulated output voltage. The VDD pin is intended to supply a microcontroller. The pin is current limited against shorts to GND and over-temperature protected.

During Stop mode the voltage regulator does not operate with its full drive capabilities and the output current is limited.

During Sleep mode the regulator output is completely shut down.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION**Figure 35. Functional Internal Block Diagram****ANALOG CIRCUITRY**

The 33910 is designed to operate under automotive operating conditions. A fully configurable window watchdog circuit will reset the connected MCU in case of an overflow. Two low power modes are available with several different wake-up sources to reactivate the device. One analog / digital input can be sensed or used as the wake-up source. The device is capable of sensing the supply voltage (VSENSE) and the internal chip temperature (CTEMP).

HIGH SIDE DRIVERS

Two current and temperature protected High Side drivers with PWM capability are provided to drive small loads such as Status LED's or small lamps. Both Drivers can be configured for periodic sense during low power modes.

MCU INTERFACE

The 33910 is providing its control and status information through a standard 8-Bit SPI interface. Critical system events such as Low- or High-voltage/Temperature conditions as well

as over-current conditions in any of the driver stages can be reported to the connected MCU via IRQ or RST. The High Side driver outputs can be controlled via the SPI register as well as the PWMIN input. The integrated LIN physical layer interface can be configured via SPI register and its communication is driven through the RXD and TXD device pins. All internal analog sources are multiplexed to the ADOUT0 pin.

VOLTAGE REGULATOR OUTPUTS

Two independent voltage regulators are implemented on the 33910. The VDD main regulator output is designed to supply a MCU with a precise 5.0 V. The switchable HVDD output is dedicated to supply small peripherals as hall sensors.

LIN PHYSICAL LAYER INTERFACE

The 33910 provides a LIN 2.0 compatible LIN physical layer interface with selectable slew rate and various diagnostic features.

FUNCTIONAL DEVICE OPERATIONS

OPERATIONAL MODES

INTRODUCTION

The 33910 offers three main operating modes: Normal (Run), Stop, and Sleep (Low Power). In Normal mode the device is active and is operating under normal application conditions. The Stop and Sleep modes are low power modes with wake-up capabilities.

In Stop mode the voltage regulator still supplies the MCU with V_{DD} (limited current capability) and in Sleep mode the voltage regulator is turned off ($V_{DD} = 0$ V).

Wake-up from Stop mode is initiated by a wake-up interrupt. Wake-up from Sleep mode is done by a reset and the voltage regulator is turned back on.

The selection of the different modes is controlled by the MOD1:2 bits in the mode control register (MCR).

[Figure 36](#) describes how transitions are done between the different operating modes and [Table 35](#), gives an overview of the Operating mode.

RESET MODE

The 33910 enters the Reset mode after a power up. In this mode, the \overline{RST} pin is low for 1.0 ms (typical value). After this delay, the 33910 enters the Normal Request mode and the RST pin is driven high.

The Reset mode is entered if a reset condition occurs (V_{DD} low, watchdog trigger fail, after a wake-up from Sleep mode, Normal Request mode timeout occurs).

NORMAL REQUEST MODE

This is a temporary mode automatically accessed by the device after the Reset mode or after a wake-up from Stop mode.

In Normal Request mode, the VDD regulator is ON, the Reset pin is high and the LIN is operating in Rx Only mode.

As soon as the device enters the Normal Request mode an internal timer is started for 150 ms (typical value). During these 150 ms, the MCU must configure the timing control register (TIMCR) and the MCR with MOD2 and MOD1 bits $ste = 0$ to enter in Normal mode. If within the 150 ms timeout the MCU does not command the 33910 to Normal mode, it will enter in Reset mode. If the WDCONF pin is grounded in order to disable the watchdog function, the 33910 goes directly in Normal mode after the Reset mode. If the WDCONF pin is open, the 33910 stays typically for 150 ms in Normal Request before entering in Normal mode.

NORMAL MODE

In Normal mode, all 33910 functions are active and can be controlled by the SPI and the PWMIN pin.

The VDD regulator is ON and delivers its full current capability.

If an external resistor is connected between the WDCONF pin and the Ground, the window watchdog function will be enabled.

The wake-up input (L1) can be read as a digital input or have its voltage routed through the analog-multiplexer.

The LIN interface has slew rate and timing compatible with the LIN protocol specification 2.0. The LIN bus can transmit and receive information.

The high side switches are active and have PWM capability according to the SPI configuration.

The interrupts are generated to report failures 5 for V_{SUP} over/under-voltage, thermal shutdown or thermal shutdown prewarning on the main regulator.

SLEEP MODE

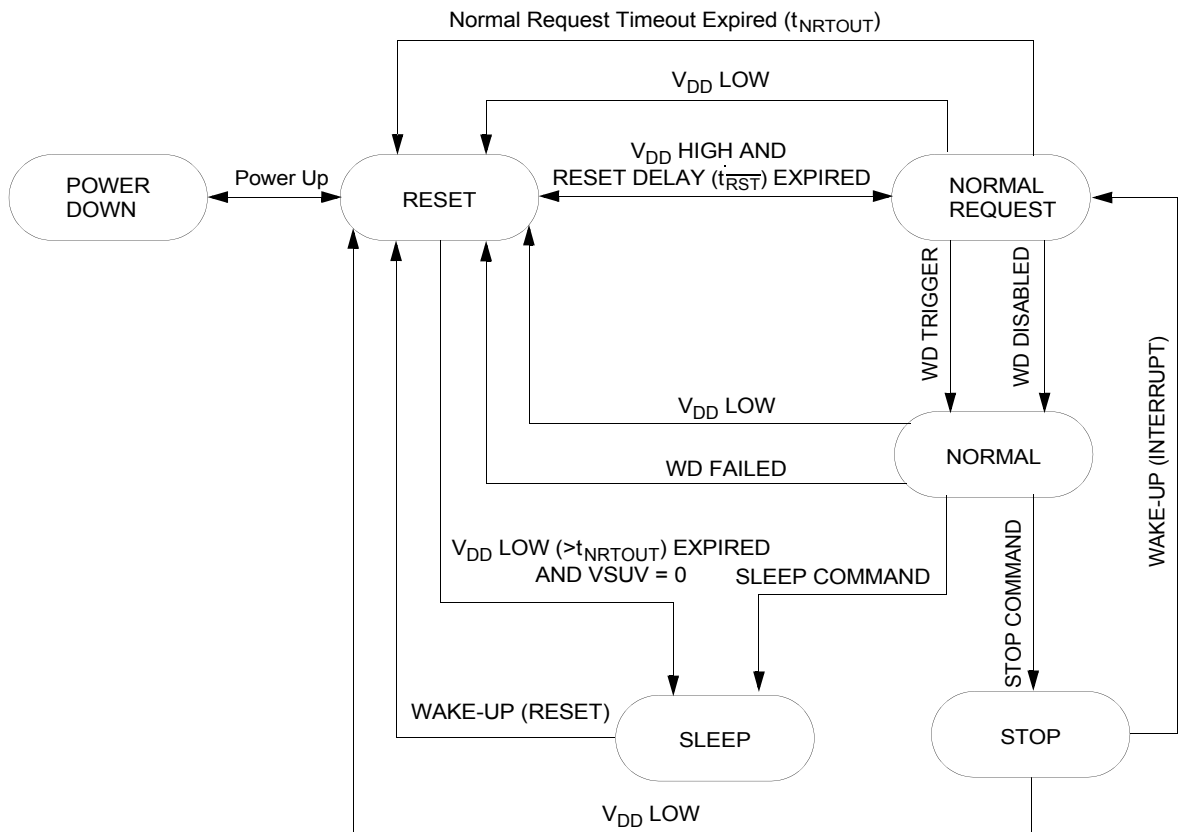
The Sleep mode is a low power mode. From Normal mode, the device enters the Sleep mode by sending one SPI command through the MCR. All blocks are in their lowest power consumption condition. Only some wake-up sources (wake-up input with or without cyclic sense, forced wake-up and LIN receiver) are active. The 5.0 V regulator is OFF. The internal low-power oscillator may be active if the IC is configured for cyclic-sense. In this condition, one of the high side switches is turned on periodically and the wake-up inputs are sampled.

Wake-up from Sleep mode is similar to a power-up. The device goes in Reset mode except that the SPI will report the wake-up source and the BATFAIL flag is not set.

STOP MODE

The Stop mode is the second low power mode, but in this case the 5.0 V regulator is ON with limited current drive capability. The application MCU is always supplied while the 33910 is operating in Stop mode.

The device can enter in Stop mode only by sending the SPI command. When the application is in this mode, it can wake-up from the 33910 side (for example: cyclic sense, force wake-up, LIN bus, wake inputs) or the MCU side (\overline{CS} , RST pins). Wake-up from Stop mode will transition the 33910 to Normal Request mode and generates an interrupt except if the wake-up event is a low to high transition on the \overline{CS} pin or comes from the \overline{RST} pin.

**Legend**

WD: Watchdog

WD Disabled: Watchdog disabled (WDCONF pin connected to GND)

WD Trigger: Watchdog is triggered by SPI command

WD Failed: No watchdog trigger or trigger occurs in closed window

Stop Command: Stop command sent via the SPI

Sleep Command: Sleep command sent via the SPI

Wake-up from Stop mode: L1 state change, LIN bus wake-up, Periodic wake-up, \overline{CS} rising edge wake-up or \overline{RST} wake-up.

Wake-up from Sleep mode: L1 state change, LIN bus wake-up, Periodic wake-up.

Figure 36. Operating Modes and Transitions

Table 35. Operating Modes Overview

| Function | Reset Mode | Normal Request Mode | Normal Mode | Stop Mode | Sleep Mode |
|------------|------------|--------------------------|-------------------------|-----------------------|-----------------------|
| VDD | full | full | full | stop | - |
| HVDD | - | SPI ⁽¹¹⁸⁾ | SPI | - | - |
| HSx | - | SPI/PWM ⁽¹¹⁹⁾ | SPI/PWM | Note ⁽¹²⁰⁾ | Note ⁽¹²¹⁾ |
| Analog Mux | - | SPI | SPI | - | - |
| L1 | - | Input | Input | Wake-up | Wake-up |
| LIN | - | Rx-Only | full/Rx-Only | Rx-Only/Wake-up | Wake-up |
| Watchdog | - | 150 ms (typ.) timeout | On ⁽⁶²⁾ /Off | - | - |
| VSENSE | On | On | On | VDD | - |

Notes

118. Operation can be enabled/controlled by the SPI.
 119. Operation can be controlled by the PWMIN input.
 120. HSx switches can be configured for cyclic sense operation in Stop mode.
 121. HSx switches can be configured for cyclic sense operation in Sleep mode.
 122. Windowing operation when enabled by an external resistor.

INTERRUPTS

Interrupts are used to signal a microcontroller that a peripheral needs to be serviced. The interrupts which can be generated change according to the Operating mode. While in Normal and Normal Request modes the 33910 signals through interrupts special conditions which may require a MCU software action. Interrupts are not generated until all pending wake-up sources are read in the interrupt source register (ISR).

While in Stop mode, interrupts are used to signal wake-up events. Sleep mode does not use interrupts, wake-up is performed by powering-up the MCU. In Normal and Normal Request mode the wake-up source can be read by SPI.

The interrupts are signaled to the MCU by a low logic level of the $\overline{\text{IRQ}}$ pin, which will remain low until the interrupt is acknowledged by a SPI read. The $\overline{\text{IRQ}}$ pin will then be driven high.

Interrupts are only asserted while in Normal-, Normal Request and Stop mode. Interrupts are not generated while the RST pin is low.

Following is a list of the interrupt sources in Normal and Normal Request modes, some of those can be masked by writing to the SPI-interrupt mask register (IMR).

Low Voltage Interrupt

Signals when the supply line (VS1) voltage drops below the VSUV threshold (V_{SUV}).

High Voltage Interrupt

Signals when the supply line (VS1) voltage increases above the VSOV threshold (V_{SOV}).

Over-temperature Prewarning

Signals when the 33910 temperature has reached the pre-shutdown warning threshold. It is used to warn the MCU that an over-temperature shutdown in the main 5.0 V regulator is imminent.

LIN Over-current Shutdown / Over-temperature Shutdown / TXD Stuck At Dominant / RXD Short-circuit

These signal faulty conditions in the LIN interface (except the LIN over-current) that had led to disable the LIN driver. In order to restart operation, the fault must be removed and must be acknowledged by reading the SPI.

The LINOC bit functionality in the LIN status register (LINSR) is to indicate that an LIN over-current occurred and the driver stays enabled.

High Side Over-temperature Shutdown

Signals a shutdown of the high side outputs.

RESET

To reset an MCU, the 33910 drives the $\overline{\text{RST}}$ pin low for the time the reset condition lasts.

After the reset source has been removed the state machine will drive the $\overline{\text{RST}}$ output low for at least 1.0 ms typical value before driving it high.

In the 33910 four main reset sources exist:

5V Regulator Low-Voltage-Reset ($\overline{\text{V}}_{\text{RSTTH}}$)

The 5V regulator output V_{DD} is continuously monitored against brown outs. If the supply monitor detects that the voltage at the VDD pin has dropped below the reset threshold $\overline{\text{V}}_{\text{RSTTH}}$ the 33910 will issue a reset. In case of over-temperature, the voltage regulator will be disabled and the

voltage monitoring will issue a VDDOT Flag independently of the V_{DD} voltage.

Window Watchdog Overflow

If the watchdog counter is not properly serviced while its window is open, the 33910 will detect a MCU software runaway and will reset the microcontroller.

Wake-up From Sleep Mode

During Sleep mode, the 5.0 V regulator is not active, hence all wake-up requests from Sleep mode require a power-up/reset sequence.

External Reset

The 33910 has a bidirectional reset pin which drives the device to a safe state (same as Reset mode) for as long as this pin is held low. The RST pin must be held low long enough to pass the internal glitch filter and get recognized by the internal reset circuit. This functionality is also active in Stop mode.

After the $\overline{\text{RST}}$ pin is released, there is no extra $t_{\overline{\text{RST}}}$ to be considered.

WAKE-UP CAPABILITIES

Once entered in to one of the low-power modes (Sleep or Stop) only wake-up sources can bring the device into Normal mode operation.

In Stop mode, a wake-up is signaled to the MCU as an interrupt, while in Sleep mode the wake-up is performed by activating the 5.0 V regulator and resetting the MCU. In both cases the MCU can detect the wake-up source by accessing the SPI registers. There is no specific SPI register bit to signal a CS wake-up or external reset. If necessary this condition is detected by excluding all other possible wake-up sources.

Wake-up From Wake-up Input (L1) With Cyclic Sense Disabled

The wake-up line is dedicated to sense state changes of external switches and wake-up the MCU (in Sleep or Stop mode).

In order to select and activate direct wake-up from the L1 input, the wake-up control register (WUCR) must be configured with L1WE input enabled. The wake-up input state is read through the wake-up status register (WUSR).

L1 input is also used to perform cyclic-sense wake-up.

Note: Selecting the L1 input in the analog multiplexer before entering Low Power mode will disable the wake-up capability of the L1 input.

Wake-up From Wake-up Input (L1) With Cyclic Sense Timer Enabled

The SBCLIN can wake-up at the end of a cyclic sense period if on the wake-up input lines (L1) a state change occurs. The HSx switch is activated in Sleep or Stop modes from an internal timer. Cyclic sense and force wake-up are exclusive. If cyclic sense is enabled, the force wake-up can not be enabled.

In order to select and activate the cyclic sense wake-up from the L1 input, before entering in low power modes (Stop or Sleep modes), the following SPI set-up has to be performed:

- In WUCR: select the L1 input to WU-enable.
- In HSCR: enable HSx.
- In TIMCR: select the $\overline{\text{CS}}/\overline{\text{WD}}$ bit and determine the cyclic sense period with CYSTx bits.
- Perform Goto Sleep/Stop command.

Forced Wake-up

The 33910 can wake-up automatically after a predetermined time spent in Sleep or Stop mode. Cyclic sense and forced wake-up are exclusive. If forced wake-up is enabled, the cyclic sense can not be enabled.

To determine the wake-up period, the following SPI set-up has to be sent before entering in Low Power modes:

- In TIMCR: select the $\overline{\text{CS}}/\overline{\text{WD}}$ bit and determine the Low Power mode period with CYSTx bits.
- In HSCR: the HSx bit must be disabled.

$\overline{\text{CS}}$ Wake-up

While in Stop mode, a rising edge on the $\overline{\text{CS}}$ will cause a wake-up. The $\overline{\text{CS}}$ wake-up does not generate an interrupt and is not reported on SPI.

LIN Wake-up

While in the low power modes the 33910 monitors the activity on the LIN bus. A dominant pulse larger than t_{PROPWL} followed by a dominant to recessive transition will cause a LIN wake-up. This behavior protects the system from a short-to-ground bus condition.

$\overline{\text{RST}}$ Wake-up

While in Stop mode, the 33910 can wake-up when the $\overline{\text{RST}}$ pin is held low long enough to pass the internal glitch filter. Then, the 33910 will change to Normal Request or Normal modes depending on the WDCONF pin configuration. The $\overline{\text{RST}}$ wake-up does not generate an interrupt and is not reported via SPI.

From Stop mode, the following wake-up events can be configured:

- Wake-up from L1 input without cyclic sense
- Cyclic sense wake-up inputs
- Force wake-up
- $\overline{\text{CS}}$ wake-up
- LIN wake-up
- $\overline{\text{RST}}$ wake-up

From Sleep mode, the following wake-up events can be configured:

- Wake-up from L1 input without cyclic sense
- Cyclic sense wake-up inputs
- Force wake-up
- LIN wake-up

WINDOW WATCHDOG

The 33910 includes a configurable window watchdog which is active in Normal mode. The watchdog can be configured by an external resistor connected to the WDCONF pin. The resistor is used to achieve higher precision in the timebase used for the watchdog.

SPI clears are performed by writing through the SPI in the MOD bits of the MCR.

During the first half of the SPI timeout watchdog clears are not allowed; but after the first half of the PSPI-timeout window the clear operation opens. If a clear operation is performed outside the window, the 33910 will reset the MCU, in the same way as when the watchdog overflows.

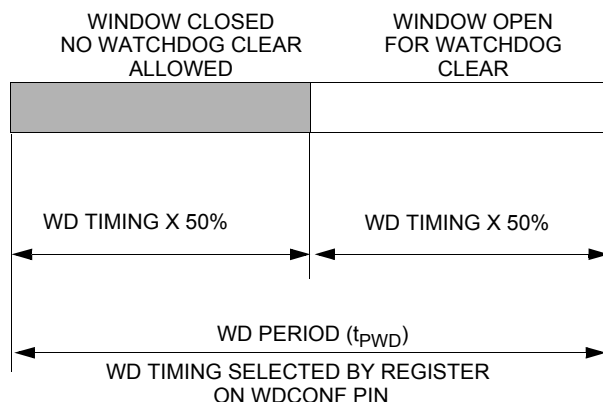


Figure 37. Window Watchdog Operation

To disable the watchdog function in Normal mode the user must connect the WDCONF pin to ground. This measure effectively disables Normal Request mode. The WDOFF bit

in the WDSR will be set. This condition is only detected during Reset mode.

If neither a resistor nor a connection to ground is detected, the watchdog falls back to the internal lower precision timebase of 150 ms (typ.) and signals the faulty condition through the WDSR.

The watchdog timebase can be further divided by a prescaler which can be configured by the TIMCR. During Normal Request mode, the window watchdog is not active but there is a 150 ms (typ.) timeout for leaving the Normal Request mode. In case of a timeout, the 33910 will enter into Reset mode, resetting the microcontroller before entering again into Normal Request mode.

HIGH SIDE OUTPUT PINS HS1 AND HS2

These outputs are two high side drivers intended to drive small resistive loads or LEDs incorporating the following features:

- PWM capability (software maskable)
- Open load detection
- Current limitation
- Over-temperature shutdown (with maskable interrupt)
- High-voltage shutdown (software maskable)
- Cyclic sense

The high side switches are controlled by the bits HS1:2 in the High Side Control Register (HSCR).

PWM Capability (direct access)

Each high side driver offers additional (to the SPI control) direct control via the PWMIN pin.

If both the bits HS1 and PWMHS1 are set in the High Side Control Register (HSCR), then the HS1 driver is turned on if the PWMIN pin is high and turned off if the PWMIN pin is low. This applies to HS2 configuring HS2 and PWMHS2 bits.

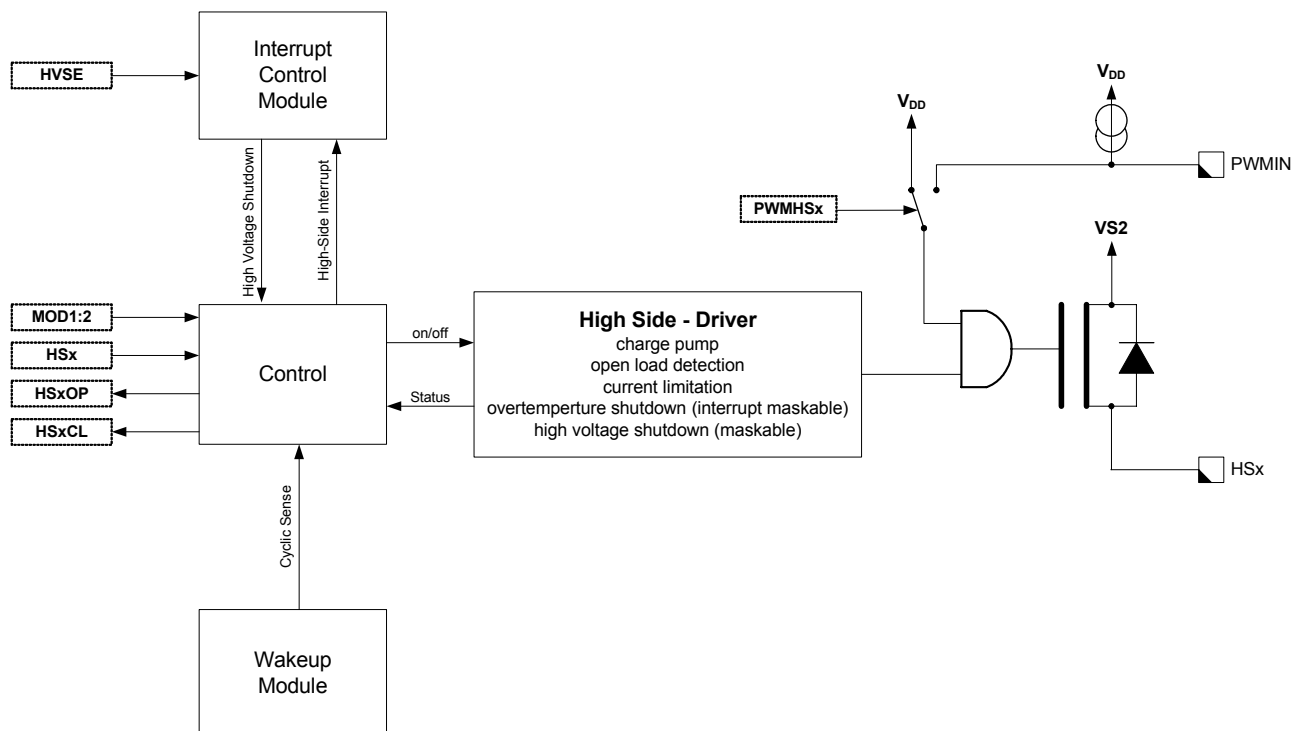


Figure 38. High Side Drivers HS1 and HS2

Open Load Detection

Each high side driver signals an open load condition if the current through the high side is below the open load current threshold.

The open load condition is indicated with the bits HS1OP and HS2OP in the High Side Status Register (HSSR).

Current Limitation

Each high side driver has an output current limitation. In combination with the over-temperature shutdown the high-side drivers are protected against over-current and short-circuit failures.

When the driver operates in the current limitation area, it is indicated with the bits HS1CL and HS2CL in the HSSR.

Note: If the driver is operating in current limitation mode, excessive power might be dissipated.

Over-temperature Protection (HS Interrupt)

Both high side drivers are protected against over-temperature. In case of an over-temperature condition both high side drivers are shut down and the event is latched in the

Interrupt Control Module. The shutdown is indicated as HS Interrupt in the Interrupt Source Register (ISR).

A thermal shutdown of the high side drivers is indicated by setting all HSxOP and HSxCL bits simultaneously.

If the bit HSM is set in the Interrupt Mask Register (IMR), then an interrupt (\overline{IRQ}) is generated.

A write to the High Side Control Register (HSCR), when the over-temperature condition is gone, will re-enable the high side drivers.

High-voltage Shutdown

In case of a high voltage condition and if the high voltage shutdown is enabled (bit HVSE in the Mode Control Register (MCR) is set) both high side drivers are shut down.

A write to the High Side Control Register (HSCR), when the high voltage condition is gone, will re-enable the high side drivers.

Sleep And Stop Mode

The high side driver can be enabled to operate in Sleep and Stop mode for cyclic sensing. Also see [Table 35. Operating Modes Overview](#).

LIN PHYSICAL LAYER

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification and has the following features:

- LIN physical layer 2.0 compliant
- Slew rate selection
- Over-current shutdown
- Over-temperature shutdown
- LIN pull-up disable in Stop and Sleep modes
- Advanced diagnostics
- LIN dominant voltage level selection

The LIN driver is a low side MOSFET with over-current and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a Slave mode. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slopes is guaranteed.

LIN Pin

The LIN pin offers a high susceptibility immunity level from external disturbance, guaranteeing communication.

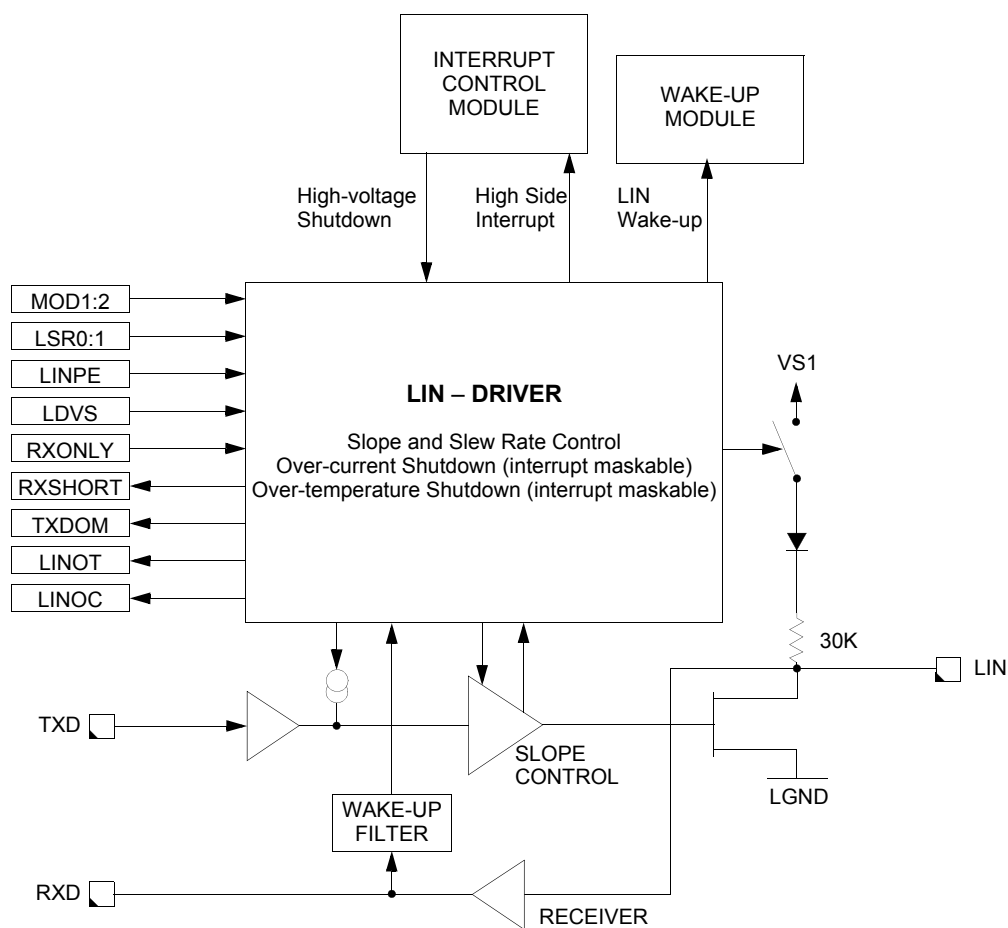


Figure 39. LIN Interface

Slew Rate Selection

The slew rate can be selected for optimized operation at 10.4 and 20 kBit/s as well as a fast baud rate for test and programming. The slew rate can be adapted with the bits LSR1:0 in the LIN control register (LINCR). The initial slew rate is optimized for 20 kBit/s.

LIN Pull-up Disable In Stop and Sleep Mode

To improve performance and for safe behavior in case of LIN bus short to ground or LIN bus leakage during Low Power mode the internal pull-up resistor on the LIN pin can be disconnected by clearing the LINPE bit in the MCR. The bit LINPE also changes the bus wake-up threshold (V_{BUSWU}).

In case of a LIN bus short to GND, this feature will reduce the current consumption in Stop and Sleep modes.

Over-current Shutdown (LIN Interrupt)

The output low side FET is protected against over-current conditions. In case of an over-current condition (e.g. LIN bus short to V_{BAT}), the transmitter will not be shut down. The bit LINOC in the LIN status register (LINSR) is set.

If the bit LINIM is set in the interrupt mask register (IMR) an Interrupt \overline{IRQ} will be generated.

Over-temperature Shutdown (LIN Interrupt)

The output low side FET is protected against over-temperature conditions. In case of an over-temperature condition, the transmitter will be shut down and the bit LINOT in the LIN status register (LINSR) is set.

If the bit LINIM is set in the interrupt mask register (IMR) an Interrupt \overline{IRQ} will be generated.

The transmitter is automatically re-enabled once the condition is gone and TXD is high.

A read of the LIN status register (LINSR) with the TXD pin will re-enable the transmitter.

RXD Short-circuit Detection (LIN Interrupt)

The LIN transceiver has a short-circuit detection for the RXD output pin. In case of a short-circuit condition, either 5.0 V or ground, the bit RXSHORT in the LIN status register (LINSR) is set and the transmitter is shutdown.

If the bit LINIM is set in the interrupt mask register (IMR) an interrupt \overline{IRQ} will be generated.

The transmitter is automatically re-enabled once the condition is gone (transition on RXD) and TXD is high.

A read of the LIN status register (LINSR) without the RXD pin short circuit condition will clear the bit RXSHORT.

TXD Dominant Detection (LIN Interrupt)

The LIN transceiver monitors the TXD input pin to detect stuck in dominant (0 V) condition. In case of a stuck condition (TXD pin 0V for more than 1 second (typ.)) the transmitter is shut down and the bit TXDOM in the LIN status register (LINSR) is set.

If the bit LINIM is set in the interrupt mask register (IMR) an interrupt \overline{IRQ} will be generated.

The transmitter is automatically re-enabled once TXD is high.

A read of the LIN status register (LINSR) with the TXD pin is high will clear the bit TXDOM.

LIN Dominant Voltage Level Selection

The LIN dominant voltage level can be selected by the bit LDVS in the LIN control register (LINCR).

LIN Receiver Operation Only

While in Normal mode the activation of the RXONLY bit disables the LIN TX driver. In the case of a LIN error condition this bit is automatically set. In case a Low Power mode is selected with this bit set, the LIN wake-up functionality is disabled, then, in Stop mode, the RXD pin will reflect the state of the LIN bus.

STOP Mode And Wake-up Feature

During Stop mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Stop mode sequence the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN pin in the recessive state. The receiver is still active and able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by a rising edge will generate a wake-up interrupt and will be reported in the ISR. Also see [Figure 32](#).

SLEEP Mode And Wake-up Feature

During Sleep mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Sleep mode sequence the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN pin in recessive state. The receiver is still active to be able to detect wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by a rising edge will generate a system wake-up (Reset) and will be reported in the ISR. Also see [Figure 31](#).

LOGIC COMMANDS AND REGISTERS

SPI AND CONFIGURATION

The SPI creates the communication link between a microcontroller (master) and the 33910.

The interface consists of four pins (see [Figure 40](#)):

- \overline{CS} —Chip Select
- MOSI—Master-Out Slave-In

- MISO—Master-In Slave-Out
- SCLK—Serial Clock

A complete data transfer via the SPI consists of 1 byte. The master sends 4 bits of address (A3:A0) + 4 bits of control information (C3:C0) and the slave replies with 3 system status bits and one not defined bit (VMS,LINS,HSS,n.d.) + 4 bits of status information (S3:S0).

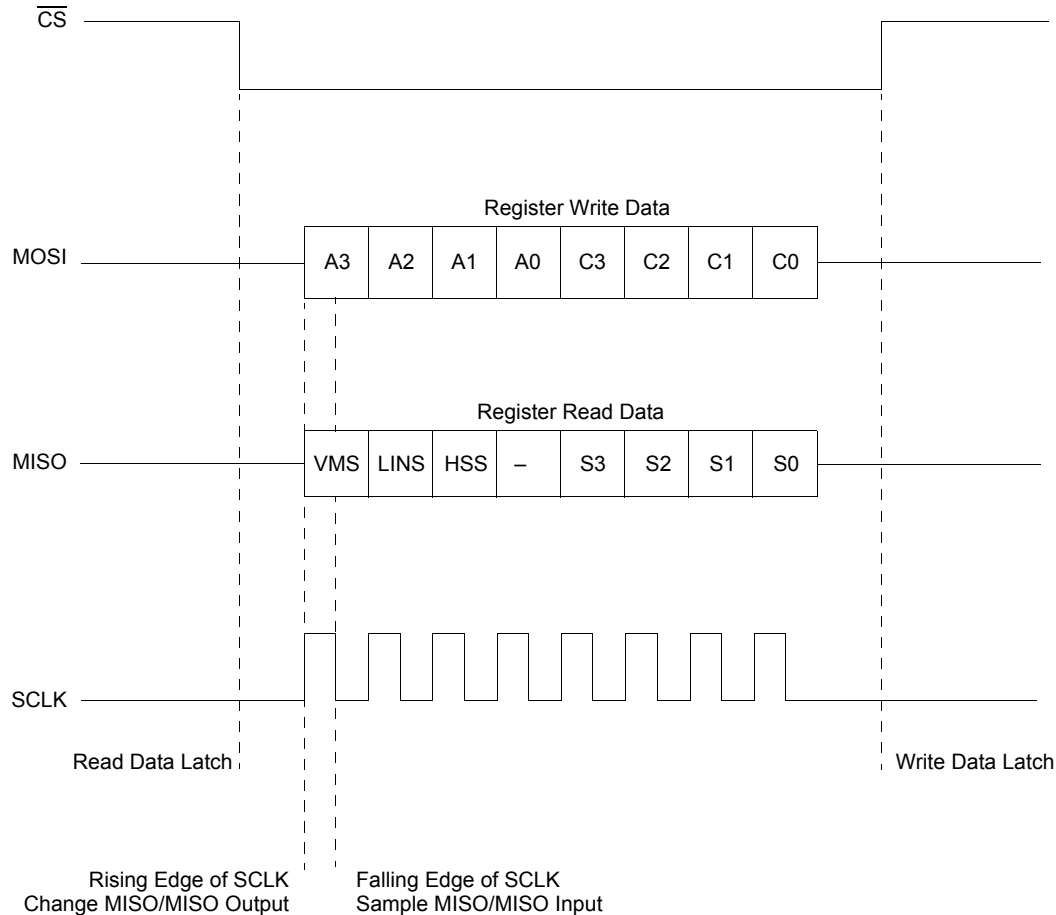


Figure 40. SPI Protocol

During the inactive phase of the \overline{CS} (HIGH), the new data transfer is prepared.

The falling edge of the \overline{CS} indicates the start of a new data transfer and puts the MISO in the low-impedance state and latches the analog status data (Register read data).

With the rising edge of the SPI clock (SCLK), the data is moved to MISO/MOSI pins. With the falling edge of the SPI clock (SCLK) the data is sampled by the receiver.

The data transfer is only valid if exactly 8 sample clock edges are present during the active (low) phase of \overline{CS} .

The rising edge of the chip select \overline{CS} indicates the end of the transfer and latches the write data (MOSI) into the register. The \overline{CS} high forces MISO to the high-impedance state.

Register reset values are described along with the reset condition. Reset condition is the condition causing the bit to be set to its reset value. The main reset conditions are:

- Power-On Reset (POR): level at which the logic is reset and BATFAIL flag sets.
- Reset mode
- Reset done by the \overline{RST} pin (ext_reset)

SPI REGISTER OVERVIEW

Table 36. System Status Register

| Address(A3:A0) | Register Name / Read/Write Information | | BIT | | | |
|----------------|--|---|-----|------|-----|---|
| | | | 7 | 6 | 5 | 4 |
| \$0 - \$F | SYSSR - System Status Register | R | VMS | LINS | HSS | - |

[Table 9](#) summarizes the SPI Register content for Control Information (C3:C0)=W and status information (S3:S0) = R.

Table 37. SPI Register Overview

| Address(A3:A0) | Register Name / Read/Write Information | | BIT | | | |
|----------------|--|---|---------|--------|-------|---------|
| | | | 3 | 2 | 1 | 0 |
| \$0 | MCR - Mode Control Register | W | HVSE | LINPE | MOD2 | MOD1 |
| | VSR - Voltage Status Register | R | VSOV | VSUV | VDDOT | BATFAIL |
| \$1 | VSR - Voltage Status Register | R | VSOV | VSUV | VDDOT | BATFAIL |
| \$2 | WUCR - Wake-up Control Register | W | - | - | - | L1WE |
| | WUSR - Wake-up Status Register | R | - | - | - | L1 |
| \$3 | WUSR - Wake-up Status Register | R | - | - | - | L1 |
| \$4 | LINCR - LIN Control Register | W | LDVS | RXONLY | LSR1 | LSR0 |
| | LINSR - LIN Status Register | R | RXSHORT | TXDOM | LINOT | LINOC |
| \$5 | LINSR - LIN Status Register | R | RXSHORT | TXDOM | LINOT | LINOC |
| \$6 | HSCR - High Side Control Register | W | PWMHS2 | PWMHS1 | HS2 | HS1 |
| | HSSR - High Side Status Register | R | HS2OP | HS2CL | HS1OP | HS1CL |
| \$7 | HSSR - High Side Status Register | R | HS2OP | HS2CL | HS1OP | HS1CL |
| \$A | TIMCR - Timing Control Register | W | CS/WD | WD2 | WD1 | WD0 |
| | | | | CYST2 | CYST1 | CYST0 |
| | WDSR - Watchdog Status Register | R | WDTO | WDERR | WDOFF | WDWO |
| \$B | WDSR - Watchdog Status Register | R | WDTO | WDERR | WDOFF | WDWO |
| \$C | AMUXCR - Analog Multiplexer Control Register | W | L1DS | MX2 | MX1 | MX0 |
| \$D | CFR - Configuration Register | W | HVDD | CYSX8 | - | - |
| \$E | IMR - Interrupt Mask Register | W | HSM | - | LINM | VMM |
| | ISR - Interrupt Source Register | R | ISR3 | ISR2 | ISR1 | ISR0 |
| \$F | ISR - Interrupt Source Register | R | ISR3 | ISR2 | ISR1 | ISR0 |

Note: Address \$8 and \$9 are reserved and must not be used.

REGISTER DEFINITIONS**System Status Register - SYSSR**

The system status register (SYSSR) is always transferred with every SPI transmission and gives a quick system status overview. It summarizes the status of the voltage status register (VSR), LIN status register (LINSR) and the HSSR.

Table 38. System Status Register

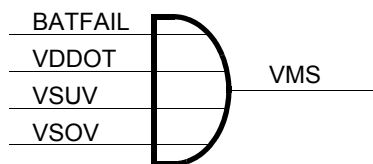
| | S7 | S6 | S5 | S4 |
|------|-----|------|-----|----|
| Read | VMS | LINS | HSS | — |

VMS - Voltage Monitor Status

This read-only bit indicates that one or more bits in the voltage status register (VSR) are set.

1 = Voltage Monitor bit set

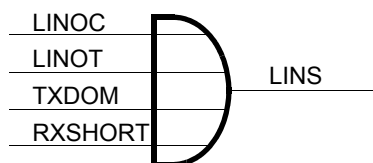
0 = None

**Figure 41. Voltage Monitor Status****LINS - LIN Status**

This read-only bit indicates that one or more bits in the LIN status register (LINSR) are set.

1 = LIN Status bit set

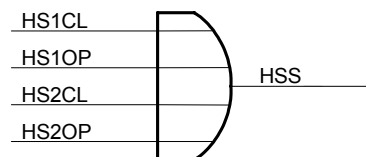
0 = None

**Figure 42. LIN Status****HSS - High Side Switch Status**

This read-only bit indicates that one or more bits in the HSSR are set.

1 = High Side Status bit set

0 = None

**Figure 43. High Side Status****Mode Control Register - MCR**

The MCR allows to switch between the operation modes and to configure the 33910. Writing the MCR will return the voltage status register (VSR).

Table 39. Mode Control Register - \$0

| | C3 | C2 | C1 | C0 |
|-----------------|------|-------|------|------|
| Write | HVSE | LINPE | MOD2 | MOD1 |
| Reset Value | 1 | 1 | - | - |
| Reset Condition | POR | POR | - | - |

HVSE - High-voltage Shutdown Enable

This write-only bit enables/disables automatic shutdown of the high side and the low side drivers during a high-voltage VSOV condition.

1 = automatic shutdown enabled

0 = automatic shutdown disabled

LINPE - LIN pull-up enable.

This write-only bit enables/disables the 30 kΩ LIN pull-up resistor in Stop and Sleep modes. This bit also controls the LIN bus wake-up threshold.

1 = LIN pull-up resistor enabled

0 = LIN pull-up resistor disabled

MOD2, MOD1 - Mode Control Bits

These write-only bits select the Operating mode and allow to clear the watchdog in accordance with [Table 38](#) Mode Control Bits.

Table 40. Mode Control Bits

| MOD2 | MOD1 | Description |
|------|------|------------------------------|
| 0 | 0 | Normal Mode |
| 0 | 1 | Stop Mode |
| 1 | 0 | Sleep Mode |
| 1 | 1 | Normal Mode + watchdog Clear |

Voltage Status Register - VSR

Returns the status of the several voltage monitors. This register is also returned when writing to the MCR.

Table 41. Voltage Status Register - \$0/\$1

| | S3 | S2 | S1 | S0 |
|------|------|------|-------|---------|
| Read | VSOV | VSUV | VDDOT | BATFAIL |

VSOV - V_{SUP} Over-voltage

This read-only bit indicates an over-voltage condition on the VS1 pin.

- 1 = Over-voltage condition.
- 0 = Normal condition.

VSUV - V_{SUP} Under-voltage

This read-only bit indicates an under-voltage condition on the VS1 pin.

- 1 = Under-voltage condition.
- 0 = Normal condition.

VDDOT - Main Voltage Regulator Over-temperature Warning

This read-only bit indicates that the main voltage regulator temperature reached the Over-Temperature Prewarning Threshold.

- 1 = Over-temperature prewarning
- 0 = Normal

BATFAIL - Battery Fail Flag.

This read-only bit is set during power-up and indicates that the 33910 had a power on reset (POR).

Any access to the MCR or voltage status register (VSR) will clear the BATFAIL flag.

- 1 = POR Reset has occurred
- 0 = POR Reset has not occurred

Wake-up Control Register - WUCR

This register is used to control the digital wake-up input. Writing the wake-up control register (WUCR) will return the wake-up status register (WUSR).

Table 42. Wake-up Control Register - \$2

| | C3 | C2 | C1 | C0 |
|-----------------|------------------------------|----|----|------|
| Write | 0 | 0 | 0 | L1WE |
| Reset Value | 1 | 1 | 1 | 1 |
| Reset Condition | POR, Reset mode or ext_reset | | | |

L1WE - Wake-up Input Enable

This write-only bit enables/disables the L1 input. In Stop and Sleep mode the L1WE bit activates the L1 input for wake-up. If the L1 input is selected on the analog multiplexer, the L1WE is masked to 0.

- 1 = Wake-up Input enabled.
- 0 = Wake-up Input disabled.

Wake-up Status Register - WUSR

This register is used to monitor the digital wake-up inputs and is also returned when writing to the wake-up control register (WUCR).

Table 43. Wake-up Status Register - \$2/\$3

| | S3 | S2 | S1 | S0 |
|------|----|----|----|----|
| Read | - | - | - | L1 |

L1 - Wake-up input

This read-only bit indicates the status of the L1 input. If the L1 input is not enabled then the wake-up status will return 0.

After a wake-up from Stop or Sleep mode this bit also allows to verify the L1 input has caused the wake-up, by first reading the interrupt status register (ISR) and then reading the wake-up status register (WUSR).

- 1 = L1 Wake-up.
- 0 = L1 Wake-up disabled or selected as analog input.

LIN Control Register - LINCx

This register controls the LIN physical interface block. Writing the LIN control register (LINCx) returns the LIN status register (LINSR).

Table 44. LIN Control Register - \$4

| | C3 | C2 | C1 | C0 |
|-----------------|------------------------------|---|------|------|
| Write | LDVS | RXONLY | LSR1 | LSR0 |
| Reset Value | 0 | 0 | 0 | 0 |
| Reset Condition | POR, Reset mode or ext_reset | POR, Reset mode, ext_reset or LIN failure gone* | POR | |

* LIN failure gone: if LIN failure (over-temp, TXD/RXD short) was set, the flag resets automatically when the failure is gone.

LDVS - LIN Dominant Voltage Select

This write-only bit controls the LIN Dominant voltage:

1 = LIN Dominant Voltage = $V_{LIN_DOM_1}$ (1.7 V typ)

0 = LIN Dominant Voltage = $V_{LIN_DOM_0}$ (1.1 V typ)

RXONLY - LIN Receiver Operation Only

This write-only bit controls the behavior of the LIN transmitter.

In Normal mode the activation of the RXONLY bit disables the LIN transmitter. In case of a LIN error condition this bit is automatically set.

In Stop mode this bit disables the LIN wake-up functionality and the RXD pin will reflect the state of the LIN bus.

1 = only LIN receiver active (Normal mode) or LIN wake-up disabled (Stop mode).

0 = LIN fully enabled.

LSRx - LIN Slew-Rate

This write-only bit controls the LIN driver slew-rate in accordance with [Table 45](#).

Table 45. LIN Slew-Rate Control

| LSR1 | LSR0 | Description |
|------|------|----------------------------------|
| 0 | 0 | Normal Slew Rate (up to 20 kb/s) |
| 0 | 1 | Slow Slew Rate (up to 10 kb/s) |
| 1 | 0 | Fast Slew Rate (up to 100 kb/s) |
| 1 | 1 | Reserved |

LIN Status Register - LINSR

This register returns the status of the LIN physical interface block and is also returned when writing to the LIN control register (LINCx).

Table 46. LIN Status Register - \$4/\$5

| | S3 | S2 | S1 | S0 |
|------|---------|-------|-------|-------|
| Read | RXSHORT | TXDOM | LINOT | LINOC |

RXSHORT - RXD Pin Short Circuit

This read-only bit indicates a short-circuit condition on the RXD pin (shorted either to 5.0 V or to Ground). The short-circuit delay must be 8.0 μ s worst case to be detected and to shutdown the driver. To clear this bit, it must be read after the condition is gone (transition detected on RXD pin). The LIN driver is automatically re-enabled once the condition is gone.

1 = RXD short circuit condition.

0 = None.

TXDOM - TXD Permanent Dominant

This read-only bit signals the detection of a TXD pin stuck at dominant (Ground) condition and the resultant shutdown in the LIN transmitter. This condition is detected after the TXD pin remains in dominant state for more than 1 second typical value.

To clear this bit, it must be read after TXD has gone high. The LIN driver is automatically re-enabled once TXD goes High.

1 = TXD stuck at dominant fault detected.

0 = None.

LINOT - LIN Driver Over-temperature Shutdown

This read-only bit signals that the LIN transceiver was shutdown due to over-temperature. The transmitter is automatically re-enabled after the over-temperature condition is gone and TXD is high. The LINOT bit is cleared after SPI read once the condition is gone.

1 = LIN over-temperature shutdown

0 = None

LINOC - LIN Driver Over-current Shutdown

This read-only bit signals an over-current condition occurred on the LIN pin. The LIN driver is not shutdown but an IRQ is generated. To clear this bit, it must be read after the condition is gone.

1 = LIN over-current shutdown

0 = None

High Side Control Register - HSCR

This register controls the operation of the high side drivers. Writing to this register returns the High Side Status Register (HSSR).

Table 47. High Side Control Register - \$6

| | C3 | C2 | C1 | C0 |
|-----------------|--------|--------|--|-----|
| Write | PWMHS2 | PWMHS1 | HS2 | HS1 |
| Reset Value | 0 | 0 | 0 | 0 |
| Reset Condition | POR | | POR, Reset mode, ext_reset, HSx over-temp or (VSOV & HVSE) | |

PWMHSx - PWM Input Control Enable

This write-only bit enables/disables the PWMIN input pin to control the high side switch. The high side switch must be enabled (HSx bit).

1 = PWMIN input controls HS1 output.

0 = HSx is controlled only by SPI.

HSx - High Side Switch Control.

This write-only bit enables/disables the high side switch.

1 = HSx switch on.

0 = HSx switch off.

High Side Status Register - HSSR

This register returns the status of the high side switch and is also returned when writing to the HSCR.

Table 48. High Side Status Register - \$6/\$7

| | S3 | S2 | S1 | S0 |
|------|-------|-------|-------|-------|
| Read | HS2OP | HS2CL | HS1OP | HS1CL |

High Side thermal shutdown

A thermal shutdown of the high side drivers is indicated by setting the HSxOP and HSxCL bits simultaneously.

HSxOP - High Side Switch Open-Load Detection

This read-only bit signals that the high side switch is conducting current below a certain threshold indicating possible load disconnection.

1 = HSx Open Load detected (or thermal shutdown)

0 = Normal

HSxCL - High Side Current Limitation

This read-only bit indicates that the high side switch is operating in current Limitation mode.

1 = HSx in current limitation (or thermal shutdown)

0 = Normal

Timing Control Register - TIMCR

This register is a double purpose register which allows to configure the watchdog and the cyclic sense periods. Writing to the TIMCR will also return the WDSR.

Table 49. Timing Control Register - \$A

| | C3 | C2 | C1 | C0 |
|-----------------|-------|-------|-------|-------|
| Write | CS/WD | WD2 | WD1 | WD0 |
| | | CYST2 | CYST1 | CYST0 |
| Reset Value | - | 0 | 0 | 0 |
| Reset Condition | - | POR | | |

CS/WD - Cyclic Sense or Watchdog Prescaler Select.

This write-only bit selects which prescaler is being written to, the cyclic sense prescaler or the watchdog prescaler.

1 = Cyclic Sense Prescaler selected

0 = Watchdog Prescaler select

WDx - Watchdog Prescaler

This write-only bits selects the divider for the watchdog prescaler and therefore selects the watchdog period in accordance with [Table 50](#). This configuration is valid only if windowing watchdog is active.

Table 50. Watchdog Prescaler

| WD2 | WD1 | WD0 | Prescaler Divider |
|-----|-----|-----|-------------------|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 6 |
| 1 | 0 | 0 | 8 |
| 1 | 0 | 1 | 10 |
| 1 | 1 | 0 | 12 |
| 1 | 1 | 1 | 14 |

CYSTx - Cyclic Sense Period Prescaler Select

This write-only bits selects the interval for the wake-up cyclic sensing together with the bit CYSX8 in the configuration register (CFR) (see [Configuration Register - CFR](#)).

This option is only active if the high side switch is enabled when entering in Stop or Sleep mode. Otherwise a timed wake-up is performed after the period shown in [Table 51](#).

Table 51. Cyclic Sense Interval

| CYSX8 ⁽¹²³⁾ | CYST2 | CYST1 | CYST0 | Interval |
|------------------------|-------|-------|-------|-----------------|
| X | 0 | 0 | 0 | No Cyclic Sense |
| 0 | 0 | 0 | 1 | 20 ms |
| 0 | 0 | 1 | 0 | 40 ms |
| 0 | 0 | 1 | 1 | 60 ms |
| 0 | 1 | 0 | 0 | 80 ms |
| 0 | 1 | 0 | 1 | 100 ms |
| 0 | 1 | 1 | 0 | 120 ms |
| 0 | 1 | 1 | 1 | 140 ms |
| 1 | 0 | 0 | 1 | 160 ms |
| 1 | 0 | 1 | 0 | 320 ms |
| 1 | 0 | 1 | 1 | 480 ms |
| 1 | 1 | 0 | 0 | 640 ms |
| 1 | 1 | 0 | 1 | 800 ms |
| 1 | 1 | 1 | 0 | 960 ms |
| 1 | 1 | 1 | 1 | 1120 ms |

Watchdog Status Register

This register returns the watchdog status information and is also returned when writing to the TIMCR.

Table 52. Watchdog Status Register - \$A/\$B

| | S3 | S2 | S1 | S0 |
|------|------|-------|-------|------|
| Read | WDTO | WDERR | WDOFF | WDWO |

WDTO - Watchdog Time Out

This read-only bit signals the last reset was caused by either a watchdog timeout or by an attempt to clear the watchdog within the window closed.

Any access to this register or the TIMCR will clear the WDTO bit.

1 = Last reset caused by watchdog timeout

0 = None

WDERR - Watchdog Error

This read-only bit signals the detection of a missing watchdog resistor. In this condition the watchdog is using the internal, lower precision timebase. The windowing function is disabled.

1 = WDCONF pin resistor missing

0 = WDCONF pin resistor not floating

WDOFF - Watchdog Off

This read-only bit signals that the watchdog pin connected to GND and therefore disabled. In this case watchdog timeouts are disabled and the device automatically enters Normal mode out of Reset. This might be necessary for software debugging and for programming the Flash memory.

1 = Watchdog is disabled

0 = Watchdog is enabled

WDWO - Watchdog Window Open

This read-only bit signals when the watchdog window is open for clears. The purpose of this bit is for testing. Should be ignored in case WDERR is High.

1 = Watchdog window open

0 = Watchdog window closed

Analog Multiplexer Control Register - MUXCR

This register controls the analog multiplexer and selects the divider ration for the L1 input divider.

Table 53. Analog Multiplexer Control Register - \$C

| | C3 | C2 | C1 | C0 |
|-----------------|------|------------------------------|-----|-----|
| Write | L1DS | MX2 | MX1 | MX0 |
| Reset Value | 1 | 0 | 0 | 0 |
| Reset Condition | POR | POR, Reset mode or ext_reset | | |

L1DS - L1 Analog Input Divider Select

This write-only bit selects the resistor divider for the L1 analog input. Voltage is internally clamped to VDD.

0 = L1 Analog divider: 1

1 = L1 Analog divider: 3.6 (typ.)

MXx - Analog Multiplexer Input Select

These write-only bits selects which analog input is multiplexed to the ADOUT0 pin according to [Table 54](#).

When disabled or when in Stop or Sleep mode, the output buffer is not powered and the ADOUT0 output is left floating to achieve lower current consumption.

Table 54. Analog Multiplexer Channel Select

| MX2 | MX1 | MX0 | Meaning |
|-----|-----|-----|------------------------|
| 0 | 0 | 0 | Disabled |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Die Temperature Sensor |
| 0 | 1 | 1 | VSENSE input |
| 1 | 0 | 0 | L1 input |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

Configuration Register - CFR

This register controls the cyclic sense timing multiplier.

Table 55. Configuration Register - \$D

| | C3 | C2 | C1 | C0 |
|-----------------|------------------------------|-------|-----|-----|
| Write | 0 | CYSX8 | 0 | 0 |
| Reset Value | 0 | 0 | 0 | 0 |
| Reset Condition | POR, Reset mode or ext_reset | POR | POR | POR |

HVDD - Hall Sensor Supply Enable

This write-only bit enables/disables the state of the hall sensor supply.

- 1 = HVDD on
- 0 = HVDD off

CYSX8 - Cyclic Sense Timing x 8

This write-only bit influences the Cyclic Sense period as shown in [Table 51](#).

- 1 = Multiplier enabled
- 0 = None

Interrupt Mask Register - IMR

This register allow to mask some of interrupt sources. The respective flags within the ISR will continue to work but will not generate interrupts to the MCU. The 5.0 V Regulator over-temperature prewarning interrupt and under-voltage (VSUV) interrupts can not be masked and will always cause an interrupt.

Writing to the interrupt mask register (IMR) will return the ISR.

Table 56. Interrupt Mask Register - \$E

| | C3 | C2 | C1 | C0 |
|-----------------|-----|----|------|-----|
| Write | HSM | - | LINM | VMM |
| Reset Value | 1 | 1 | 1 | 1 |
| Reset Condition | POR | | | |

HSM - High Side Interrupt Mask

This write-only bit enables/disables interrupts generated in the high side block.

- 1 = HS Interrupts Enabled
- 0 = HS Interrupts Disabled

LINM - LIN Interrupts Mask

This write-only bit enables/disables interrupts generated in the LIN block.

- 1 = LIN Interrupts Enabled
- 0 = LIN Interrupts Disabled

VMM - Voltage Monitor Interrupt Mask

This write-only bit enables/disables interrupts generated in the voltage monitor block. The only maskable interrupt in the voltage monitor block is the V_{SUP} over-voltage interrupt.

- 1 = Interrupts Enabled
- 0 = Interrupts Disabled

Interrupt Source Register - ISR

This register allows the MCU to determine the source of the last interrupt or wake-up respectively. A read of the register acknowledges the interrupt and leads IRQ pin to high, in case there are no other pending interrupts. If there are pending interrupts, \overline{IRQ} will be driven high for 10 μ s and then be driven low again.

This register is also returned when writing to the interrupt mask register (IMR).

Table 57. Interrupt Source Register - \$E/\$F

| | S3 | S2 | S1 | S0 |
|------|------|------|------|------|
| Read | ISR3 | ISR2 | ISR1 | ISR0 |

ISR_x - Interrupt Source Register

These read-only bits indicate the interrupt source following [Table 58](#). If no interrupt is pending than all bits are 0.

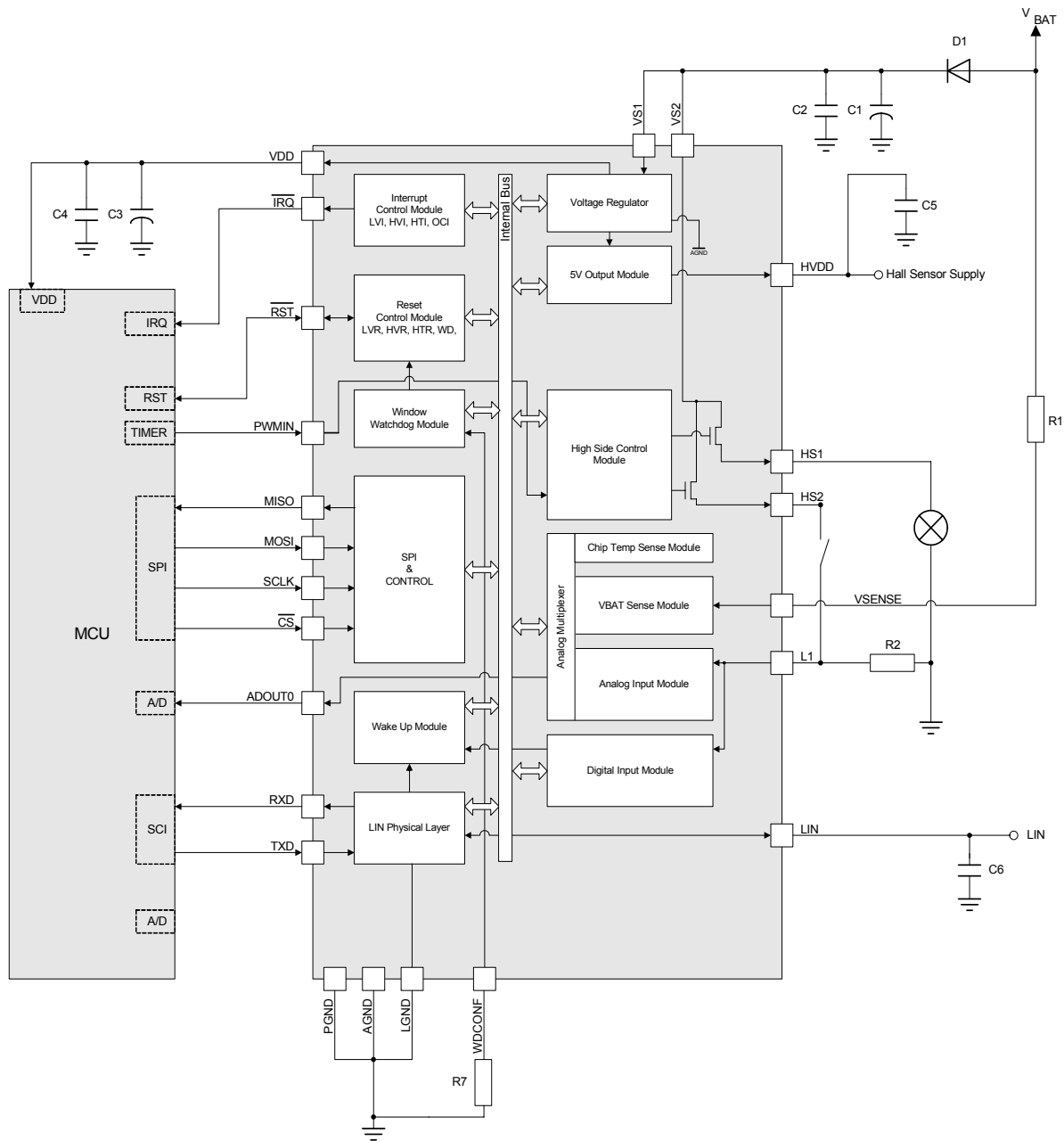
In case more than one interrupt is pending, than the interrupt sources are handled sequentially multiplex.

Table 58. Interrupt Sources

| | | | | Interrupt Source | | Priority |
|------|------|------|------|---|---|----------|
| ISR3 | ISR2 | ISR1 | ISR0 | none maskable | maskable | |
| 0 | 0 | 0 | 0 | no interrupt | no interrupt | none |
| 0 | 0 | 0 | 1 | | L1 wake-up from Stop mode- | highest |
| 0 | 0 | 1 | 0 | - | HS interrupt (Over-temperature) | |
| 0 | 0 | 1 | 1 | - | Reserved | |
| 0 | 1 | 0 | 0 | | LIN interrupt (RXSHORT, TXDOM, LIN OT, LIN OC) or LIN wake-up | |
| 0 | 1 | 0 | 1 | Voltage monitor interrupt (Low-voltage and VDD over-temperature) | Voltage monitor interrupt (High-voltage) | |
| 0 | 1 | 1 | 0 | - | Forced wake-up | lowest |

TYPICAL APPLICATIONS

The 33910 can be configured in several applications. The figure below shows the 33910 in the typical Slave Node Application.

**Typical Component Values:**

C1 = 47 μ F; C2 = C4 = 100 nF; C3 = 10 μ F; C5 = 220 pF

R1 = 10 k Ω ; R2 = 20 k Ω -200 k Ω

Recommended Configuration of the not Connected Pins (NC):

Pin 15, 16, 17, 19, 20, 21, 22 = GND

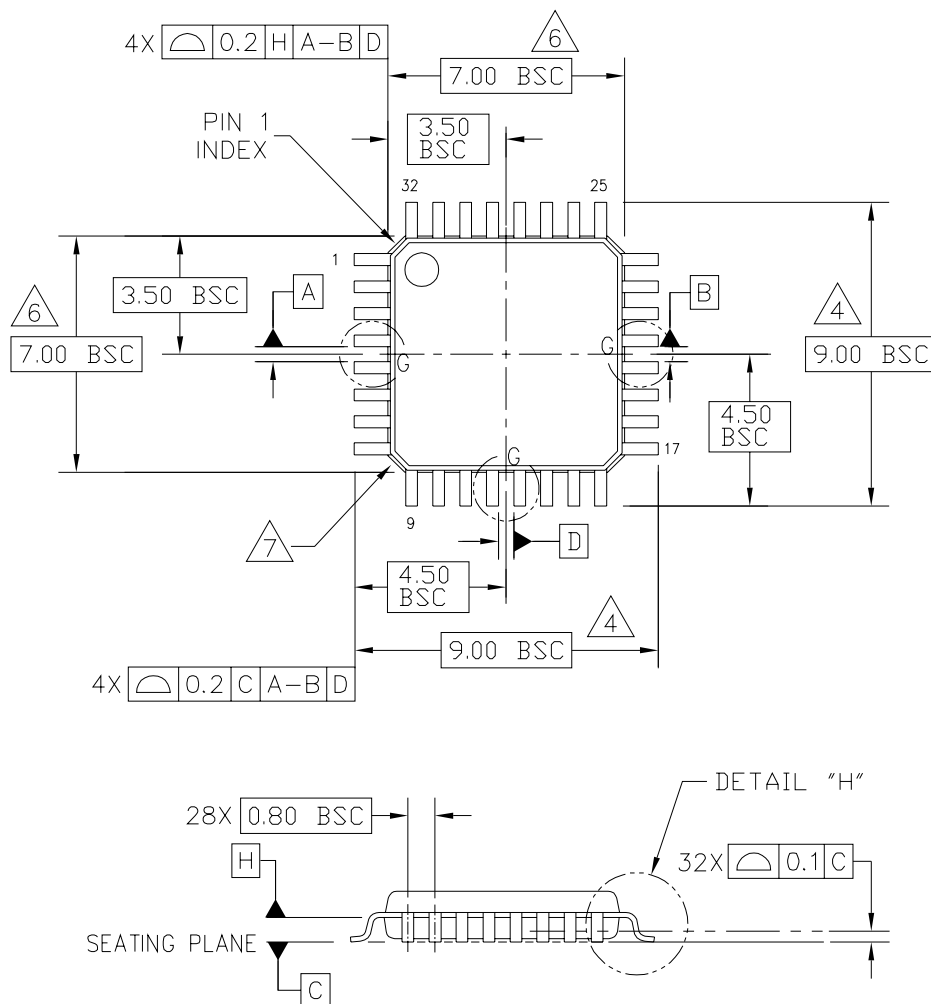
Pin 11 = open (floating)

Pin 28 = this pin is not internally connected and may be used for PCB routing optimization.

PACKAGING

PACKAGE DIMENSIONS

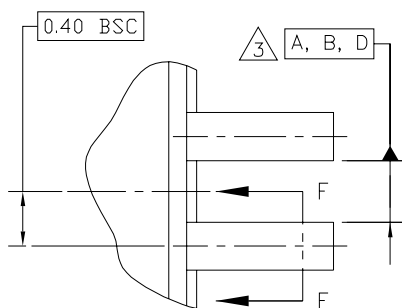
Important For the most current revision of the package, visit www.Freescale.com and select Documentation, then under Available Documentation column select Packaging Information.



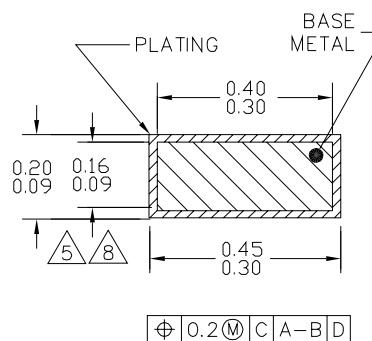
| | | | |
|---|----------------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
| TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4) | DOCUMENT NO: 98ASH70029A | | REV: D |
| | CASE NUMBER: 873A-03 | | 19 MAY 2005 |
| | STANDARD: JEDEC MS-026 BBA | | |

AC SUFFIX (PB-FREE)
32-PIN LQFP
98ASH70029A
REVISION D

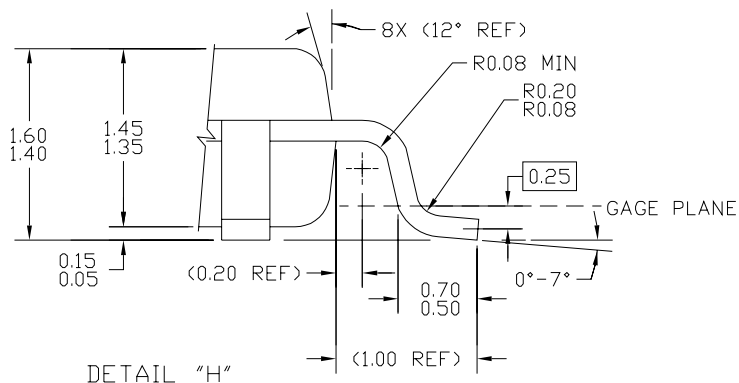
PACKAGE DIMENSIONS (Continued)



DETAIL G



SECTION F-F
ROTATED 90°CW
32 PLACES



DETAIL "H"

| | | | |
|---|----------------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
| TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4) | DOCUMENT NO: 98ASH70029A | | REV: D |
| | CASE NUMBER: 873A-03 | | 19 MAY 2005 |
| | STANDARD: JEDEC MS-026 BBA | | |

AC SUFFIX (PB-FREE)

32-PIN LQFP
98ASH70029A
REVISION D

REVISION HISTORY

| Revision | Date | Description of Changes |
|----------|------|---|
| 1.0 | | <ul style="list-style-type: none"> Initial Release |
| 2.0 | | <ul style="list-style-type: none"> Several textual corrections Page 11: "Analog Output offset Ratio" changed to "Analog Output offset" +/-22mV Page 11: VSENSE Input Divider Ratio adjusted to 5,0/5,25/5,5 Page 12: Common mode input impedance corrected to 75kΩ Page 13/15: LIN PHYSICAL LAYER parameters adjusted to final LIN specification release |
| 3.0 | | <ul style="list-style-type: none"> Revision number incremented at engineering request. |
| 4.0 | | <ul style="list-style-type: none"> Changed Functional Block Diagram on page 24. |
| 5.0 | | <ul style="list-style-type: none"> Datasheet updated according to the Pass1.2 silicon version electrical parameters Add Maximum Rating on I_{BUS_NO_GND} parameter Added L1, Temperature Sense Analog Output Voltage per characterization⁽³⁶⁾, Internal Chip Temperature Sense Gain per characterization at 3 temperatures⁽³⁶⁾ See Figure 16, Temperature Sense Gain, VSENSE Input Divider Ratio (RATIOVSENSE=Vsense/Vadout0) per characterization⁽³⁶⁾, and VSENSE Output Related Offset per characterization⁽³⁶⁾ parameters Added Temperature Sense Gain section Minor corrections to ESD Capability, ⁽¹⁸⁾, Cyclic Sense ON Time from Stop and Sleep Mode⁽⁴⁵⁾, Lin Bus Pin (LIN), Serial Data Clock Pin (SCLK), Master Out Slave In Pin (MOSI), Master In Slave Out Pin (MISO), Digital/ analog Pin (L1), Normal Request Mode, Sleep Mode, LIN Over-temperature Shutdown / TXD Stuck At Dominant / RXD Short-circuit, Fault Detection Management Conditions, Lin Physical Layer, LIN Interface, Over-temperature Shutdown (LIN Interrupt), LIN Receiver Operation Only, SPI Protocol, L1 - Wake-up input 1, LIN Control Register - LINCRCR, and RXSHORT - RXD Pin Short-circuit Updated Freescale form and style |
| 6.0 | | <ul style="list-style-type: none"> Added explanation for pins Not Connected (NC). |
| 7.0 | | <ul style="list-style-type: none"> Changed VBAT_SHIFT and GND_SHIFT maximum from 10% to 11.5% for both parameters on page 13. |
| 8.0 | | <ul style="list-style-type: none"> Combined Complete Data sheet for Part Numbers MC33910BAC and MC34910BAC to the back of this data sheet. Changed ESD Voltage for Machine Model from ± 200 to ± 150 |

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.



Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2009. All rights reserved.

MC33910
Rev. 8.0
3/2010