

9.14.5 Baud Rate Register

The baud rate register (BAUD), shown in [Figure 9-12](#), selects the baud rate for both the receiver and the transmitter.

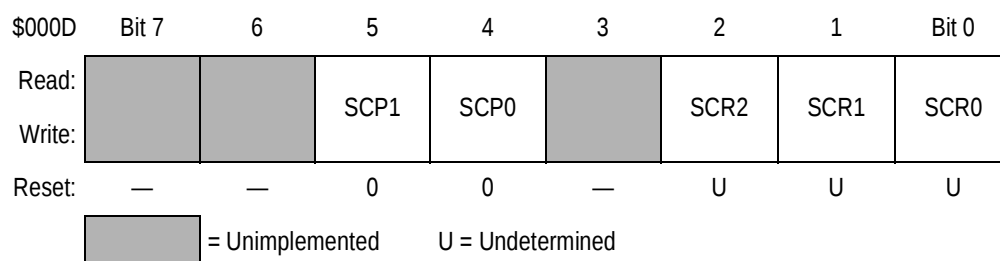


Figure 9-12. Baud Rate Register (BAUD)

SCP1 — SCP0—SCI Prescaler Select Bits

These read/write bits control prescaling of the baud rate generator clock, as shown in [Table 9-1](#). Reset clears both SCP1 and SCP0.

Table 9-1. Baud Rate Generator Clock Prescaling

SCP[1:0]	Baud Rate Generator Clock
00	Internal Clock ÷ 1
01	Internal Clock ÷ 3
10	Internal Clock ÷ 4
11	Internal Clock ÷ 13

SCR2 — SCR0—SCI Baud Rate Select Bits

These read/write bits select the SCI baud rate, as shown in [Table 9-2](#). Resets have no effect on the SCR2–SCR0 bits.

Table 9-2. Baud Rate Selection

SCR[2:0]	SCI Baud Rate (Baud)
000	Prescaled Clock ÷ 1
001	Prescaled Clock ÷ 2
010	Prescaled Clock ÷ 4
011	Prescaled Clock ÷ 8
100	Prescaled Clock ÷ 16
101	Prescaled Clock ÷ 32
110	Prescaled Clock ÷ 64
111	Prescaled Clock ÷ 128

Section 10. Serial Peripheral Interface (SPI)

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10.2 Introduction

The serial peripheral interface (SPI) is an interface built into the device which allows several MC68HC05 MCUs, or MC68HC05 MCU plus peripheral devices, to be interconnected within a single printed circuit board. In an SPI, separate wires are required for data and clock. In the SPI format, the clock is not included in the data stream and must be furnished as a separate signal. An SPI system may be configured in one containing one master MCU and several slave MCUs, or in a system in which an MCU is capable of being a master or a slave.

10.5 Functional Description

Figure 10-2 shows a block diagram of the serial peripheral interface circuitry. When a master device transmits data to a slave via the MOSI line, the slave device responds by sending data to the master device via the master's MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal. Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receive-full status bits. A single status bit (SPIF) is used to signify that the I/O operation has been completed.

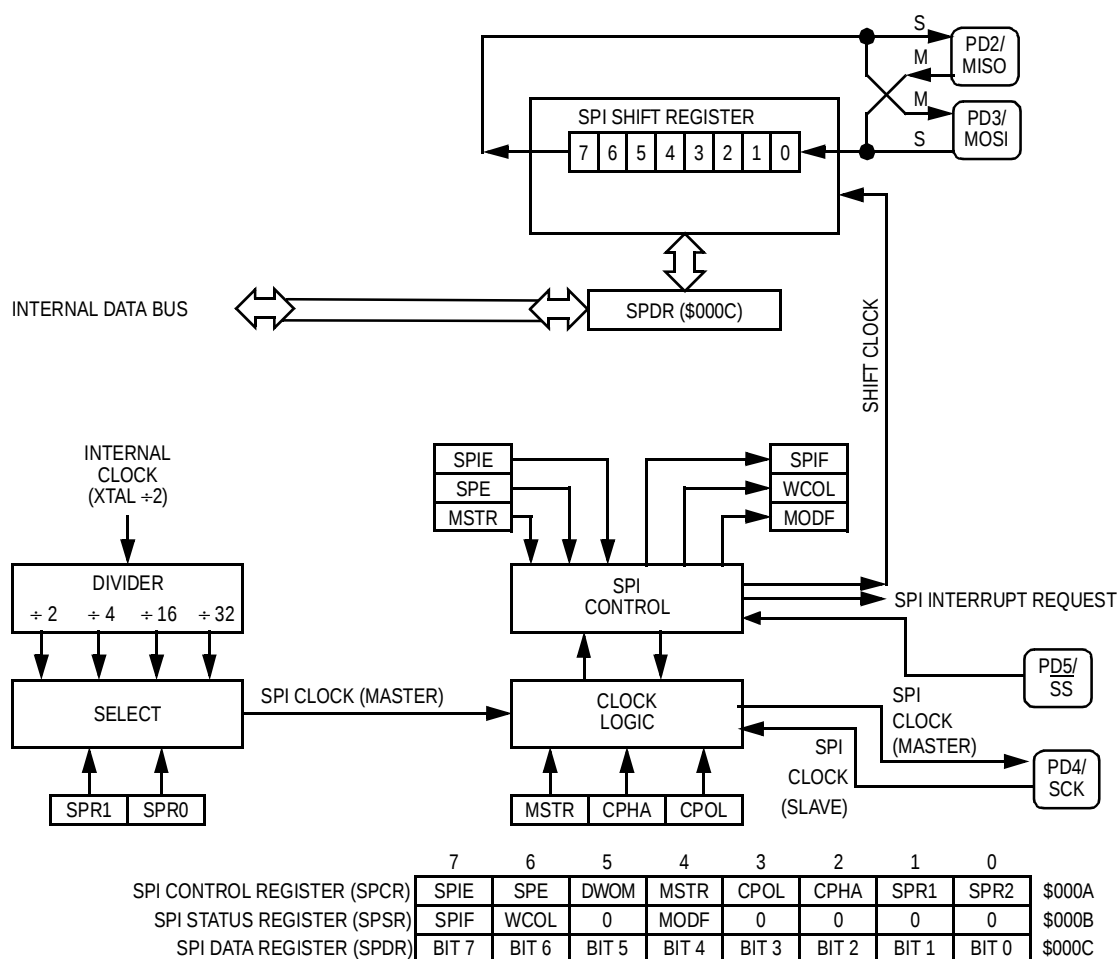


Figure 10-2. Serial Peripheral Interface Block Diagram

SPR1 and SPR0 — SPI Clock Rate Selects

These read/write bits select one of four master mode serial clock rates, as shown in [Table 10-1](#). They have no effect in the slave mode.

Table 10-1. SPI Clock Rate Selection

SPR[1:0]	SPI Clock Rate
00	Internal Clock ÷ 2
01	Internal Clock ÷ 4
10	Internal Clock ÷ 16
11	Internal Clock ÷ 32

10.6.2 Serial Peripheral Status Register

The SPI status register (SPSR), shown in [Figure 10-5](#), contains flags to signal the following conditions:

- SPI transmission complete
- Write collision
- Mode fault

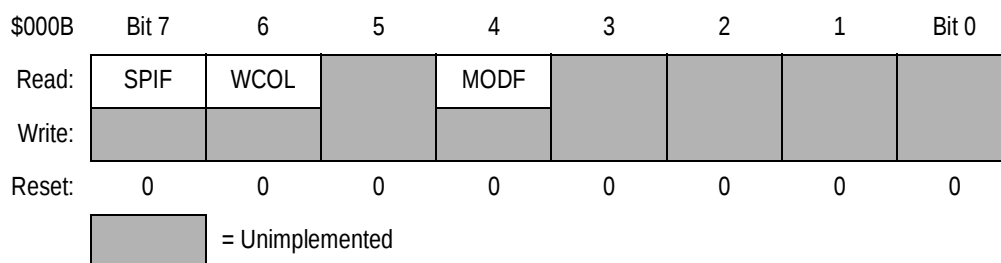


Figure 10-5. SPI Status Register

SPIF — SPI Transfer Complete Flag

The serial peripheral data transfer flag bit is set upon completion of data transfer between the processor and external device. If SPIF goes high, and if SPIE is set, a serial peripheral interrupt is generated. Clearing the SPIF bit is accomplished by reading the SPSR (with

Section 11. Instruction Set

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11.2 Introduction

The MCU instruction set has 62 instructions and uses eight addressing modes. The instructions include all those of the M146805 CMOS Family plus one more: the unsigned multiply (MUL) instruction. The MUL instruction allows unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high-order product is

11.4 Instruction Types

The MCU instructions fall into the following five categories:

- Register/memory instructions
- Read-modify-write instructions
- Jump/branch instructions
- Bit manipulation instructions
- Control instructions

11.4.1 Register/Memory Instructions

These instructions operate on CPU registers and memory locations. Most of them use two operands. One operand is in either the accumulator or the index register. The CPU finds the other operand in memory.

Table 11-1. Register/Memory Instructions

Instruction	Mnemonic
Add Memory Byte and Carry Bit to Accumulator	ADC
Add Memory Byte to Accumulator	ADD
AND Memory Byte with Accumulator	AND
Bit Test Accumulator	BIT
Compare Accumulator	CMP
Compare Index Register with Memory Byte	CPX
EXCLUSIVE OR Accumulator with Memory Byte	EOR
Load Accumulator with Memory Byte	LDA
Load Index Register with Memory Byte	LDX
Multiply	MUL
OR Accumulator with Memory Byte	ORA
Subtract Memory Byte and Carry Bit from Accumulator	SBC
Store Accumulator in Memory	STA
Store Index Register in Memory	STX
Subtract Memory Byte from Accumulator	SUB

11.4.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify its contents, and write the modified value back to the memory location or to the register.

NOTE: Do not use read modify-write operations on write-only registers.

Table 11-2. Read-Modify-Write Instructions

Instruction	Mnemonic
Arithmetic Shift Left (Same as LSL)	ASL
Arithmetic Shift Right	ASR
Bit Clear	BCLR ⁽¹⁾
Bit Set	BSET ⁽¹⁾
Clear Register	CLR
Complement (One's Complement)	COM
Decrement	DEC
Increment	INC
Logical Shift Left (Same as ASL)	LSL
Logical Shift Right	LSR
Negate (Two's Complement)	NEG
Rotate Left through Carry Bit	ROL
Rotate Right through Carry Bit	ROR
Test for Negative or Zero	TST ⁽²⁾

1. Unlike other read-modify-write instructions, BCLR and BSET use only direct addressing.
2. TST is an exception to the read-modify-write sequence because it does not write a replacement value.

Table 11-3. Jump and Branch Instructions

Instruction	Mnemonic
Branch if Carry Bit Clear	BCC
Branch if Carry Bit Set	BCS
Branch if Equal	BEQ
Branch if Half-Carry Bit Clear	BHCC
Branch if Half-Carry Bit Set	BHCS
Branch if Higher	BHI
Branch if Higher or Same	BHS
Branch if $\overline{\text{IRQ}}$ Pin High	BIH
Branch if $\overline{\text{IRQ}}$ Pin Low	BIL
Branch if Lower	BLO
Branch if Lower or Same	BLS
Branch if Interrupt Mask Clear	BMC
Branch if Minus	BMI
Branch if Interrupt Mask Set	BMS
Branch if Not Equal	BNE
Branch if Plus	BPL
Branch Always	BRA
Branch if Bit Clear	BRCLR
Branch Never	BRN
Branch if Bit Set	BRSET
Branch to Subroutine	BSR
Unconditional Jump	JMP
Jump to Subroutine	JSR

11.4.4 Bit Manipulation Instructions

The CPU can set or clear any writable bit in the first 256 bytes of memory, which includes I/O registers and on-chip RAM locations. The CPU can also test and branch based on the state of any bit in any of the first 256 memory locations.

Table 11-4. Bit Manipulation Instructions

Instruction	Mnemonic
Bit Clear	BCLR
Branch if Bit Clear	BRCLR
Branch if Bit Set	BRSET
Bit Set	BSET

11.4.5 Control Instructions

These instructions act on CPU registers and control CPU operation during program execution.

Table 11-5. Control Instructions

Instruction	Mnemonic
Clear Carry Bit	CLC
Clear Interrupt Mask	CLI
No Operation	NOP
Reset Stack Pointer	RSP
Return from Interrupt	RTI
Return from Subroutine	RTS
Set Carry Bit	SEC
Set Interrupt Mask	SEI
Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin	STOP
Software Interrupt	SWI
Transfer Accumulator to Index Register	TAX
Transfer Index Register to Accumulator	TXA
Stop CPU Clock and Enable Interrupts	WAIT

Instruction Set

11.5 Instruction Set Summary

Table 11-6. Instruction Set Summary (Sheet 1 of 6)

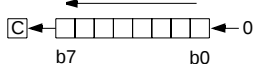
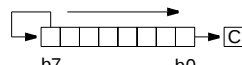
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ADC #opr ADC opr ADC opr ADC opr,X ADC opr,X ADC ,X	Add with Carry	$A \leftarrow (A) + (M) + (C)$	↑	—	↑	↑	↑	IMM DIR EXT IX2 IX1 IX	A9 B9 C9 D9 E9 F9	ii dd hh ll ee ff ff	2 3 4 5 4 3
ADD #opr ADD opr ADD opr ADD opr,X ADD opr,X ADD ,X	Add without Carry	$A \leftarrow (A) + (M)$	↑	—	↑	↑	↑	IMM DIR EXT IX2 IX1 IX	AB BB CB DB EB FB	ii dd hh ll ee ff ff	2 3 4 5 4 3
AND #opr AND opr AND opr AND opr,X AND opr,X AND ,X	Logical AND	$A \leftarrow (A) \wedge (M)$	—	—	↑	↑	—	IMM DIR EXT IX2 IX1 IX	A4 B4 C4 D4 E4 F4	ii dd hh ll ee ff ff	2 3 4 5 4 3
ASL opr ASLA ASLX ASL opr,X ASL ,X	Arithmetic Shift Left (Same as LSL)		—	—	↑	↑	↑	DIR INH INH IX1 IX	38 48 58 68 78	dd ff	5 3 3 6 5
ASR opr ASRA ASRX ASR opr,X ASR ,X	Arithmetic Shift Right		—	—	↑	↑	↑	DIR INH INH IX1 IX	37 47 57 67 77	dd ff	5 3 3 6 5
BCC rel	Branch if Carry Bit Clear	$PC \leftarrow (PC) + 2 + rel ? C = 0$	—	—	—	—	—	REL	24	rr	3
BCLR n opr	Clear Bit n	$Mn \leftarrow 0$	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS rel	Branch if Carry Bit Set (Same as BLO)	$PC \leftarrow (PC) + 2 + rel ? C = 1$	—	—	—	—	—	REL	25	rr	3
BEQ rel	Branch if Equal	$PC \leftarrow (PC) + 2 + rel ? Z = 1$	—	—	—	—	—	REL	27	rr	3
BHCC rel	Branch if Half-Carry Bit Clear	$PC \leftarrow (PC) + 2 + rel ? H = 0$	—	—	—	—	—	REL	28	rr	3
BHCS rel	Branch if Half-Carry Bit Set	$PC \leftarrow (PC) + 2 + rel ? H = 1$	—	—	—	—	—	REL	29	rr	3
BHI rel	Branch if Higher	$PC \leftarrow (PC) + 2 + rel ? C \vee Z = 0$	—	—	—	—	—	REL	22	rr	3
BHS rel	Branch if Higher or Same	$PC \leftarrow (PC) + 2 + rel ? C = 0$	—	—	—	—	—	REL	24	rr	3

Table 11-6. Instruction Set Summary (Sheet 2 of 6)

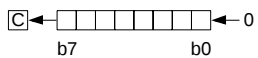
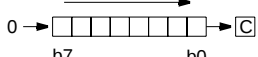
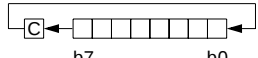
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BIH <i>rel</i>	Branch if IRQ Pin High	$PC \leftarrow (PC) + 2 + rel ? IRQ = 1$	—	—	—	—	—	REL	2F	rr	3
BIL <i>rel</i>	Branch if IRQ Pin Low	$PC \leftarrow (PC) + 2 + rel ? IRQ = 0$	—	—	—	—	—	REL	2E	rr	3
BIT # <i>opr</i> BIT <i>opr</i> BIT <i>opr</i> BIT <i>opr</i> ,X BIT <i>opr</i> ,X BIT ,X	Bit Test Accumulator with Memory Byte	$(A) \wedge (M)$	—	—	↑	↑	—	IMM DIR EXT IX2 IX1 IX	A5 B5 C5 D5 E5 F5	ii dd hh ll ee ff ff	2 3 4 5 4 3
BLO <i>rel</i>	Branch if Lower (Same as BCS)	$PC \leftarrow (PC) + 2 + rel ? C = 1$	—	—	—	—	—	REL	25	rr	3
BLS <i>rel</i>	Branch if Lower or Same	$PC \leftarrow (PC) + 2 + rel ? C \vee Z = 1$	—	—	—	—	—	REL	23	rr	3
BMC <i>rel</i>	Branch if Interrupt Mask Clear	$PC \leftarrow (PC) + 2 + rel ? I = 0$	—	—	—	—	—	REL	2C	rr	3
BMI <i>rel</i>	Branch if Minus	$PC \leftarrow (PC) + 2 + rel ? N = 1$	—	—	—	—	—	REL	2B	rr	3
BMS <i>rel</i>	Branch if Interrupt Mask Set	$PC \leftarrow (PC) + 2 + rel ? I = 1$	—	—	—	—	—	REL	2D	rr	3
BNE <i>rel</i>	Branch if Not Equal	$PC \leftarrow (PC) + 2 + rel ? Z = 0$	—	—	—	—	—	REL	26	rr	3
BPL <i>rel</i>	Branch if Plus	$PC \leftarrow (PC) + 2 + rel ? N = 0$	—	—	—	—	—	REL	2A	rr	3
BRA <i>rel</i>	Branch Always	$PC \leftarrow (PC) + 2 + rel ? 1 = 1$	—	—	—	—	—	REL	20	rr	3
BRCLR <i>n opr rel</i>	Branch if Bit n Clear	$PC \leftarrow (PC) + 2 + rel ? Mn = 0$	—	—	—	—	↑	DIR (b0)	01	dd rr	5
								DIR (b1)	03	dd rr	5
								DIR (b2)	05	dd rr	5
								DIR (b3)	07	dd rr	5
								DIR (b4)	09	dd rr	5
								DIR (b5)	0B	dd rr	5
								DIR (b6)	0D	dd rr	5
BRSET <i>n opr rel</i>	Branch if Bit n Set	$PC \leftarrow (PC) + 2 + rel ? Mn = 1$	—	—	—	—	↑	DIR (b7)	0F	dd rr	5
								DIR (b0)	00	dd rr	5
								DIR (b1)	02	dd rr	5
								DIR (b2)	04	dd rr	5
								DIR (b3)	06	dd rr	5
								DIR (b4)	08	dd rr	5
								DIR (b5)	0A	dd rr	5
BSET <i>n opr</i>	Set Bit n	$Mn \leftarrow 1$	—	—	—	—	—	DIR (b6)	0C	dd rr	5
								DIR (b7)	0E	dd rr	5
								DIR (b0)	10	dd	5
								DIR (b1)	12	dd	5
								DIR (b2)	14	dd	5
								DIR (b3)	16	dd	5
								DIR (b4)	18	dd	5
BSR <i>rel</i>	Branch to Subroutine	$PC \leftarrow (PC) + 2$; push (PCL) $SP \leftarrow (SP) - 1$; push (PCH) $SP \leftarrow (SP) - 1$ $PC \leftarrow (PC) + rel$	—	—	—	—	—	DIR (b5)	1A	dd	5
								DIR (b6)	1C	dd	5
								DIR (b7)	1E	dd	5
								REL	AD	rr	6
CLC	Clear Carry Bit	$C \leftarrow 0$	—	—	—	—	0	INH	98		2
CLI	Clear Interrupt Mask	$I \leftarrow 0$	—	0	—	—	—	INH	9A		2

Instruction Set

Table 11-6. Instruction Set Summary (Sheet 3 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
CLR <i>opr</i> CLRA CLR X CLR <i>opr</i> ,X CLR ,X	Clear Byte	$M \leftarrow \$00$ $A \leftarrow \$00$ $X \leftarrow \$00$ $M \leftarrow \$00$ $M \leftarrow \$00$	—	—	0	1	—	DIR INH INH IX1 IX	3F 4F 5F 6F 7F	dd ff	5 3 3 6 5
CMP # <i>opr</i> CMP <i>opr</i> CMP <i>opr</i> CMP <i>opr</i> ,X CMP <i>opr</i> ,X CMP ,X	Compare Accumulator with Memory Byte	(A) – (M)	—	—	↑	↑	↑	IMM DIR EXT IX2 IX1 IX	A1 B1 C1 D1 E1 F1	ii dd hh ll ee ff ff	2 3 4 5 4 3
COM <i>opr</i> COMA COMX COM <i>opr</i> ,X COM ,X	Complement Byte (One's Complement)	$M \leftarrow \overline{(M)} = \$FF - (M)$ $A \leftarrow \overline{(A)} = \$FF - (A)$ $X \leftarrow \overline{(X)} = \$FF - (X)$ $M \leftarrow \overline{(M)} = \$FF - (M)$ $M \leftarrow \overline{(M)} = \$FF - (M)$	—	—	↑	↑	1	DIR INH INH IX1 IX	33 43 53 63 73	dd ff	5 3 3 6 5
CPX # <i>opr</i> CPX <i>opr</i> CPX <i>opr</i> CPX <i>opr</i> ,X CPX <i>opr</i> ,X CPX ,X	Compare Index Register with Memory Byte	(X) – (M)	—	—	↑	↑	↑	IMM DIR EXT IX2 IX1 IX	A3 B3 C3 D3 E3 F3	ii dd hh ll ee ff ff	2 3 4 5 4 3
DEC <i>opr</i> DECA DECX DEC <i>opr</i> ,X DEC ,X	Decrement Byte	$M \leftarrow (M) - 1$ $A \leftarrow (A) - 1$ $X \leftarrow (X) - 1$ $M \leftarrow (M) - 1$ $M \leftarrow (M) - 1$	—	—	↑	↑	—	DIR INH INH IX1 IX	3A 4A 5A 6A 7A	dd ff	5 3 3 6 5
EOR # <i>opr</i> EOR <i>opr</i> EOR <i>opr</i> EOR <i>opr</i> ,X EOR <i>opr</i> ,X EOR ,X	EXCLUSIVE OR Accumulator with Memory Byte	$A \leftarrow (A) \oplus (M)$	—	—	↑	↑	—	IMM DIR EXT IX2 IX1 IX	A8 B8 C8 D8 E8 F8	ii dd hh ll ee ff ff	2 3 4 5 4 3
INC <i>opr</i> INCA INCX INC <i>opr</i> ,X INC ,X	Increment Byte	$M \leftarrow (M) + 1$ $A \leftarrow (A) + 1$ $X \leftarrow (X) + 1$ $M \leftarrow (M) + 1$ $M \leftarrow (M) + 1$	—	—	↑	↑	—	DIR INH INH IX1 IX	3C 4C 5C 6C 7C	dd ff	5 3 3 6 5
JMP <i>opr</i> JMP <i>opr</i> JMP <i>opr</i> ,X JMP <i>opr</i> ,X JMP ,X	Unconditional Jump	PC ← Jump Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff	2 3 4 3 2

Table 11-6. Instruction Set Summary (Sheet 4 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
JSR <i>opr</i> JSR <i>opr</i> JSR <i>opr</i> ,X JSR <i>opr</i> ,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Effective Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	5 6 7 6 5
LDA # <i>opr</i> LDA <i>opr</i> LDA <i>opr</i> LDA <i>opr</i> ,X LDA <i>opr</i> ,X LDA ,X	Load Accumulator with Memory Byte	A ← (M)	—	—	↑	↑	—	IMM DIR EXT IX2 IX1 IX	A6 B6 C6 D6 E6 F6	ii dd hh ll ee ff ff	2 3 4 5 4 3
LDX # <i>opr</i> LDX <i>opr</i> LDX <i>opr</i> LDX <i>opr</i> ,X LDX <i>opr</i> ,X LDX ,X	Load Index Register with Memory Byte	X ← (M)	—	—	↑	↑	—	IMM DIR EXT IX2 IX1 IX	AE BE CE DE EE FE	ii dd hh ll ee ff ff	2 3 4 5 4 3
LSL <i>opr</i> LSLA LSLX LSL <i>opr</i> ,X LSL ,X	Logical Shift Left (Same as ASL)		—	—	↑	↑	↑	DIR INH INH IX1 IX	38 48 58 68 78	dd ff	5 3 3 6 5
LSR <i>opr</i> LSRA LSRX LSR <i>opr</i> ,X LSR ,X	Logical Shift Right		—	—	0	↑	↑	DIR INH INH IX1 IX	34 44 54 64 74	dd ff	5 3 3 6 5
MUL	Unsigned Multiply	X : A ← (X) × (A)	0	—	—	—	0	INH	42		11
NEG <i>opr</i> NEGA NEGX NEG <i>opr</i> ,X NEG ,X	Negate Byte (Two's Complement)	M ← -(M) = \$00 - (M) A ← -(A) = \$00 - (A) X ← -(X) = \$00 - (X) M ← -(M) = \$00 - (M) M ← -(M) = \$00 - (M)	—	—	↑	↑	↑	DIR INH INH IX1 IX	30 40 50 60 70	dd ff	5 3 3 6 5
NOP	No Operation		—	—	—	—	—	INH	9D		2
ORA # <i>opr</i> ORA <i>opr</i> ORA <i>opr</i> ORA <i>opr</i> ,X ORA <i>opr</i> ,X ORA ,X	Logical OR Accumulator with Memory	A ← (A) ∨ (M)	—	—	↑	↑	—	IMM DIR EXT IX2 IX1 IX	AA BA CA DA EA FA	ii dd hh ll ee ff ff	2 3 4 5 4 3
ROL <i>opr</i> ROLA ROLX ROL <i>opr</i> ,X ROL ,X	Rotate Byte Left through Carry Bit		—	—	↑	↑	↑	DIR INH INH IX1 IX	39 49 59 69 79	dd ff	5 3 3 6 5

Instruction Set

Table 11-6. Instruction Set Summary (Sheet 5 of 6)

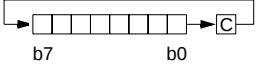
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ROR <i>opr</i> RORA RORX ROR <i>opr</i> ,X ROR ,X	Rotate Byte Right through Carry Bit		—	—	↑	↑	↑	DIR INH INH IX1 IX	36 46 56 66 76	dd ff	5 3 3 6 5
RSP	Reset Stack Pointer	SP ← \$00FF	—	—	—	—	—	INH	9C		2
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↑	↑	↑	↑	↑	INH	80		9
RTS	Return from Subroutine	SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	—	—	—	—	—	INH	81		6
SBC # <i>opr</i> SBC <i>opr</i> SBC <i>opr</i> SBC <i>opr</i> ,X SBC <i>opr</i> ,X SBC ,X	Subtract Memory Byte and Carry Bit from Accumulator	A ← (A) – (M) – (C)	—	—	↑	↑	↑	IMM DIR EXT IX2 IX1 IX	A2 B2 C2 D2 E2 F2	ii dd hh ll ee ff ff	2 3 4 5 4 3
SEC	Set Carry Bit	C ← 1	—	—	—	—	1	INH	99		2
SEI	Set Interrupt Mask	I ← 1	—	1	—	—	—	INH	9B		2
STA <i>opr</i> STA <i>opr</i> STA <i>opr</i> ,X STA <i>opr</i> ,X STA ,X	Store Accumulator in Memory	M ← (A)	—	—	↑	↑	—	DIR EXT IX2 IX1 IX	B7 C7 D7 E7 F7	dd hh ll ee ff ff	4 5 6 5 4
STOP	Stop Oscillator and Enable IRQ Pin		—	0	—	—	—	INH	8E		2
STX <i>opr</i> STX <i>opr</i> STX <i>opr</i> ,X STX <i>opr</i> ,X STX ,X	Store Index Register In Memory	M ← (X)	—	—	↑	↑	—	DIR EXT IX2 IX1 IX	BF CF DF EF FF	dd hh ll ee ff ff	4 5 6 5 4
SUB # <i>opr</i> SUB <i>opr</i> SUB <i>opr</i> SUB <i>opr</i> ,X SUB <i>opr</i> ,X SUB ,X	Subtract Memory Byte from Accumulator	A ← (A) – (M)	—	—	↑	↑	↑	IMM DIR EXT IX2 IX1 IX	A0 B0 C0 D0 E0 F0	ii dd hh ll ee ff ff	2 3 4 5 4 3
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	—	1	—	—	—	INH	83		10

Table 11-6. Instruction Set Summary (Sheet 6 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
TAX	Transfer Accumulator to Index Register	$X \leftarrow (A)$	—	—	—	—	—	INH	97		2
TST <i>opr</i> TSTA TSTX TST <i>opr</i> ,X TST ,X	Test Memory Byte for Negative or Zero	(M) – \$00	—	—	↓	↓	—	DIR INH INH IX1 IX	3D 4D 5D 6D 7D	dd ff	4 3 3 5 4
TXA	Transfer Index Register to Accumulator	$A \leftarrow (X)$	—	—	—	—	—	INH	9F		2
WAIT	Stop CPU Clock and Enable Interrupts		—	0	—	—	—	INH	8F		2

A	Accumulator	<i>opr</i>	Operand (one or two bytes)
C	Carry/borrow flag	PC	Program counter
CCR	Condition code register	PCH	Program counter high byte
dd	Direct address of operand	PCL	Program counter low byte
dd rr	Direct address of operand and relative offset of branch instruction	REL	Relative addressing mode
DIR	Direct addressing mode	<i>rel</i>	Relative program counter offset byte
ee ff	High and low bytes of offset in indexed, 16-bit offset addressing	rr	Relative program counter offset byte
EXT	Extended addressing mode	SP	Stack pointer
ff	Offset byte in indexed, 8-bit offset addressing	X	Index register
H	Half-carry flag	Z	Zero flag
hh ll	High and low bytes of operand address in extended addressing	#	Immediate value
I	Interrupt mask	^	Logical AND
ii	Immediate operand byte	∨	Logical OR
IMM	Immediate addressing mode	⊕	Logical EXCLUSIVE OR
INH	Inherent addressing mode	()	Contents of
IX	Indexed, no offset addressing mode	—()	Negation (two's complement)
IX1	Indexed, 8-bit offset addressing mode	←	Loaded with
IX2	Indexed, 16-bit offset addressing mode	?	If
M	Memory location	:	Concatenated with
N	Negative flag	↑	Set or cleared
n	Any bit	—	Not affected

11.6 Opcode Map

See [Table 11-7](#).

Advance Information

MOTOROLA

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Section 12. Electrical Specifications

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Electrical Specifications

12.2 Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table below. Keep V_{In} and V_{Out} within the range $V_{SS} \leq (V_{In} \text{ or } V_{Out}) \leq V_{DD}$. Connect unused inputs to the appropriate voltage level, either V_{SS} or V_{DD} .

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.3 to +7.0	V
Input voltage Normal operation Bootloader mode ($\overline{IRQ}$ pin only)	V_{In}	$V_{SS} - 0.3$ to $V_{DD} + 0.3$ $V_{SS} - 0.3$ to $2 \times V_{DD} + 0.3$	V
Current drain per pin (Excluding V_{DD} and V_{SS})	I	25	mA
Storage temperature range	T_{STG}	-65 to +150	°C

NOTE: This device is not guaranteed to operate properly at the maximum ratings. Refer to [12.6 5.0-Vdc Electrical Characteristics](#) for guaranteed operating conditions.

12.3 Operating Temperature

Characteristic	Symbol	Value	Unit
Operating temperature range	T_A	-40 to +85	°C

12.4 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance plastic dual in-line (PDIP)	θ_{JA}	60	°C/W
Thermal resistance plastic leaded chip carrier (PLCC)	θ_{JA}	70	°C/W
Thermal resistance quad flat pack (QFP)	θ_{JA}	95	°C/W
Thermal resistance plastic shrink DIP (SDIP)	θ_{JA}	60	°C/W

12.5 Power Considerations

The average chip-junction temperature, T_J , in °C, can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$ watts (chip internal power)

$P_{I/O}$ = Power dissipation on input and output pins (user determined)

For most applications $P_{I/O} \ll P_{INT}$ and can be neglected.

The following is an approximate relationship between P_D and T_J (neglecting P_J):

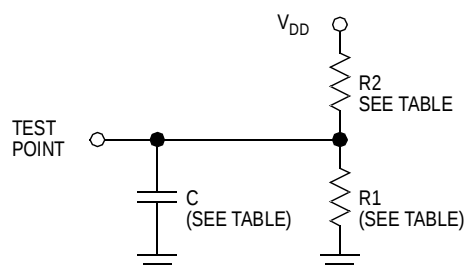
$$P_D = K \div (T_J + 273 \text{ °C}) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273 \text{ °C}) + \theta_{JA} \times (P_D)^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

Electrical Specifications



$V_{DD} = 4.5 \text{ V}$

Pins	R1	R2	C
PA7–PA0 PB7–PB0 PC7–PC0 PD5–PD0, PD7	3.26 Ω	2.38 Ω	50 pF

$V_{DD} = 3.0 \text{ V}$

Pins	R1	R2	C
PA7–PA0 PB7–PB0 PC7–PC0 PD5–PD0, PD7	10.91 Ω	6.32 Ω	50 pF

Figure 12-1. Test Load

12.6 5.0-Vdc Electrical Characteristics

Characteristic ⁽¹⁾	Symbol	Min	Typ ⁽²⁾	Max	Unit
Output voltage $I_{Load} = 10.0 \mu A$ $I_{Load} = -10.0 \mu A$	V_{OL} V_{OH}	— $V_{DD} - 0.1$	— —	0.1 —	V
Output high voltage ($I_{Load} = -0.8 \text{ mA}$) PA7–PA0, PB7–PB0, PC6–PC0, TCMP, PD7, PD0 ($I_{Load} = -1.6 \text{ mA}$) PD5–PD1 ($I_{Load} = -5.0 \text{ mA}$) PC7	V_{OH}	$V_{DD} - 0.8$ $V_{DD} - 0.8$ $V_{DD} - 0.8$	— — —	— — —	V
Output low voltage ($I_{Load} = 1.6 \text{ mA}$) PA7–PA0, PB7–PB0, PC6–PC0, PD7, PD5–PD0, TCMP ($I_{Load} = 10 \text{ mA}$) PC7	V_{OL}	— —	— —	0.4 0.4	V
Input high voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, IRQ, RESET, OSC1	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input low voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, IRQ, RESET, OSC1	V_{IL}	V_{SS}	—	$0.2 \times V_{DD}$	V
Supply current (4.5–5.5 Vdc @ $f_{OP} = 2.1 \text{ MHz}$) Run ⁽³⁾ Wait ⁽⁴⁾ Stop ⁽⁵⁾ 25°C –40 to 85 °C	I_{DD}	— — — —	3.5 1.0 1.0 7.0	5.25 3.25 20.0 50.0	mA mA μA μA
I/O ports hi-Z leakage current PA7–PA0, PB7–PB0 (without pullup) PC7–PC0, PD7, PD5–PD0	I_{OZ}	—	—	10	μA
Input current RESET, IRQ, OSC1, TCAP, PD7, PD5–PD0	I_{IN}	—	—	1	μA
Input pullup current ⁽⁶⁾ PB7–PB0 (with pullup)	I_{IN}	5	—	60	μA
Capacitance Ports (as input or output) RESET, IRQ, OSC1, TCAP, PD7, PD5, PD0	C_{Out} C_{In}	— —	— —	12 8	pF
Programming voltage (25°C)	V_{PP}	15.0	16.0	17.0	V
Programming current (25°C)	I_{PP}	—	—	200	mA

1. $V_{DD} = 5.0 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = -40$ to $+85^\circ\text{C}$, unless otherwise noted

2. Typical values reflect measurements taken on average processed devices at the midpoint of voltage range, 25 °C only.

3. Run (operating) I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, port B = V_{DD} , all other inputs $V_{IL} = 0.2 \text{ V}$, $V_{IH} = V_{DD} - 0.2 \text{ V}$; no DC loads; less than 50 pF on all outputs; $C_L = 20 \text{ pF}$ on OSC24. Wait I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, port B = V_{DD} , all other inputs $V_{IL} = 0.2 \text{ V}$, $V_{IH} = V_{DD} - 0.2 \text{ V}$; no DC loads; less than 50 pF on all outputs; $C_L = 20 \text{ pF}$ on OSC2. Wait I_{DD} is affected linearly by the OSC2 capacitance.5. Stop I_{DD} measured with OSC1 = 0.2 V; all I/O pins configured as inputs, port B = V_{DD} , all other inputs $V_{IL} = 0.2 \text{ V}$, $V_{IH} = V_{DD} - 0.2 \text{ V}$.6. Input pullup current measured with $V_{IL} = 0.2 \text{ V}$.

Electrical Specifications

12.7 3.3-Vdc Electrical Characteristics

Characteristic ⁽¹⁾	Symbol	Min	Typ ⁽²⁾	Max	Unit
Output voltage $I_{Load} = 10.0 \mu A$ $I_{Load} = -10.0 \mu A$	V_{OL} V_{OH}	— $V_{DD} - 0.1$	— —	0.1 —	V
Output high voltage ($I_{Load} = -0.2 \text{ mA}$) PA7–PA0, PB7–PB0, PC6–PC0, TCMP, PD7, PD0 ($I_{Load} = -0.4 \text{ mA}$) PD5–PD1 ($I_{Load} = -1.5 \text{ mA}$) PC7	V_{OH}	$V_{DD} - 0.3$ $V_{DD} - 0.3$ $V_{DD} - 0.3$	— — —	— — —	V
Output low voltage ($I_{Load} = 0.4 \text{ mA}$) PA7–PA0, PB7–PB0, PC6–PC0, PD7, PD5–PD0, TCMP ($I_{Load} = 6 \text{ mA}$) PC7	V_{OL}	— —	— —	0.3 0.3	V
Input high voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, IRQ, RESET, OSC1	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input low voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, IRQ, RESET, OSC1	V_{IL}	V_{SS}	—	$0.2 \times V_{DD}$	V
Supply current (3.0–3.6 Vdc @ $f_{OP} = 1.0 \text{ MHz}$) Run ⁽³⁾ Wait ⁽⁴⁾ Stop ⁽⁵⁾ 25°C –40 to 85°C	I_{DD}	— — — —	1.0 500 1.0 2.5	1.6 900 8 20	mA μA μA μA
I/O ports hi-Z leakage current PA7–PA0, PB7–PB0 (without pullup) PC7–PC0, PD7, PD5–PD0	I_{OZ}	—	—	10	μA
Input current RESET, IRQ, OSC1, TCAP, PD7, PD5–PD0	I_{In}	—	—	1	μA
Input pullup current ⁽⁶⁾ PB7–PB0 (with pullup)	I_{In}	0.5	—	20	μA
Capacitance Ports (as input or output) RESET, IRQ, OSC1, TCAP, PD7, PD5, PD0	C_{Out} C_{In}	— —	— —	12 8	pF

1. $V_{DD} = 3.3 \text{ Vdc} \pm 0.3 \text{ Vdc}$, $V_{SS} = 0 \text{ Vdc}$, $T_A = -40$ to $+85^\circ\text{C}$, unless otherwise noted

2. Typical values reflect measurements taken on average processed devices at the midpoint of voltage range, 25°C only.

3. Run (operating) I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, port B = V_{DD} , all other inputs $V_{IL} = 0.2 \text{ V}$, $V_{IH} = V_{DD} - 0.2 \text{ V}$; no DC loads; less than 50 pF on all outputs; $C_L = 20 \text{ pF}$ on OSC2

4. Wait I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, port B = V_{DD} , all other inputs $V_{IL} = 0.2 \text{ V}$, $V_{IH} = V_{DD} - 0.2 \text{ V}$; no DC loads; less than 50 pF on all outputs; $C_L = 20 \text{ pF}$ on OSC2. Wait I_{DD} is affected linearly by the OSC2 capacitance.

5. Stop I_{DD} measured with OSC1 = 0.2 V ; all I/O pins configured as inputs, port B = V_{DD} , all other inputs $V_{IL} = 0.2 \text{ V}$, $V_{IH} = V_{DD} - 0.2 \text{ V}$.

6. Input pullup current measured with $V_{IL} = 0.2 \text{ V}$.

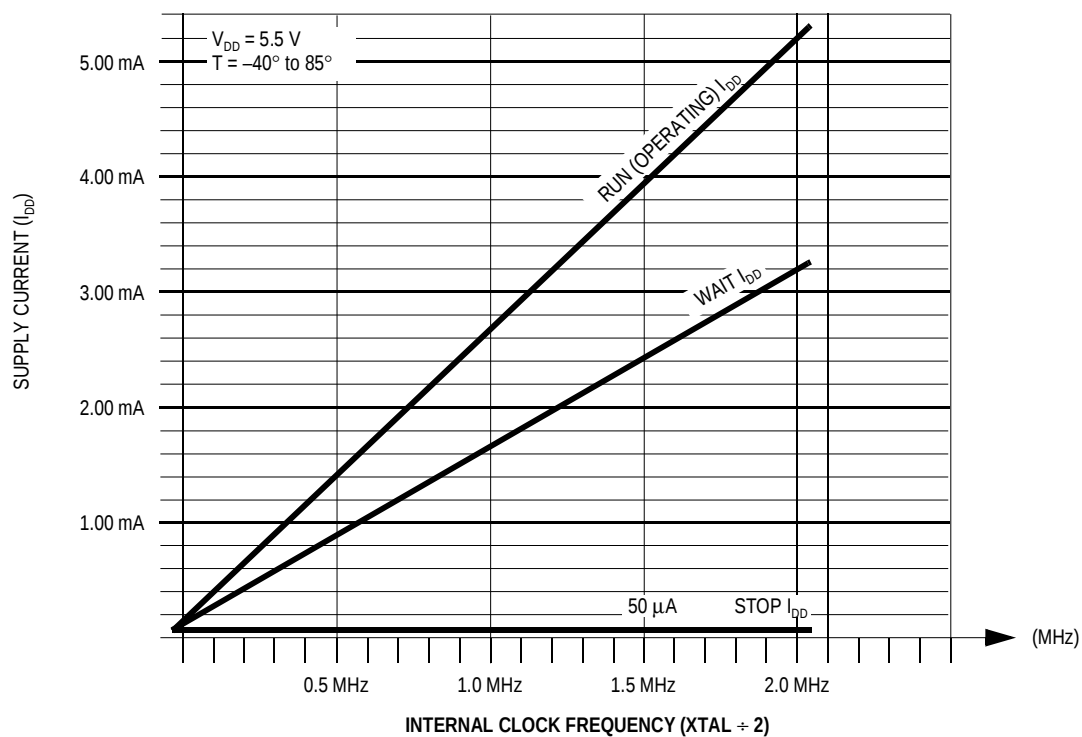


Figure 12-2. Maximum Supply Current vs Internal Clock Frequency, $V_{DD} = 5.5$ V

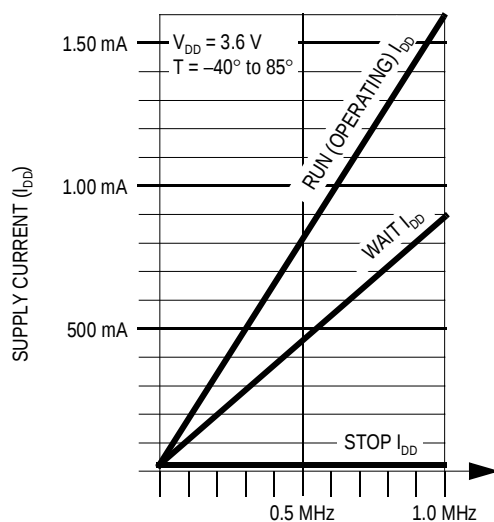


Figure 12-3. Maximum Supply Current vs Internal Clock Frequency, $V_{DD} = 3.6$ V

Electrical Specifications

12.8 5.0-Vdc Control Timing

Characteristic ⁽¹⁾	Symbol	Min	Max	Unit
Frequency of operation Crystal External clock	f_{OSC}	— DC	4.2 4.2	MHz
Internal pperating frequency ($f_{OSC} \div 2$) Crystal External clock	f_{OP}	— DC	2.1 2.1	MHz
Cycle time	t_{CYC}	480	—	ns
Crystal oscillator startup time	t_{OXOV}	—	100	ms
Stop recovery startup time (crystal oscillator)	t_{ILCH}	—	100	ms
$\overline{RESET}$ pulse width	t_{RL}	1.5	—	t_{CYC}
Timer Resolution ⁽²⁾ Input capture pulse width Input capture pulse period	t_{RESL} t_{TH}, t_{TL} t_{TLTL}	4.0 125 (3)	— — —	t_{CYC} ns t_{CYC}
Interrupt pulse width low (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	90	—	ns

1. $V_{DD} = 5.0 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = -40$ to $+85^\circ\text{C}$, unless otherwise noted

2. Because a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.

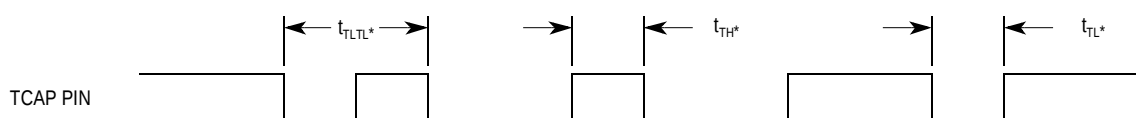
3. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus $24 t_{CYC}$.

4. The minimum t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus $19 t_{CYC}$.

12.9 3.3-Vdc Control Timing

Characteristic ⁽¹⁾	Symbol	Min	Max	Unit
Frequency of operation Crystal External clock	f_{OSC}	— DC	2.0 2.0	MHz
Internal operating frequency ($f_{OSC} \div 2$) Crystal External clock	f_{OP}	— DC	1.0 1.0	MHz
Cycle time	t_{CYC}	1000	—	ns
Crystal oscillator startup time	t_{OXOV}	—	100	ms
Stop recovery startup time (crystal oscillator)	t_{ILCH}	—	100	ms
$\overline{RESET}$ pulse width	t_{RL}	1.5	—	t_{CYC}
Timer Resolution ⁽²⁾ Input capture pulse width Input capture pulse period	t_{RESL} t_{TH}, t_{TL} t_{TLTL}	4.0 125 (3)	— — —	t_{CYC} ns t_{CYC}
Interrupt pulse width low (edge-triggered)	t_{ILIH}	250	—	ns
Interrupt pulse period	t_{ILIL}	(4)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	200	—	ns

1. $V_{DD} = 3.3Vdc \pm 0.3 Vdc$, $V_{SS} = 0 Vdc$, $T_A = -40$ to $+85^\circ C$, unless otherwise noted
2. Because a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
3. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus $24 t_{CYC}$.
4. The minimum t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus $19 t_{CYC}$.



* Refer to timer resolution data in [12.8 5.0-Vdc Control Timing](#) and [12.9 3.3-Vdc Control Timing](#).

Figure 12-4. TCAP Timing Relationships

Electrical Specifications

12.10 5.0-Vdc Serial Peripheral Interface Timing

No.	Characteristic ⁽¹⁾	Symbol	Min	Max	Unit
	Operating frequency Master Slave	$f_{OP(M)}$ $f_{OP(S)}$	dc dc	0.5 2.1	f_{OP} MHz
1	Cycle time Master Slave	$t_{CYC(M)}$ $t_{CYC(S)}$	2.0 480	— —	t_{CYC} ns
2	Enable lead time Master Slave	$t_{LEAD(M)}$ $t_{LEAD(S)}$	(2) 240	— —	ns
3	Enable lag time Master Slave	$t_{LAG(M)}$ $t_{LAG(S)}$	(2) 720	— —	ns
4	Clock (SCK) high time Master Slave	$t_{W(SCKH)M}$ $t_{W(SCKH)S}$	340 190	— —	ns
5	Clock (SCK) low time Master Slave	$t_{W(SCKL)M}$ $t_{W(SCKL)S}$	340 190	— —	ns
6	Data setup time (inputs) Master Slave	$t_{SU(M)}$ $t_{SU(S)}$	100 100	— —	ns
7	Data hold time (inputs) Master Slave	$t_{H(M)}$ $t_{H(S)}$	100 100	— —	ns
8	Slave access time (time to data active from high-impedance state)	t_A	0	120	ns
9	Slave disable time (hold time to high-impedance state)	t_{DIS}	—	240	ns
10	Data valid Master (before capture edge) Slave (after enable edge) ⁽³⁾	$t_{V(M)}$ $t_{V(S)}$	0.25 —	— 240	$t_{CYC(M)}$ ns
11	Data hold time (outputs) Master (after capture edge) slave (After Enable Edge)	$t_{HO(M)}$ $t_{HO(S)}$	0.25 0	— —	$t_{CYC(M)}$ ns
12	Rise time (20% V_{DD} to 70% V_{DD} , $C_L = 200$ pF) SPI outputs (SCK, MOSI, and MISO) SPI inputs (SCK, MOSI, MISO, and SS)	t_{RM} t_{RS}	— —	100 2.0	ns μ s
13	Fall time (70% V_{DD} to 20% V_{DD} , $C_L = 200$ pF) SPI outputs (SCK, MOSI, and MISO) SPI inputs (SCK, MOSI, MISO, and SS)	t_{FM} t_{FS}	— —	100 2.0	ns μ s

1. $V_{DD} = 5.0$ Vdc $\pm 10\%$; $V_{SS} = 0$ Vdc, $T_A = -40$ to $+85^\circ\text{C}$, unless otherwise noted. Refer to [Figure 12-9](#) and [Figure 12-10](#).

2. Signal production depends on software.

3. Assumes 200 pF load on all SPI pins.

12.11 3.3- Vdc Serial Peripheral Interface Timing

No.	Characteristic ⁽¹⁾	Symbol	Min	Max	Unit
	Operating frequency Master Slave	$f_{OP(M)}$ $f_{OP(S)}$	dc dc	0.5 1.0	f_{OP} MHz
1	Cycle time Master Slave	$t_{CYC(M)}$ $t_{CYC(S)}$	2.0 1.0	— —	t_{CYC} μ s
2	Enable lead time Master Slave	$t_{LEAD(M)}$ $t_{LEAD(S)}$	(2) 500	— —	ns
3	Enable lag time Master Slave	$t_{LAG(M)}$ $t_{LAG(S)}$	(2) 1.5	— —	ns μ s
4	Clock (SCK) high time Master Slave	$t_{W(SCKH)M}$ $t_{W(SCKH)S}$	720 400	— —	ns
5	Clock (SCK) low time Master Slave	$t_{W(SCKL)M}$ $t_{W(SCKL)S}$	720 400	— —	ns
6	Data setup time (inputs) Master Slave	$t_{SU(M)}$ $t_{SU(S)}$	200 200	— —	ns
7	Data hold time (inputs) Master Slave	$t_{H(M)}$ $t_{H(S)}$	200 200	— —	ns
8	Slave access time (time to data active from high-impedance state)	t_A	0	250	ns
9	Slave disable time (hold time to high-impedance state)	t_{DIS}	—	500	ns
10	Data valid Master (before capture edge) Slave (after enable edge) ⁽³⁾	$t_{V(M)}$ $t_{V(S)}$	0.25 —	— 500	$t_{CYC(M)}$ ns
11	Data hold time (outputs) Master (after capture edge) Slave (after enable edge)	$t_{HO(M)}$ $t_{HO(S)}$	0.25 0	— —	$t_{CYC(M)}$ ns
12	Rise time (20% V_{DD} to 70% V_{DD} , $C_L = 200$ pF) SPI outputs (SCK, MOSI, and MISO) SPI inputs (SCK, MOSI, MISO, and SS)	t_{RM} t_{RS}	— —	200 2.0	ns μ s
13	Fall time (70% V_{DD} to 20% V_{DD} , $C_L = 200$ pF) SPI outputs (SCK, MOSI, and MISO) SPI inputs (SCK, MOSI, MISO, and SS)	t_{FM} t_{FS}	— —	200 2.0	ns μ s

1. $V_{DD} = 3.3$ Vdc ± 0.3 Vdc; $V_{SS} = 0$ Vdc, $T_A = -40$ to $+85$ °C, unless otherwise noted. Refer to [Figure 12-9](#) and [Figure 12-10](#).

2. Signal production depends on software.

3. Assumes 200 pF load on all SPI pins.

Mechanical Specifications

13.6 44-Lead Quad Flat Pack (QFP) (Case 824A-01)

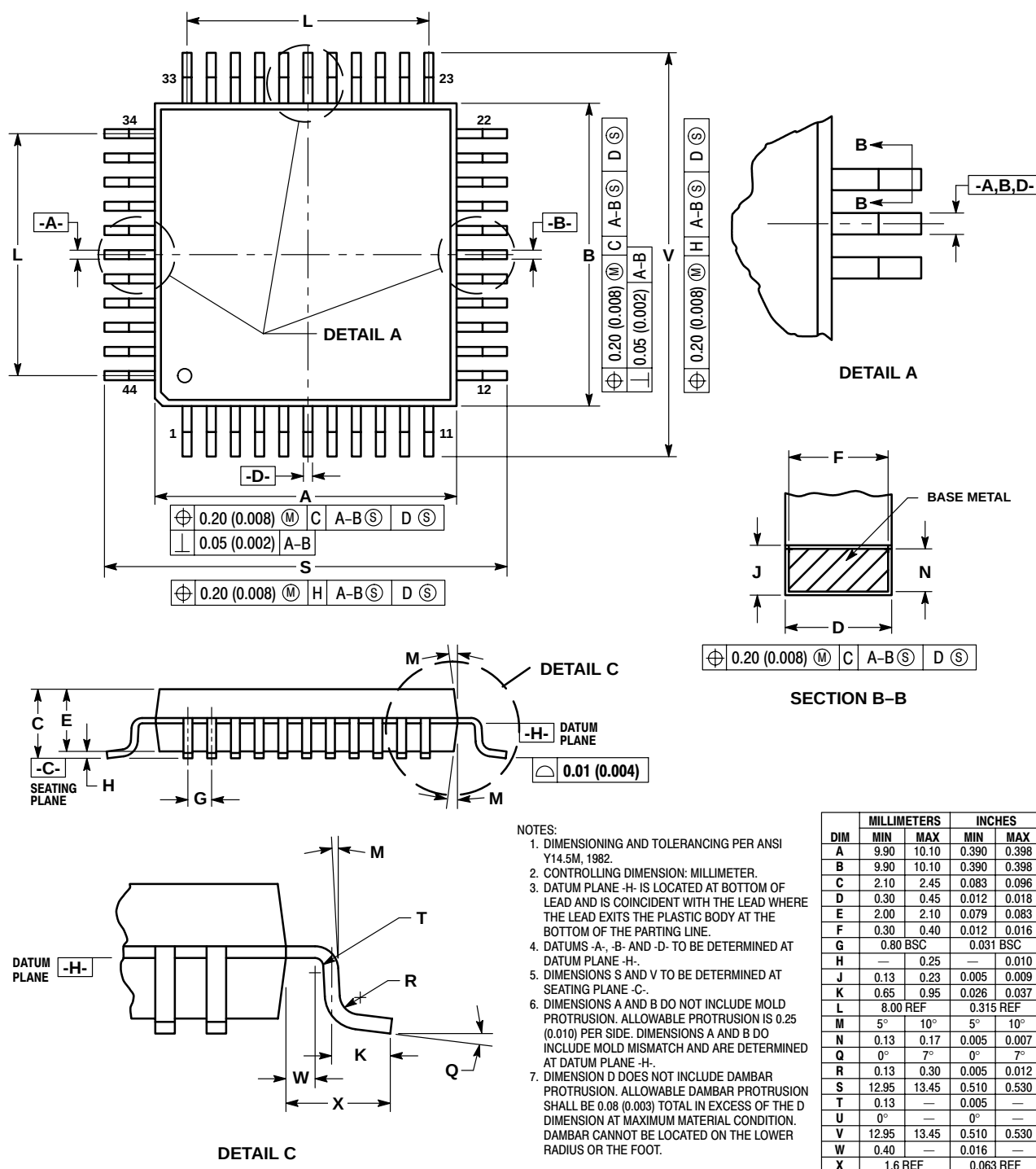


Figure 13-4. 44-Lead QFP (Case 824A-01)

Section 14. Ordering Information

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14.2 Introduction

This section contains ordering information for the available package types.

14.3 MC Order Numbers

Table 14-1 shows the MC order numbers for the available package types.

Table 14-1. MC Order Numbers

Package Type	Temperature Range	Order Number
40-pin plastic dual in-line package (DIP)	–40°C to 85°C	MC68HC705C9ACP
42-pin shrink dual in-line package (SDIP)	–40°C to 85°C	MC68HC705C9ACB
44-lead plastic leaded chip carrier (PLCC)	–40°C to 85°C	MC68HC705C9ACFN
44-pin quad flat pack (QFP)	–40°C to 85°C	MC68HC705C9ACFB

P = Plastic dual in-line package (PDIP)

B = Shrink dual in-line package (SDIP)

FN = Plastic-leaded chip carrier (PLCC)

FB = Quad flat pack (QFP)