

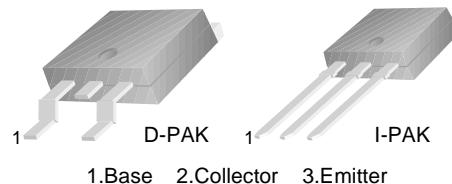


MJD350

MJD350

High Voltage Power Transistors D-PAK for Surface Mount Applications

- Lead Formed for Surface Mount Applications (No Suffix)
- Straight Lead (I-PAK, "- I" Suffix)



PNP Epitaxial Silicon Transistor

Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	- 300	V
V_{CEO}	Collector-Emitter Voltage	- 300	V
V_{EBO}	Emitter-Base Voltage	- 3	V
I_C	Collector Current (DC)	- 0.5	A
I_{CP}	Collector Current (Pulse)	- 0.75	A
P_C	Collector Dissipation ($T_C = 25^\circ\text{C}$)	15	W
	Collector Dissipation ($T_a = 25^\circ\text{C}$)	1.56	W
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature	- 65 ~ 150	$^\circ\text{C}$

Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
$V_{CEO(\text{sus})}$	* Collector-Emitter Sustaining Voltage	$I_C = 1\text{mA}$, $I_B = 0$	-300		V
I_{CEO}	Collector Cut-off Current	$V_{CB} = -300\text{V}$, $I_E = 0$		-0.1	mA
I_{EBO}	Emitter Cut-off Current	$V_{EB} = -3\text{V}$, $I_C = 0$		-0.1	mA
h_{FE}	* DC Current Gain	$V_{CE} = -10\text{V}$, $I_C = -50\text{mA}$	30	240	

* Pulse Test: $PW \leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

Typical Characteristics

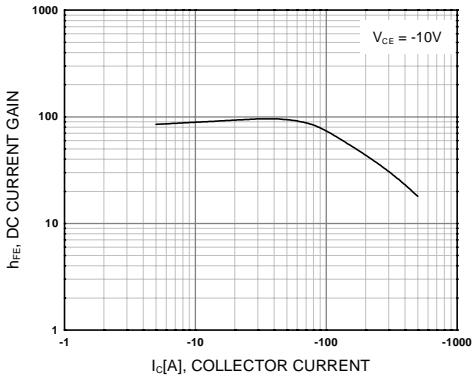


Figure 1. DC current Gain

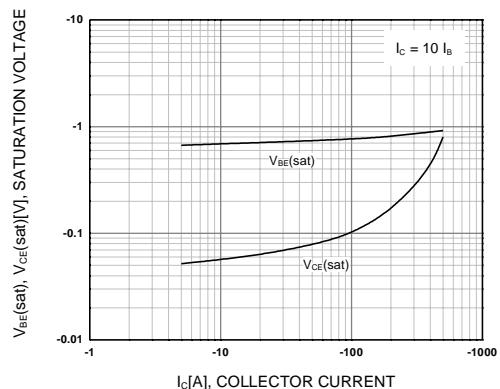


Figure 2. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

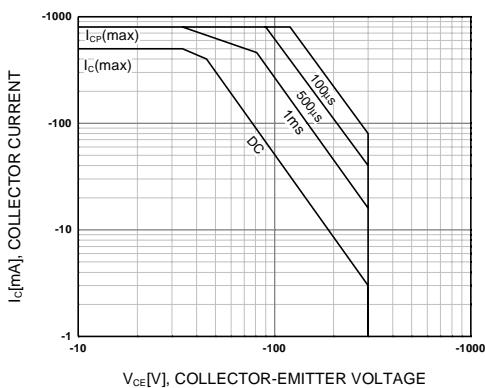


Figure 3. Safe Operating Area

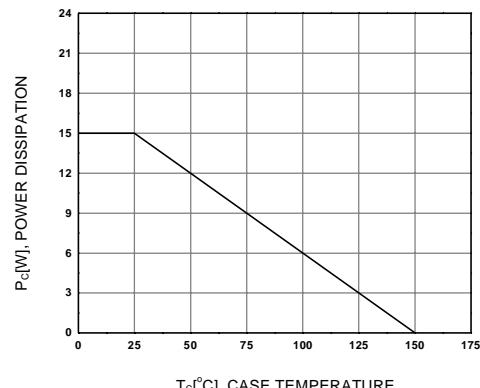
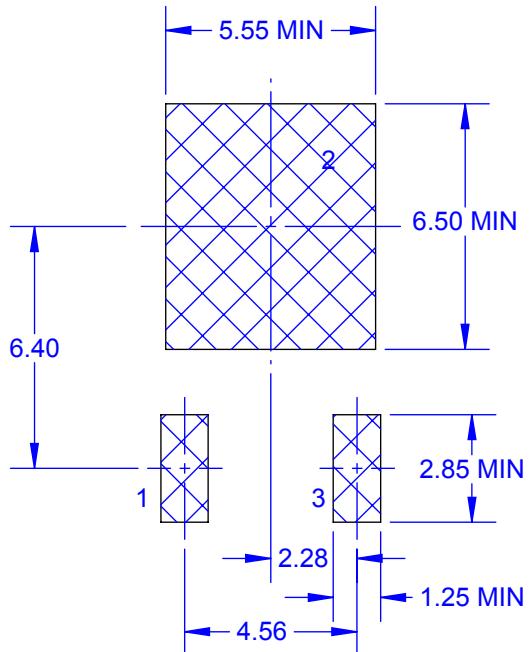
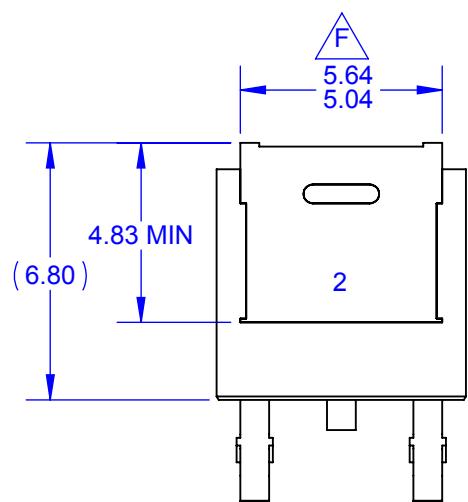
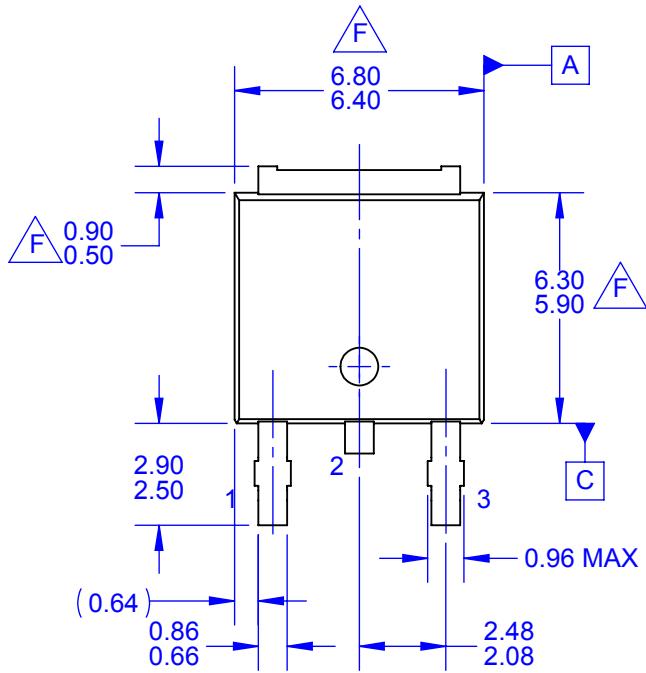
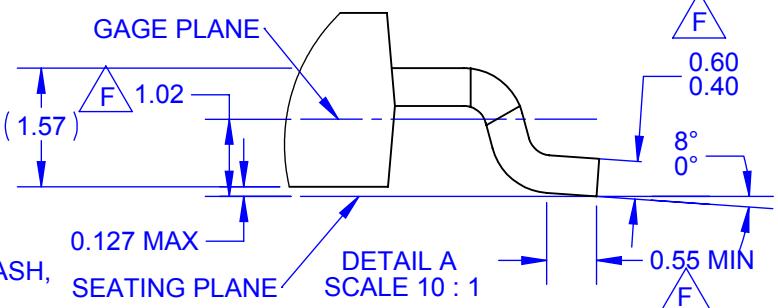
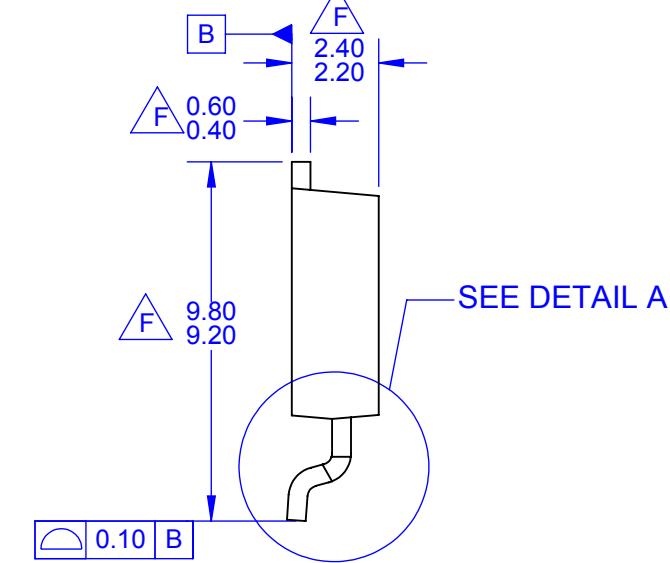


Figure 4. Power Derating



LAND PATTERN RECOMMENDATION



NOTES:UNLESS OTHERWISE SPECIFIED

- A) NOT COMPLIANT TO JEDEC TO-252 VARIATION AB
- B) ALL DIMENSION ARE IN MILLIMETER
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D) LAND PATTERN PER IPC7351A AT STANDARD TO228P991X239-3N
- E) DRAWING FILE NAME: MKT-TO252D03REV3.
- F) DOES NOT COMPLY JEDEC STANDARD VALUE.
- G) FAIRCHILD SEMICONDUCTOR.



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