MP2126

1.25MHz, 2.5A Step-Down Switcher with a 0.5A LDO

The Future of Analog IC Technology

DESCRIPTION

The MP2126 is an internally compensated 2.5A synchronous step-down switcher plus a standalone 0.5A low dropout (LDO) linear regulator. It is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) Battery. The MP2126 can provide up to 2.5A to the switcher output, and 0.5A load current to the LDO output from a 2.5V to 6V input voltage. Both switcher and LDO output voltages can be regulated as low as 0.6V.

The 2.5A switcher features an integrated high-side switch and synchronous rectifier for high efficiency. The switcher operating frequency is internally set at 1.25MHz. With peak current mode control and internal compensation, the MP2126 can be stabilized with ceramic capacitors and small inductors. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The standalone 0.5A LDO output is used to power noise sensitive circuitry. The LDO separate input supply pin (IN2) can be connected to the switcher output to reduce power dissipation and noise from the main switcher.

MP2126 is available in an 8-pin SOIC package with exposed pad.

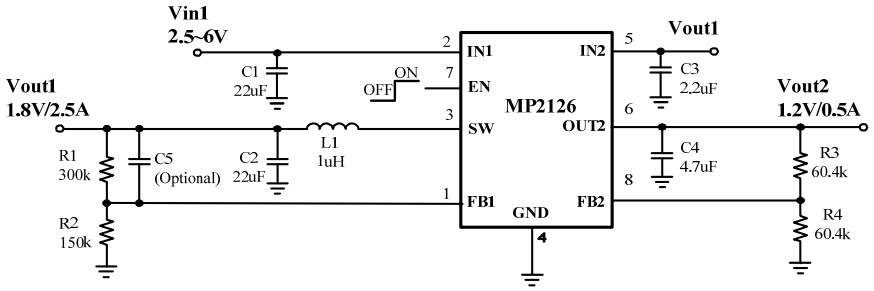
FEATURES

- 2.5A Switcher Output Current
- 0.5A LDO Output Current
- Internal Power MOSFET Switches
- Stable with Ceramic Capacitors
- Up to 90% Efficiency for Switcher
- Switcher Low Dropout Operation: 100% Duty Cycle
- 1μA Shutdown Current
- 1.25MHz Switching Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Short Circuit Protection
- Internal Soft-start for Switcher
- Power On Reset Output
- 2.5V to 6V Input Range V_{IN1} for Switcher
- 1V to V_{IN1} Input Range V_{IN2} for LDO
- Available in 8-pin SOIC with Exposed Pad

APPLICATIONS

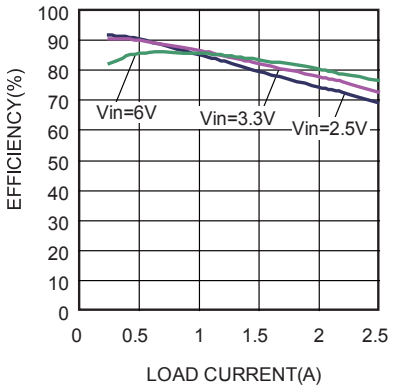
- DVD+/-RW Drives
- LCD TVs
- Industrial Instruments

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT}=1.8V



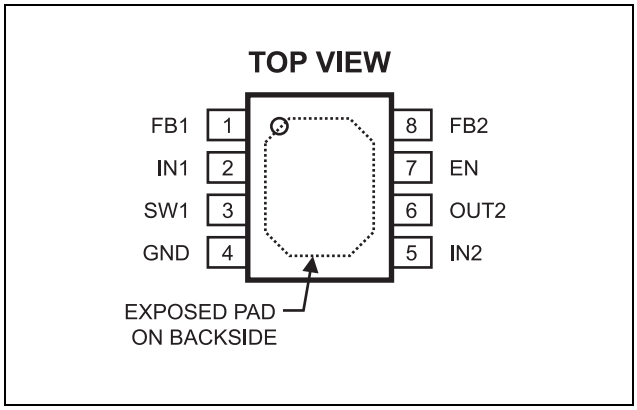
ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP2126DN	SOIC8E	MP2126DN	–40°C to +85°C

*For Tape & Reel, add suffix –Z (e.g. 2126DN–Z).

For RoHS compliant packaging, add suffix –LF (e.g. MP2126DN–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

IN1, OUT1/2 to GND .....–0.3V to + 6.5V
IN2 to GND .....–0.3V to V_{IN1} + 0.3V
SW1 to GND .....–0.3V to V_{IN1} + 0.3V
.....(V_{SW1}>-2.5V, Transient <50ns;
.....V_{SW1}<+8.5V, Transient <50ns)
FB1/2, EN to GND .....–0.3V to +6.5V
Operating Temperature..... –40°C to +85°C
Continuous Power Dissipation (T_A = +25°C)(2)
……..... 2.5W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN1} ..... 2.5V to 6V
Supply Voltage V_{IN2} .....1V to V_{IN1}
Output Voltage V_{OUT} ..... 0.6V to 6V
Operating Temperature .....–40°C to +85°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}
SOIC8E	50	10... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD5 1-7, 4-layer PCB..

ELECTRICAL CHARACTERISTICS (5)

$V_{IN1/2}$ = V_{EN} = 3.6V, T_A = +25°C, unless otherwise noted.

Parameters	Condition	Min	Typ	Max	Units
No Load Supply Current	$V_{IN1/2}$ = 3.6V, V_{EN1}=3.6V, V_{FB1} = 0.65V, V_{FB2} = 0.65V		350	500	µA
Shutdown Current	V_{EN} = 0V, V_{IN1} = 6V, V_{IN2} = 6V		0.01	1	µA
EN Trip Threshold	–40°C ≤ T_A ≤ +85°C	0.3		1.5	V
EN Pull Down Resistor			600		kΩ
Switching Regulator					
IN1 Under Voltage Lockout Threshold	Rising Edge, Hysteresis=0.3V	1.8	2.2		V
Undervoltage Lockout Hysteresis			300		mV
Regulated FB1Voltage	T_A = +25°C	0.584	0.596	0.608	V
	–40°C ≤ T_A ≤ +85°C	0.578	0.596	0.614	
FB1 Input Bias Current	V_{FB1} = 0.65V, –40°C ≤ T_A ≤ +85°C	–50		+50	nA
SW PFET On Resistance	I_{SW} = 100mA		0.20		Ω
SW NFET On Resistance	I_{SW} = –100mA		0.15		Ω
SW Leakage Current	V_{EN} = 0V, V_{IN} = 6V V_{SW1} = 0V or 6V	–5		+5	µA
SW PFET Peak Current Limit	Duty Cycle = 100%, Current Pulse Width < 1ms	2.5	3.3	4.5	A
Oscillator Frequency		1.00	1.25	1.50	MHz
Linear Regulator LDO					
IN2 Input Range	I_{LOAD2} = 10mA, V_{OUT2}=V_{FB2}	1.1		V_{IN1}	V
Regulated FB2 Voltage	T_A = +25°C	0.588	0.600	0.612	V
	–40°C ≤ T_A ≤ +85°C	0.582	0.600	0.618	
FB2 Input Bias Current	V_{FB2} = 0.6V	–50		+50	nA
OUT2 Output Current	V_{OUT2} = 1.2V	500			mA
OUT2 Short Protection	V_{OUT2} = 0V	625	725		mA
Dropout Voltage (6)	I_{LOAD} = 0.3A, V_{OUT2} = 1.2V		250		mV
Thermal Shutdown					
Thermal Shutdown Trip Threshold			150		°C
Thermal Shutdown Hysteresis			20		°C

Notes:

5) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

6) Dropout voltage is defined as the input-to-output differential when the output voltage drops 3% below the normal output voltage.

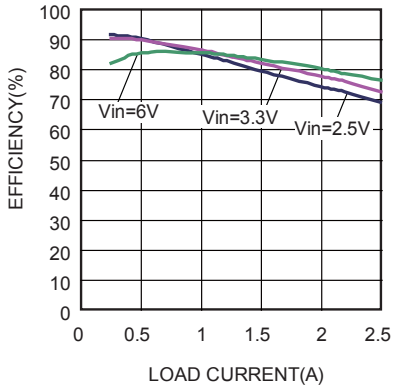
PIN FUNCTIONS

Pin #	Name	Description
1	FB1	Feedback Input for the switcher output VOUT1.
2	IN1	Main Input Supply Pin. Input supply for both the switcher and the low dropout (LDO) linear regulator.
3	SW1	Switcher switch node.
4	GND	Ground.
5	IN2	Input Supply for the auxiliary linear regulator LDO output power device.
6	OUT2	Output of the 500mA LDO. The LDO is designed to be stable with an external minimum 4.7µF ceramic capacitor at 500mA load current.
7	EN	Enable Input. Enable both the switcher and the linear regulator LDO.
8	FB2	Feedback Input for the linear regulator output VOUT2.

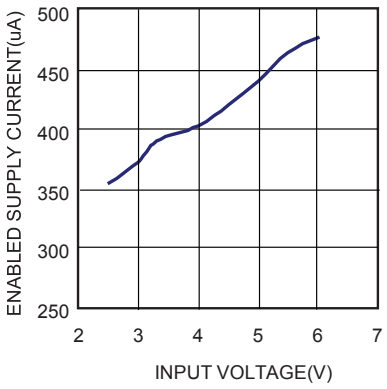
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT1} = 1.8V,V_{OUT2} = 1.2V, L=1uH, T_A = +25ºC, unless otherwise noted

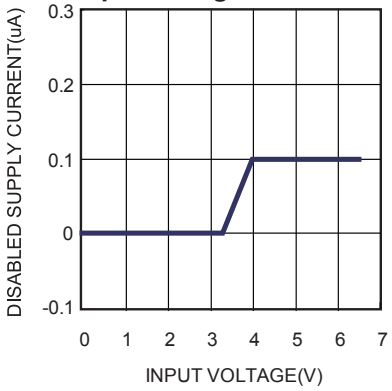
Efficiency vs. Load Current



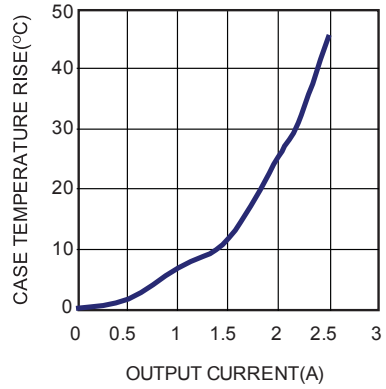
Enabled Supply Current vs. Input Voltage



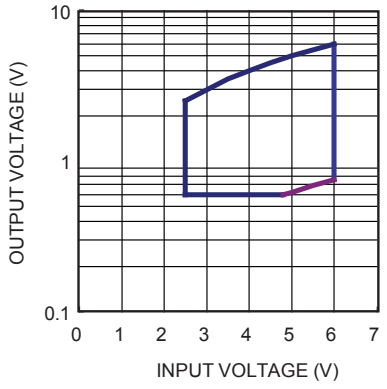
Disabled Supply Current vs. Input Voltage



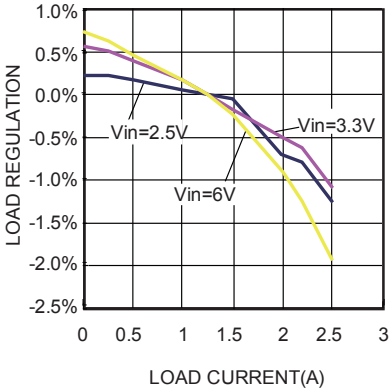
Case Temperature Rise vs. Output Current (Io2=0)



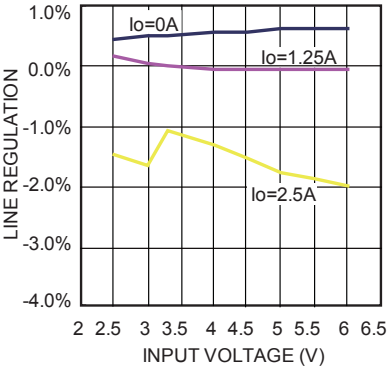
Operating Range



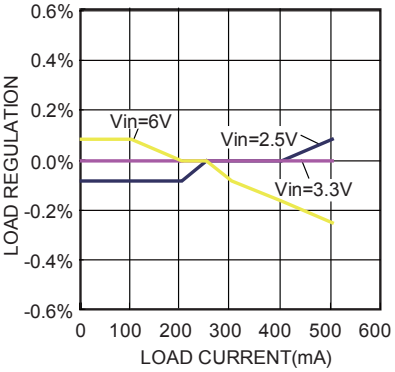
Load Regulation



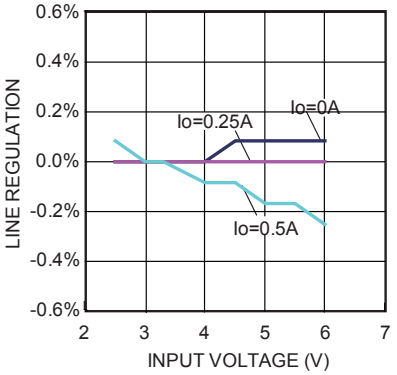
Line Regulation



Load Regulation (LDO)



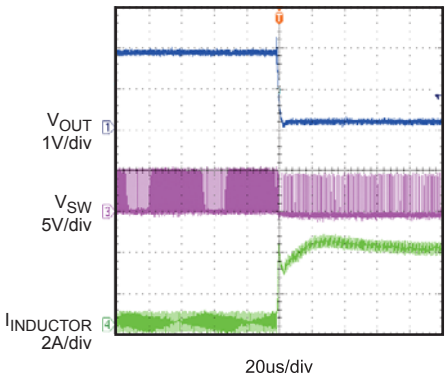
Line Regulation (LDO)



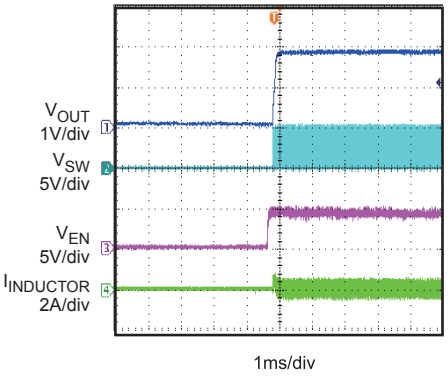
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V,V_{OUT2} = 1.2V, L=1uH, T_A = +25ºC, unless otherwise noted

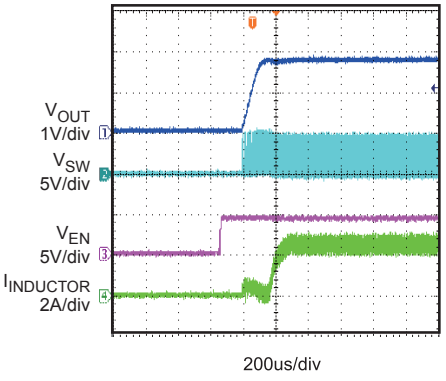
Output Short
I_{O1}=0A



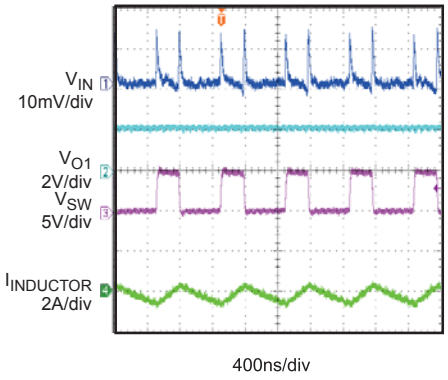
Enable Startup
I_{O1}=0A



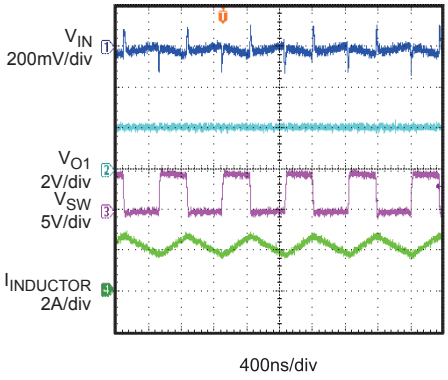
Enable Startup
I_{O1}=2.5A



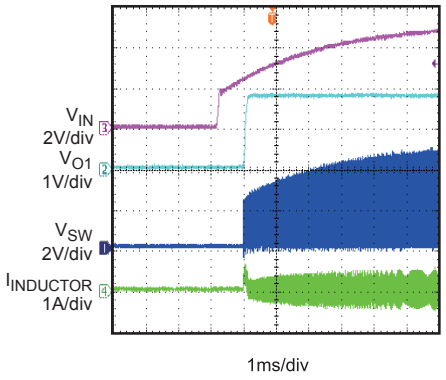
Input Ripple Voltage
I_{O1}=0A



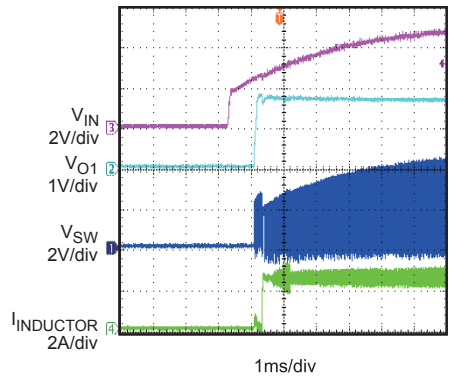
Input Ripple Voltage
I_{O1}=2.5A



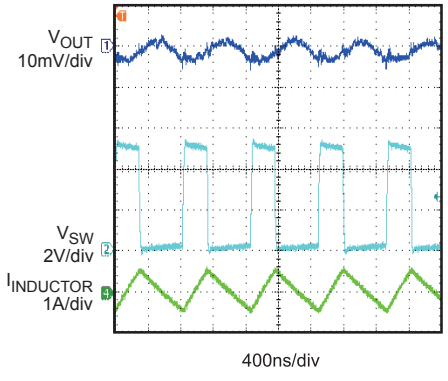
Power Up
I_{O1}=0A



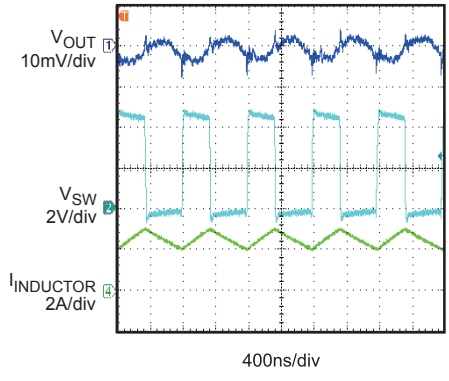
Power Up
I_{O1}=2.5A



Output Ripple Voltage
I_{O1}=0A



Output Ripple Voltage
I_{O1}=2.5A

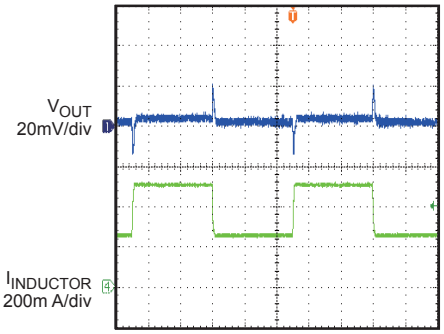


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V,V_{OUT2} = 1.2V, L=1uH, T_A = +25ºC, unless otherwise noted

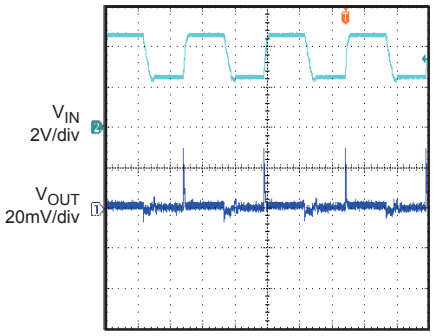
Load Transient Response

I_{O2}=0.25~0.5A, Slew Rate: 1A/us



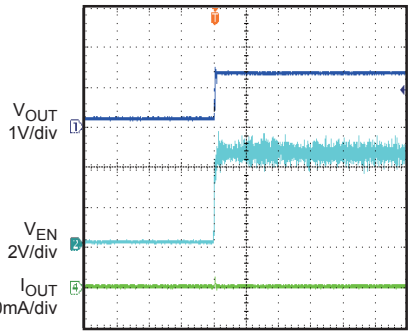
Line Transient Response

V_{IN2}=2.5~5V, I_{O2}=0.5A



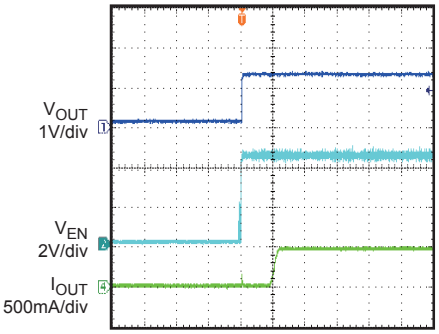
EN On

I_{O2}=0A



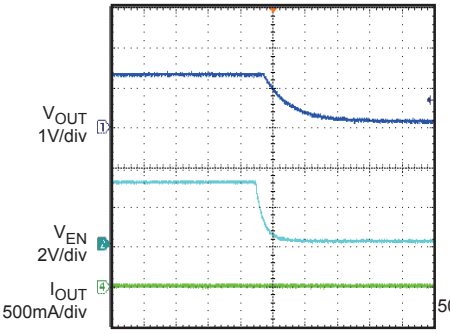
EN On

I_{O2}=0.5A



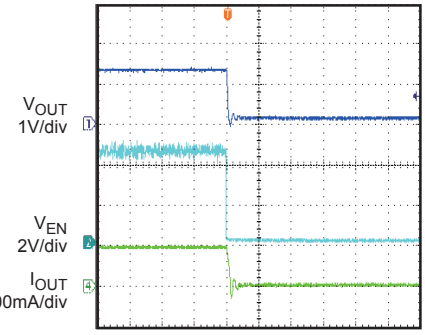
EN Off

I_{O2}=0A



EN Off

I_{O2}=0.5A



OPERATION

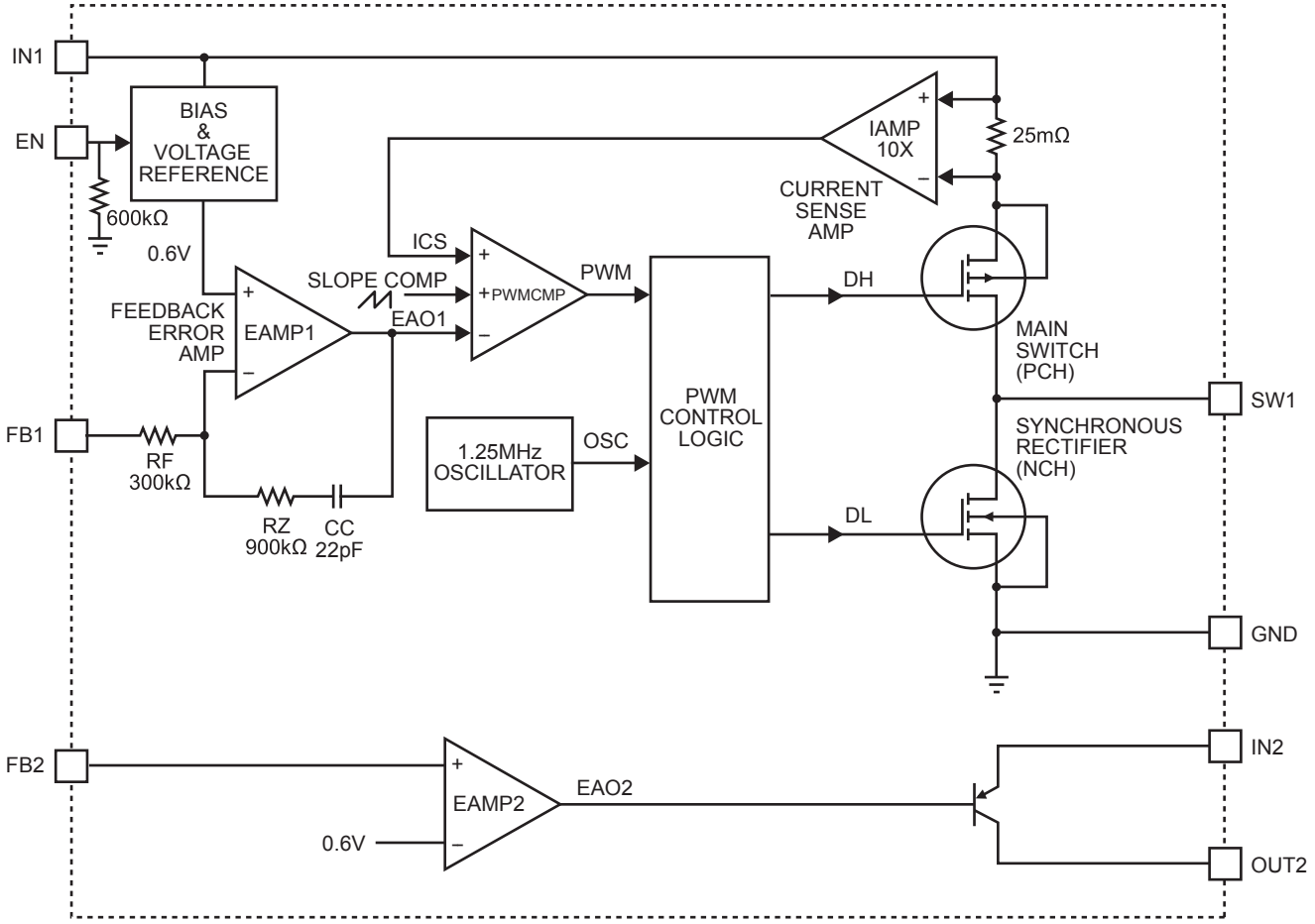


Figure 1—Functional Block Diagram

The MP2126 is a 1.25MHz fixed frequency current mode synchronous step-down switcher with a 0.5A low dropout (LDO) linear regulator.

The MP2126 uses an external resistor divider to set both the switcher and LDO output voltage from 0.6V to 6V.

2.5A Synchronous Step-Down Switcher

The switcher integrates both a main switch and a synchronous rectifier, which provides high efficiency and eliminates an external Schottky diode.

The duty cycle D of a step-down switcher is defined as:

$$D = T_{ON} \times f_{OSC} \times 100\% \approx \frac{V_{OUT}}{V_{IN}} \times 100\%$$

Where T_{ON} is the main switch on time and f_{OSC} is the oscillator frequency (1.25MHz).

Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limiting for superior load and line response in addition to protection of the internal main switch and synchronous rectifier. The MP2126 switches at a constant frequency (1.25MHz) and regulates the output voltage. During each cycle the PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. During normal operation, the main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. When the main switch is off, the synchronous rectifier will be turned on immediately and stay on until the next cycle starts.

Dropout Operation

The MP2126 allows the main switch to remain on for more than one switching cycle and increases the duty cycle while the input voltage is dropping close to the output voltage. When the duty cycle reaches 100%, the main switch is held on continuously to deliver current to the output up to the PFET current limit. The output voltage then becomes the input voltage minus the voltage drop across the main switch and the inductor.

Short Circuit Protection

When the output is shorted to ground, the oscillator frequency is reduced to prevent the inductor current from increasing beyond the PFET current limit. The PFET current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage reaches 0.6V.

Enable Control

MP2126 has a dedicated Enable control pin. By pulling it to high or low, the IC can be enabled and disabled by EN. Tie EN to VIN by proper voltage divider for automatic start up as Figure 2 shows. And make sure that:

$$\text{Max. EN Threshold} < V_{IN} \times \frac{R_{EN2}}{(R_{EN1} + R_{EN2})} < 6V$$

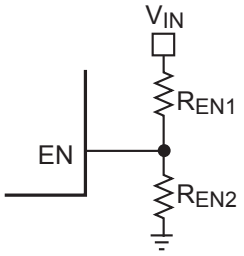


Figure 2

Maximum Load Current

The MP2126 can operate down to 2.5V input voltage; however the maximum load current decreases at lower input due to a large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely, the current limit increases as the duty cycle decreases.

0.5A Linear Regulator

The 500mA low dropout (LDO) linear regulator has separate input IN2 and output OUT2 pins for the internal power device. The control circuitry of the LDO takes power from the main input supply IN1. Both IN1 and IN2 input supplies must be presented for the LDO working properly. The LDO power device input IN2 can be connected to the switcher output (Figure1) or directly to the main supply IN1 (Figure2). If the IN2 tied to the IN1, it is optional to insert a RC filter between IN1 and IN2. The RC filter will reduce switching noise coupling from IN1 to IN2 and power dissipation inside the MP2126.

APPLICATION INFORMATION

Output Voltage Setting

The external resistor dividers set the output voltage of the switcher and LDO. Choose feedback resistors R2 and R4 value between 1kΩ and 100kΩ for good transient response.

R1 and R3 are then given by:

$$R1 = R2 \times (\frac{V_{OUT1}}{0.6V} - 1)$$

$$R3 = R4 \times (\frac{V_{OUT2}}{0.6V} - 1)$$

Table 1—Resistor Selection vs. Output Voltage Setting

V_{OUT}	R1	R2	R3	R4
1.2V	60.4kΩ	60.4kΩ	60.4kΩ	60.4kΩ
1.5V	90.9kΩ	60.4kΩ	90.9kΩ	60.4kΩ
1.8V	121kΩ	60.4kΩ	121kΩ	60.4kΩ
2.5V	191kΩ	60.4kΩ)	191kΩ	60.4kΩ
3.3V	274KΩ	60.4kΩ	274KΩ	60.4kΩ

It is optional to speed the switcher loop response by adding a small feedforward capacitor C_F parallel with R1. Choose R1xC_F time constant around 3usec.

Inductor Selection

A 1μH to 10μH inductor with DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance should be <100mΩ. See Table 2 for recommended inductors and manufacturers. For most designs, the inductance value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is inductor ripple current. Choose inductor ripple current approximately 30% of the maximum load current, 2.5A.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2}$$

Table 2—Suggested Surface Mount Inductors

Manufacturer	Part Number	Inductance (μH)	Max DCR (mΩ)	Saturation Current (A)
Toko	D62CB-#A920CY-1R0M	1.0	11	3.48
Wurth	744314110	1.1	13	3.2

Switcher Input Capacitor C_{IN1} Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency should be less than input source impedance to prevent high frequency switching current passing to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF~22μF capacitor is sufficient.

Switcher Output Capacitor C_{O1} Selection

The output capacitor keeps output voltage ripple small and ensures regulation loop stable. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended. For most applications, a 22μF~47μF capacitor is sufficient.

The output ripple ΔV_{OUT} is approximately:

$$\Delta V_{OUT1} \le \frac{V_{OUT1} \times (V_{IN1} - V_{OUT1})}{V_{IN1} \times f_{OSC} \times L} \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{O1}} \right)$$

Thermal Dissipation

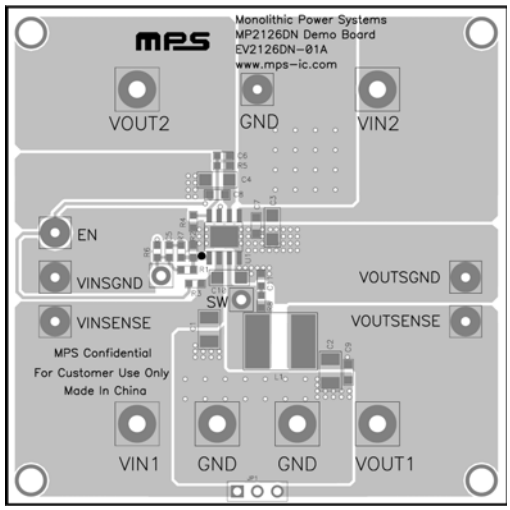
Power dissipation should be considered when both channels of the MP2126 provide maximum 2.5A switcher output current and 0.5A LDO output current to the loads at high ambient temperature. If the junction temperature rises above 150°C, the MP2126 two channels will be shut down.

The junction-to-ambient thermal resistance of the 8-pin SOIC $R_{\Theta JA}$ is 50°C/W. The maximum power dissipation is about 1.6W when the MP2126 is operating in a 70°C ambient temperature environment.

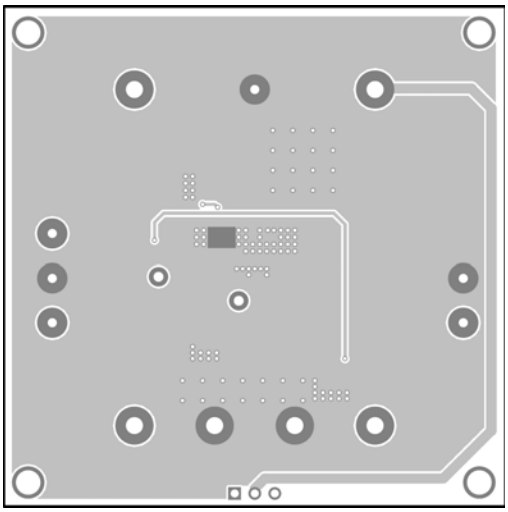
$$PD_{MAX} = \frac{150^{o}C - 70^{o}C}{50^{o}C/W} = 1.6W$$

PCB Layout

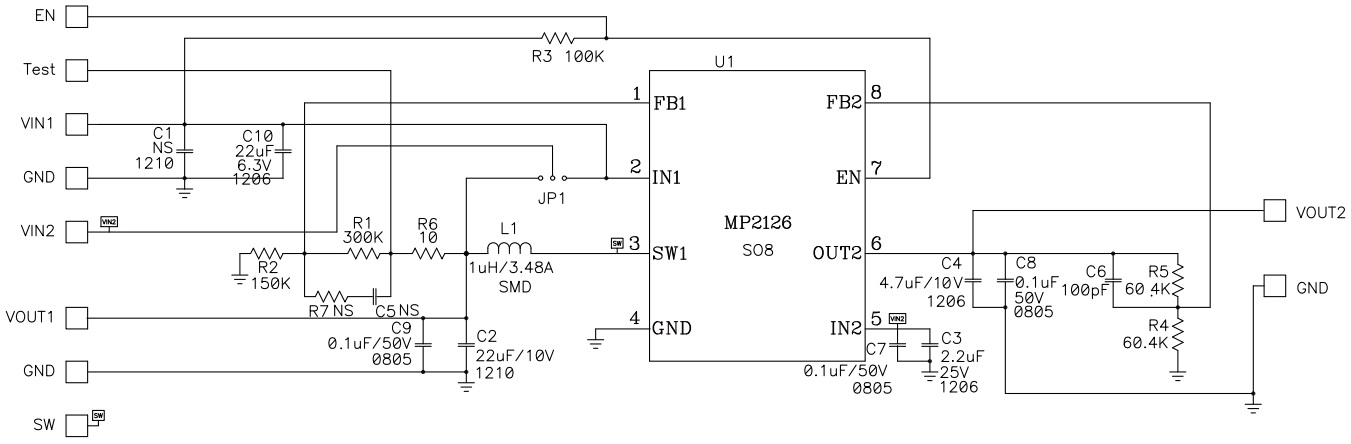
The high current paths (GND, IN1/IN2 and SW) should be placed very close to the device with short, direct and wide traces. Input capacitors should be placed as close as possible to the respective VIN and GND pins. The external feedback resistors should be placed next to the FB pins. Keep the switching nodes SW short and away from the feedback network. An external diode (i.e. B130) can be added between SW and GND to reduce switching noise and to improve the load regulation. The reference layout and its schematic are shown below:



Top Layer



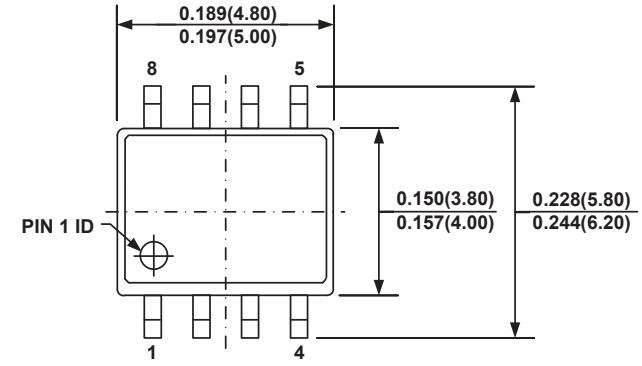
Bottom Layer



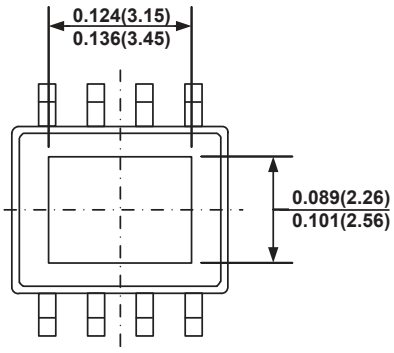
Figure—3

PACKAGE INFORMATION

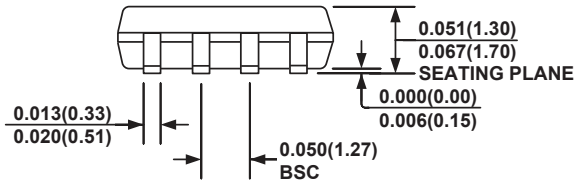
SOIC8E



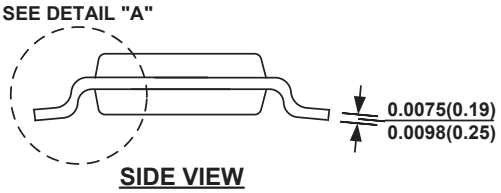
TOP VIEW



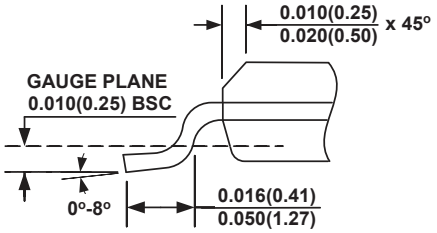
BOTTOM VIEW



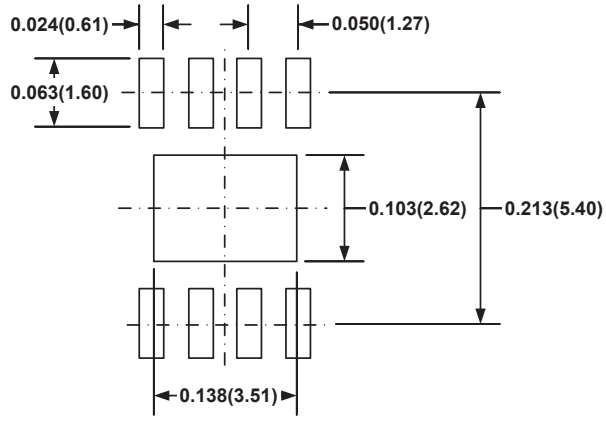
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.