MP4651
Off-line WLED Driver
Application Notes

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CONTENT

1. INTRODUCTION

The MP4651 is a high performance off-line LED driver designed for powering the LEDs especially for high power isolated application.

The MP4651 utilizes fixed operating frequency PWM control. It outputs two 180 degree phase shifted driving signals for various external power stages. Its enhanced 9V gate driver provides adequate driving capability for the external MOSFETs and directly drives the external gate driving transformer.

The MP4651 implements fast and high contrast ratio PWM dimming to the LEDs. PWM dimming is controlled with either an external DC voltage or PWM signal. The burst dimming frequency can be synchronized to an external synchronizing signal.

The Built-in fault management features include open LED protection, short LED protection, over voltage protection, and over temperature protection. The protection interface is flexible for various setups and is easy to use. MP4651 integrates a delay timer to recover the system.

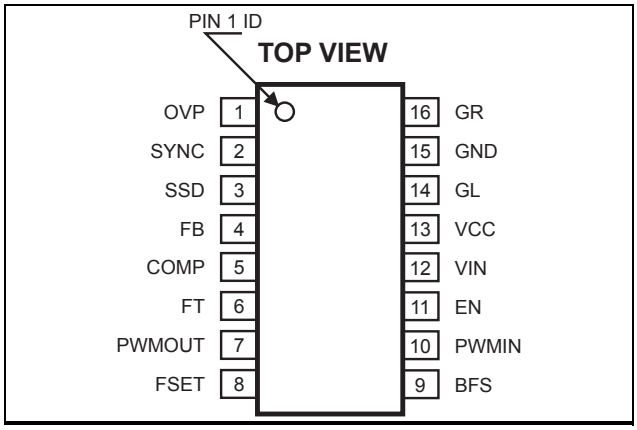
The MP4651 is available in a 16-pin SOIC package.

Features

- 9V Enhanced Gate Driver
- Programmable Fixed Operating Frequency
- Input Voltage Range from 9V to 30V
- DC or PWM Input Dimming Control
- Burst Dimming Frequency Synchronization
- Smart Fault Protection Interface
- Built-in Fault Management
- Built-in Delay Timer for System Recovery
- Available in SOIC 16 Package

Applications

- LCD TV and LCD Monitor
- Flat Panel Video Displays
- LED Lighting Applications



2. DESIGN INFORMATION

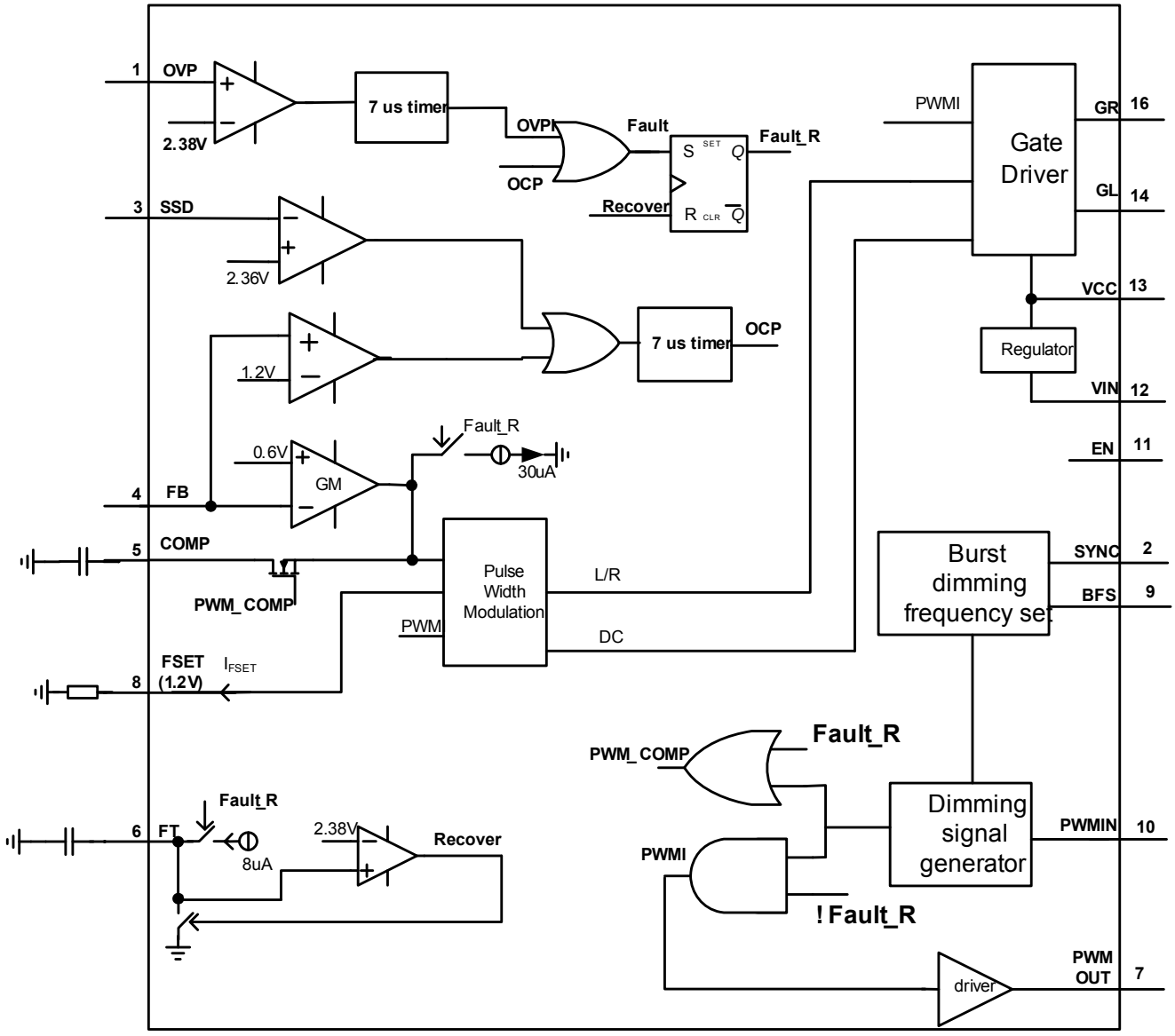


Figure 1—MP4651 Block Diagram

Steady State and Gate Driver

The MP4651 is a fixed operating frequency off-line LED driver specifically designed for the high power isolated application. Powered by 9V to 30V input supplies, the MP4651 outputs two 180 degree phase shifted driving signals for the external power stages. Its enhanced 9V gate driver provides adequate driving capability to the external MOSFETs. MP4651 is able to directly drive the external gate driving transformer. Figure 2 shows a brief driving scheme.

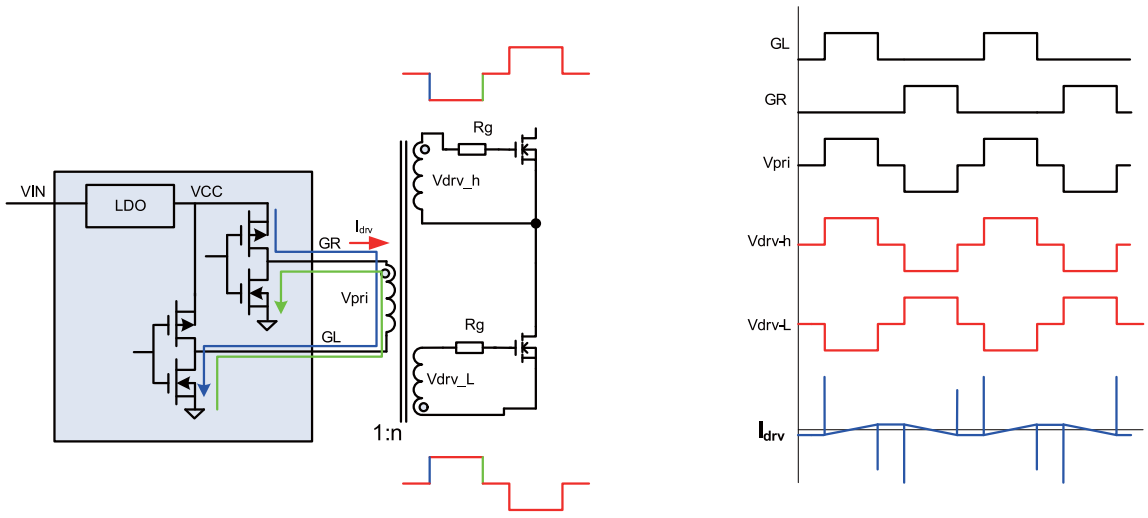


Figure 2—MP4651 Gate Driver Sequence

The operating frequency can be set by the resistor connected from FSET pin to GND. Please refer to pin 8 FSET descriptions on page 14.

The MP4651 utilizes PWM (pulse width modulation) control to the LED driver. The LED current is sensed to FB pin and compared with internal reference. The internal error amplifier generates the error signal to the compensation network on COMP pin to control the PWM duty cycle.

The system power is controlled by EN pin. A high level voltage on EN pin enables the chip and when the chip is enabled, the built-in regulator for VCC is powered up and the internal circuit starts.

Brightness Control

MP4651 implements burst dimming (digital brightness) control to the LED current. The MP4651 has a built-in burst oscillator which can generate a triangle waveform on the BFS pin. Burst dimming can be achieved by either a DC voltage input or external PWM dimming signal.

When burst dimming with a DC input voltage, add a capacitor in parallel with a resistor on BFS pin to set the burst frequency and apply the DC voltage on the PWMIN pin to program the burst duty cycle.

The burst frequency can be synchronized to an external frequency. Applying a synchronizing frequency signal with narrow pulse on SYNC pin can synchronize the burst frequency. The synchronizing frequency should be higher than the burst frequency set by the BFS pin. Please refer to SYNC pin description for details.

When burst dimming with external PWM signal, pull up BFS pin to VCC through a 20kΩ resistor and apply the PWM signal on PWMIN pin.

Fast and High Contrast Ratio PWM Dimming

The MP4651 implements fast and high contrast ratio PWM dimming to the WLED. The PWM dimming signal (controlled by a DC input voltage or direct PWM signal) is output on PWMOUT pin to drive the external dimming MOSFET in series with the LED bar, therefore the LED current rises up immediately when PWM dimming signal is effective.

The PWM dimming signal is also used to disconnect the compensation network (on comp pin, a capacitor or a R-C network) from the error amplifier at PWM off interval, and so that the compensation network voltage is hold at this interval and gets nearly immediately to the steady state value when PWM signal is effective. It eliminates the control loop response time and realizes fast dimming.

The MP4651 strictly controls the sequence of the driving signals. Both the sequence of GL and GR signals and the delay time between PWM dimming signal and driving signals are accurately fixed. Therefore, for each time of PWM dimming, the driving signals are exactly the same and so does the output power delivered to the load. It eliminates the possibility of flicker at small PWM dimming pulse and thus realizes the high contrast ratio PWM dimming.

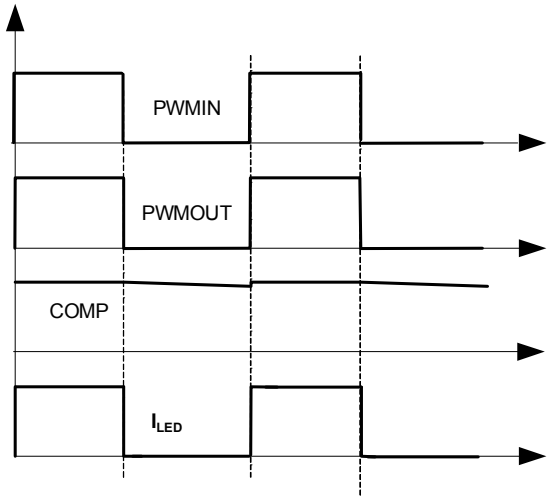


Figure 3—Fast and High Contrast Ratio PWM Dimming

Fault Protection

MP4651 fault management facilities include the Open LED Protection, Short LED Protection, Over LED Current Protection and a hiccup mode fault delay timer. The **Fault Mode** is triggered when any of these three types of protection is detected

The **Fault Mode** can be triggered by:

1, OVP>2.38V for 7us, or

2, SSD<2.36V for 7us, or

3, FB>1.2V for 7us

The OVP pin monitors the output voltage of the LED driver through a voltage divider. When the LED bar is open, the output voltage goes high and so does OVP pin. When OVP voltage gets higher than 2.38V for 7us, MP4651 recognizes it as Open LED Protection and triggers the Fault Mode. Please refer to OVP pin description for details.

The SSD pin monitors the secondary side current for short LED protection. When any point of the LED bar is shorted to ground, the secondary side current gets larger and the SSD pin voltage goes lower, when SSD pin voltage is lower than 2.36V for 7us, the Short LED protection is detected and the Fault Mode is triggered. Please refer to the SSD pin description for details.

The FB pin senses the LED current for regulation and also functions the Over LED Current Protection. When FB voltage gets higher than 1.2V for 7us, the Fault Mode is triggered. Figure 4 shows the fault protection of MP4651.

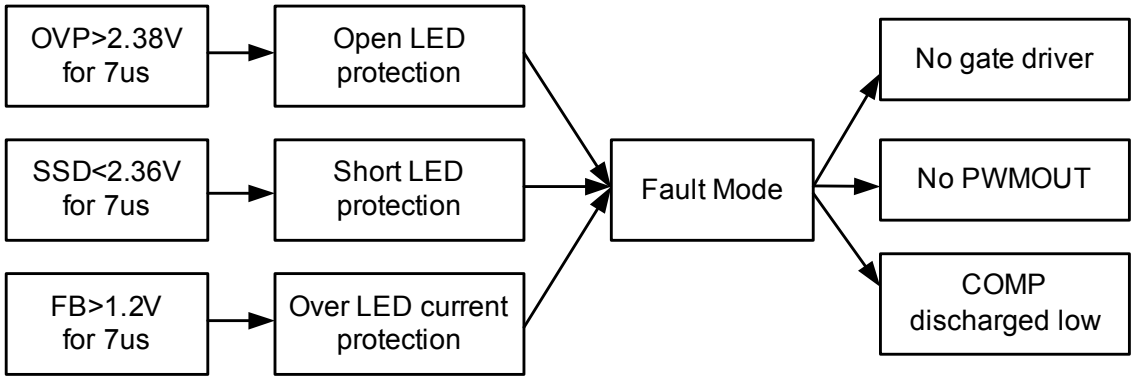


Figure 4—MP4651 Protection and Fault Mode

At **Fault Mode,** the output of gate driving signals GL and GR are disabled, the PWMOUT signal which is used for driving the dimming MOS is pulled low and the COMP voltage is discharged low to its clamp voltage. No power is delivered to the output at this condition. The fault signals on OVP, SSD or FB will disappear gradually at the Fault Mode as no power is delivered to the output.

When the fault signals on OVP, SSD and FB pin disappear, the internal hiccup mode fault delay timer is started. The FT capacitor is charged by an 8uA internal current source and when FT pin voltage hits the 2.38V threshold, system recovers. It enables the gate driving signals and the PWMOUT signal, and COMP voltage is recharged up by the compensation loop. The FT pin is pulled low when system recovers. The time interval when FT pin charged from 0V to 2.38V is the fault delay time, calculated by the following equation:

$$T_{FT} = \frac{2.38V \times C_{FT}}{8uA}$$

A 10nF capacitor on FT sets the delay time around 3ms.

Figure 5 shows the protection sequence. Fault Mode is triggered when a fault signal occurs at OVP, SSD or FB pin. System stays at the fault mode till the fault signals disappear and recovers after a fault delay time set by the FT cap.

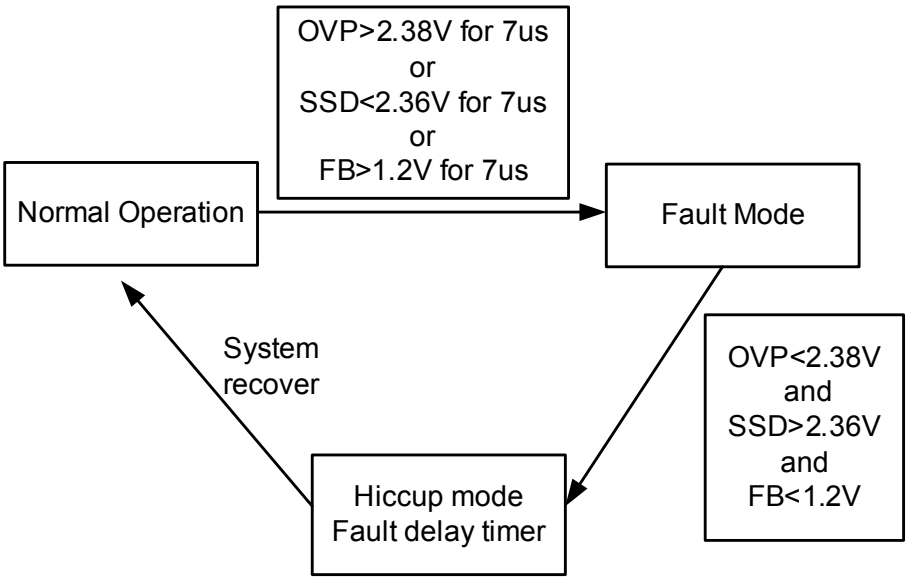


Figure 5—MP4651 Protection Sequence

The MP4651 implements protection for the open LED, short LED or over LED current condition. System auto recovers after a hiccup mode fault delay time.

3. APPLICATION INFORMATION AND PIN FUNCTIONS

Pin 1 (OVP):

Over Voltage Protection: This pin is used for over voltage protection at open LED condition. The output voltage is monitored by this pin and when the voltage on this pin exceeds 2.38V for 7us, the Fault Mode is triggered.

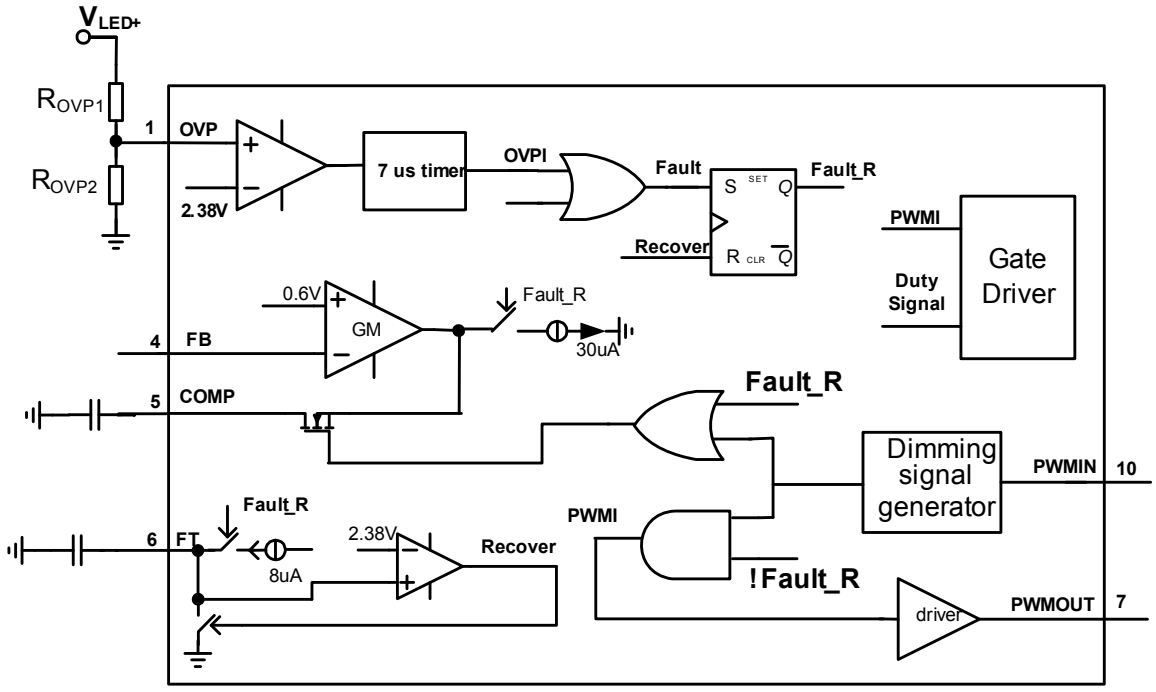


Figure 6—OVP Protection Scheme

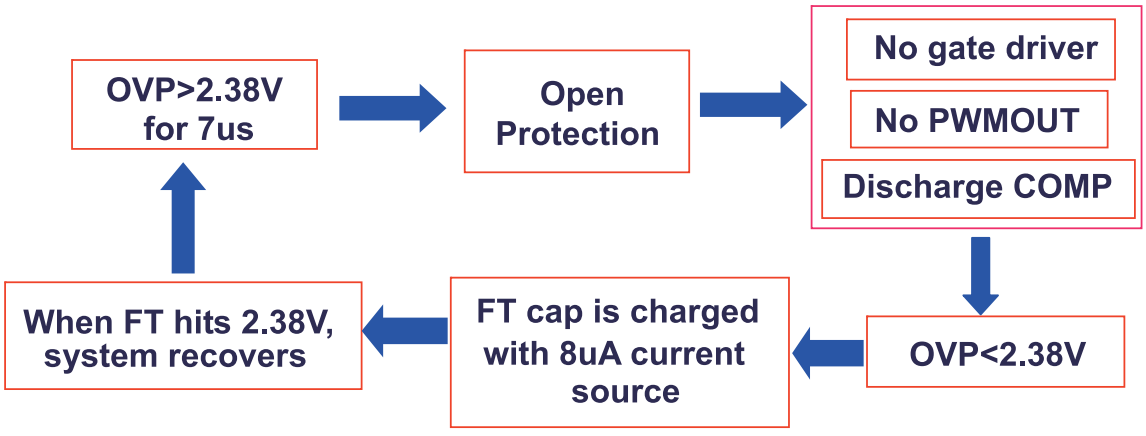


Figure 7—Open Protection Process

Figure 6 shows the OVP protection scheme. The output voltage of the LED driver is sensed to OVP pin through the voltage divider. An internal comparator is integrated on OVP pin. When open LED occurs, the output voltage goes higher and so does the OVP pin voltage. When the OVP pin voltage get higher than the 2.38V threshold, the comparator outputs a high level signal. If this high level signal exists longer than the 7us timer, the OVPI fault signal sets the RS flip-flop and triggers the Fault Mode.

Set the resistor R_{OVP1} and R_{OVP2} for the over voltage protection point of the output voltage, which is typically 20% higher than the normal operation voltage of the LED bar.

$$V_{OVP} = 2.38V * \frac{R_{OVP1} + R_{OVP2}}{R_{OVP2}}$$

The R_{OVP1} is usually in 500kΩ to 1MΩ range to reduce the power consumption.

At Fault Mode, the gate driving signals and PWMOUT signal are disabled, the COMP is discharged and no power is delivered to the output. The output voltage decreases and OVP voltage gradually gets lower than 2.38V, and then the hiccup mode fault delay timer starts. After the fault delay time, system auto recovers. If the open LED condition still exists, system repeats the OVP protection process as shown in figure 7. If open LED condition disappears, system inters normal operation.

Pin 3 (SSD):

Short String Detection: This pin is used for short string protection. An internal comparator is integrated on this pin and when the voltage on this pin gets lower than 2.36V for 7us, the IC treats it as short string condition and triggers the Fault Mode.

Figure 8 shows the SSD protection scheme. The secondary side current is used for the short protection. When short LED condition occurs, the secondary side current gets larger, the OCP pin gets an even lower negative voltage which is biased to SSD pin. When SSD pin voltage get lower than 2.36V, the internal comparator outputs a high level signal, if this high level signal exists longer than the 7us timer, the fault signal gets high and sets the RS flip-flop. It holds the fault status until the recover signal comes which is triggered by the hiccup mode fault delay timer FT, IC enters Fault Mode at this interval.

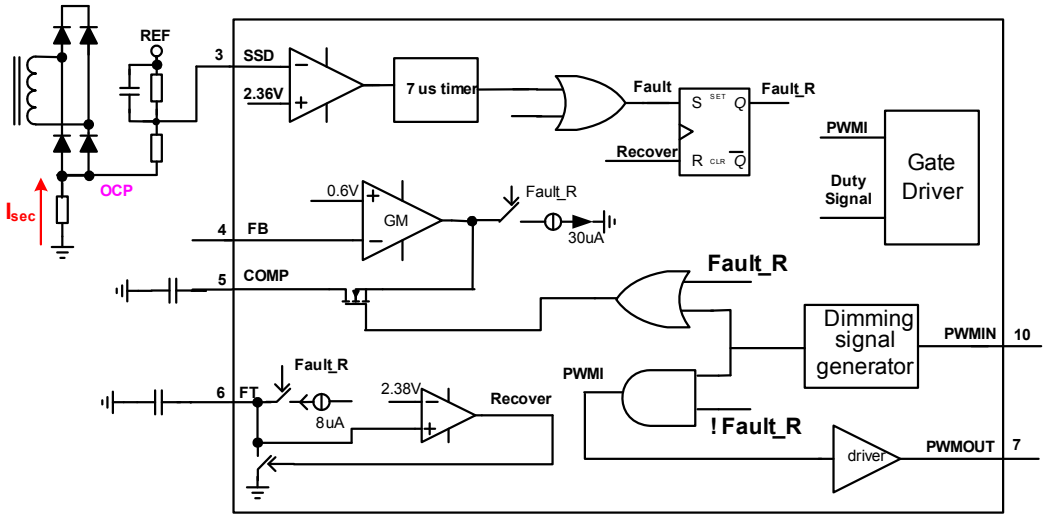


Figure 8—SSD Detection and Protection Scheme

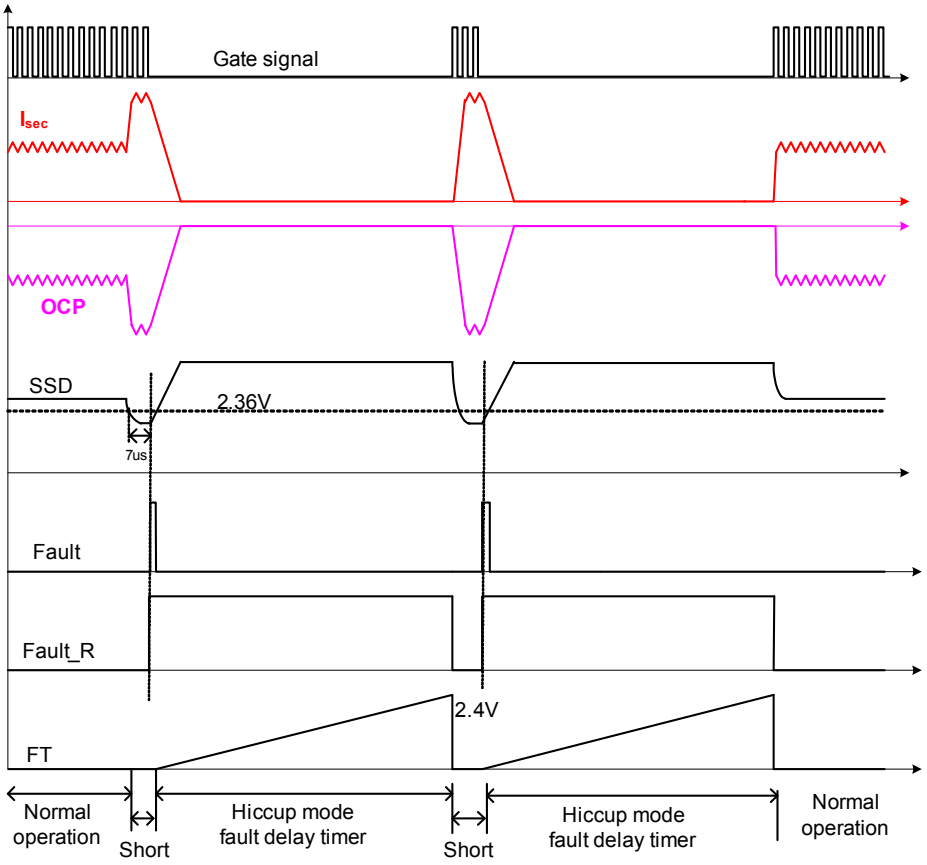


Figure 9—SSD Protection Sequence

At Fault Mode, the gate driving signals and the PWMOUT signal are disabled, and the COMP is discharged low to its clamp voltage.

Figure 9 shows the protection sequence. When short condition occurs, the short current gets larger, OCP gets lower and SSD gets lower than 2.36V. The fault signal goes high when SSD is lower than 2.36V for 7us, and the RS flip-flop output Fault_R is set high. The gate signal is disabled and the secondary current goes low. The SSD returns to a high level. When SSD gets higher than 2.36V again, the Fault signal gets low, but the RS flip-flop output Fault_R keeps high status. The hiccup mode delay timer starts and FT is charged up when the fault signal gets low. When FT hits the 2.38V threshold, the RS flip-flop is reset and its output Fault_R gets low. System recovers and gate driving signal is enabled. If the short condition still exists, IC repeats the fault protection sequence. System recovers to normal operation when the fault condition disappears.

MP4651 integrates the hiccup mode fault delay timer and enjoys an auto recovery for the short protection.

Pin 4 (FB):

LED Current Feedback: This pin is used for LED current regulation. The LED current is sensed to this pin and the voltage on this pin is regulated with 0.6V average value at PWM on interval. At the

PWM off interval, the signal on this pin has no influence to the regulation. Set the LED current with a proper LED current sensing resistor R_{FB}:

$$R_{FB} = \frac{0.6V}{I_{LED}}$$

FB pin also functions as over LED current protection. When the voltage on FB gets higher than 1.2V for 7us, the IC triggers the Fault Mode.

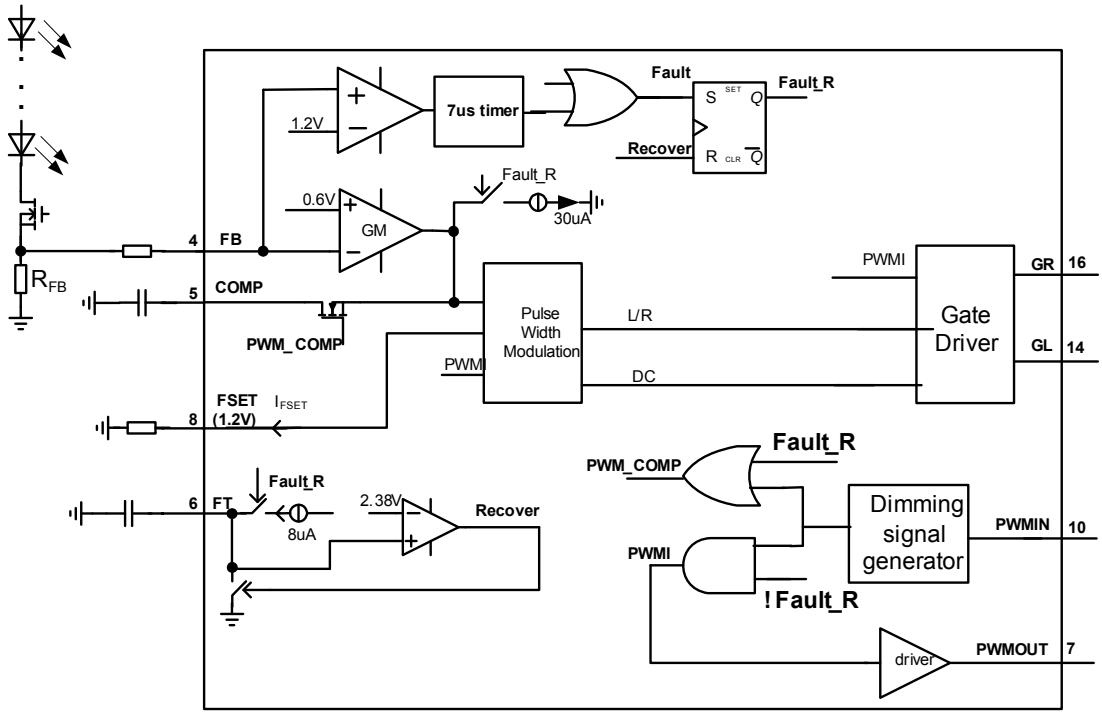
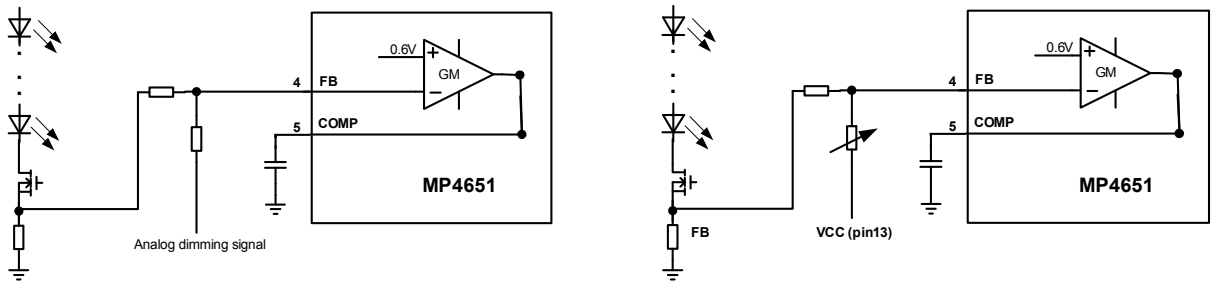


Figure 10—FB pin Regulation and Protection Scheme

Figure 10 shows the regulation and protection scheme of FB pin. An error amplifier and a comparator are integrated on this pin. The error amplifier regulates the LED current to 0.6V reference voltage at PWM on interval. At PWM off interval, the output of the error amplifier is pulled low. The compensation network on COMP pin is connected to the output of the error amplifier through an inner switch. At PWM on interval, the switch is on and the compensation network functions; at PWM off interval, the switch is turned off, the compensation network is disconnected from the error amplifier and holds its value, the signal on FB pin has no influence to the compensation network and therefore has no influence to the current regulation.

The comparator on FB pin functions the over LED current protection. It compares the FB voltage with the internal 1.2V threshold voltage. When the FB voltage gets higher than 1.2V, it outputs a high level signal. If this signal exists longer than the 7us timer, the fault signal gets high and sets the RS flip-flop, which triggers the Fault Mode. The process is similar to the short LED protection as described in SSD pin. System can auto recover from the over current LED protection after the hiccup mode fault delay time.

The LED current can be adjusted by an external analog dimming DC voltage or a variable resistor as shown in figure 11.



Adjust LED current with external A-dim signal **Adjust LED current with variable resistor**

Figure 11—Adjust LED Current

Pin 5 (COMP):

This pin is used for compensation. Connect a 1~47nF capacitor from COMP to GND. This cap should be X7R ceramic. The value of this cap influences the bandwidth of the control loop and determines the stability of the LED current regulation. At PWM on interval, the COMP pin is connected to the output of the error amplifier, and the LED current is regulated by the compensation loop. At PWM off condition, the COMP pin capacitor is internally disconnected from the amplifier and holds its voltage at PWM off interval. This COMP feature improves the response speed of LED current at PWM dimming condition and allows a wide PWM dimming range.

At fault condition, the COMP voltage is discharged to its clamp voltage by an internal 30uA current source.

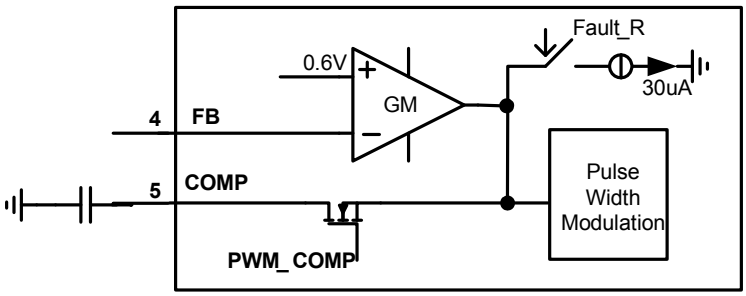


Figure 12—COMP Pin Diagram

Pin 6 (FT):

Hiccup Mode Fault Delay Timer: Connect a capacitor from this pin to GND to set the hiccup mode fault delay timer. It sets the delay time to recover the system when a fault condition is detected. When the fault signals on the detection pins disappeared, an internal 8uA current source charges FT pin capacitor and when FT hits the 2.38V threshold, IC recovers. This interval is the fault delay time.

$$T_{FT} = \frac{2.38V \times C_{FT}}{8uA}$$

A 10nF capacitor on FT sets the fault delay time around 3ms.

If requiring system latch off when fault condition is detected, connect a resistor with its value lower than 200kΩ on FT pin. The FT pin can not hit the 2.38V threshold with this set and system will not recover. For this set, need to toggle the EN pin to restart the system.

Pin 8 (FSET):

Frequency Set: Connect a resistor from this pin to GND to set the operating frequency (f_o). The FSET pin is internally regulated with typical 1.2V, and its output current determines the operating frequency. The value for this resistor R_{FSET} is calculated by

$$R_{FSET} = \frac{1.25 \times 10^9}{f_o}$$

For R_{FSET} = 25kΩ, operating frequency will be 50 kHz.

Adjusting the output current of FSET pin will program the operating frequency. This function makes MP4651 suitable for the frequency controlled system.

Pin 7 (PWMOUT):

Output of PWM Dimming Signal: This pin outputs the burst dimming signal to the LED for fast PWM dimming. Connect this pin directly to the gate of the dimming MOSFET in series of the LED bar.

At Fault Mode, the PWMOUT is internally pulled low.

Pin 9 (BFS):

Burst Frequency Set: BFS pin is used to set the burst frequency. For DC input burst dimming, connect a resistor (R_{BFS}) in parallel with a capacitor (C_{BFS}) on this pin to set the burst frequency.

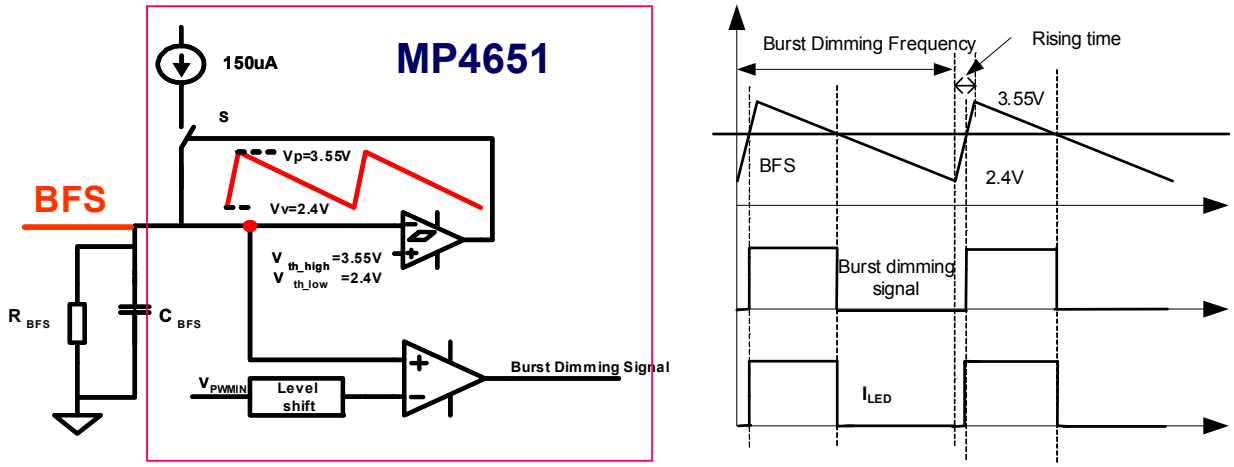


Figure 13—MP4651 Burst Mode with DC Input Voltage

As shown in figure 13, the voltage on BFS pin is compared in a hysteretic comparator, whose peak threshold is 3.55V, and valley threshold is 2.4V. When the BFS pin voltage is lower than the valley threshold 2.4V, an internal current source (typical 150uA) charges the BFS pin capacitor C_{BFS} and the BFS pin voltage increases until it hits the peak threshold 3.55V, which will turn off the internal current source. Then the voltage on C_{BFS} is discharged through R_{BFS}, until it hits the valley threshold 2.4V

again. Therefore a triangle waveform with peak value Vp=3.55V and valley value Vv=2.4V is obtained on BFS pin.

The triangle waveform on BFS pin is compared with a DC input voltage from PWMIN pin (pin 10) after a level shift circuit, which shifts the voltage of PWMIN pin V_{PWMIN} to 3.6V-V_{PWMIN}. The output signal of the comparator is for the burst dimming.

C_{BFS} and R_{BFS} determine the triangle waveform on BFS pin, as shown in figure 13. The values are determined as follows:

Set a percentage of the rising time, where:

$$D_{rise} = t_{rise} \times f_{Burst}$$

R_{BFS} and C_{BFS} are determined by:

$$R_{BFS} \approx 21.16k\left(\frac{1}{D_{rise}} - 1\right) + 21.43k$$

$$C_{BFS} = \frac{1 - D_{rise}}{f_{Burst} \times R_{BFS} \times 0.405}$$

For D_{rise}= 0.1, f_{Burst} = 200Hz, then R_{BFS} = 212k, C_{BFS} = 52nF

For direct PWM burst dimming, pull BFS high to VCC through a 20kΩ resistor and apply the PWM signal to PWMIN pin.

Pin 10 (PWMIN):

This pin is used for burst dimming duty ratio control. For DC input burst dimming, the DC voltage on this pin controls the burst dimming duty ratio. This signal needs to be filtered for optimal operation. A voltage ranging from 0 to 1.2V on PWMIN programs the burst dimming duty cycle from 0 to 100%. Adding a bias voltage (from VCC) on this pin can set the minimum PWM dimming duty ratio.

For direct Pulse Width Modulation (PWM) burst dimming, Pull BFS high to VCC through a 20kΩ resistor and connect PWMIN to a logic level PWM signal. Logic High is Burst On and a logic Low is Burst Off.

Pin 2 (SYNC):

Burst frequency synchronization. This pin is used to synchronize the burst dimming frequency. Applying a synchronizing frequency signal with small pulse will synchronize the burst frequency.

Figure 4 shows the synchronized DC input burst dimming. The synchronizing signal is filtered by a high pass filter. Its rising edge is caught and used for synchronizing the triangle waveform on BFS pin. The synchronizing frequency should be higher than that set by BFS pin and the amplitude of the synchronizing signal should be higher than 1.4V.

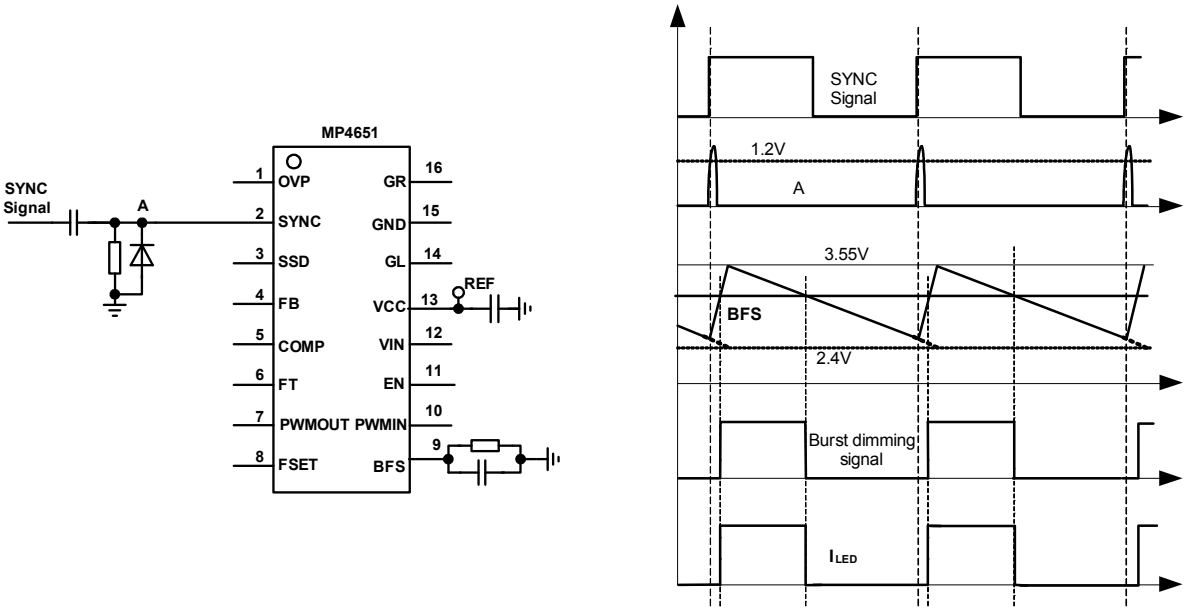


Figure 14—Synchronized DC Input Burst Dimming

Table 1—Function Mode

Function	Pin Connection		
	PWMIN	BFS	SYNC
Burst Mode with DC Input Voltage	0V to 1.2V	C_{BFS}, R_{BFS}	GND or open
Burst Mode with DC Input Voltage and Synchronizing frequency	0V to 1.2V	C_{BFS}, R_{BFS}	R,C,D network
Burst Mode with External PWM Source	PWM	To VCC through 20kΩ resistor	GND or open

Burst Brightness Polarity: 100% duty cycle at PWMIN voltage 1.2V.

Pin 11 (EN):

Enable of the IC: Pull this pin high to enable the chip, and pull it low to disable the chip. For safe operation, apply a voltage higher than 2V to turn on the chip, and a voltage lower than 1V to turn off the chip.

Pin 12 (VIN):

Supply voltage input. By pass the supply voltage with a 0.1uF or greater ceramic cap. This cap should be placed close to the IC.

Pin 13 (VCC):

This pin provides the gate driver supply voltage, its typical value is 9.7V (at no load condition). Connect a 1uF or greater ceramic capacitor on this pin to bypass the supply voltage. This voltage is also used to supply the external control circuit.

Just as other power supplies, VCC voltage may decrease when the output current gets larger. To ensure a good operating performance, VCC output current is not recommended more than 20mA. Do not pull too much current though VCC pin.

In the off-line application, the external MOSFETs are usually driven through a gate driving transformer. The output driving current includes two types: the magnetic current of the gate driving transformer and the driving current of the MOSFETs when they turn on or turn off. To limit the magnetic current, the magnetic inductance of the gate driving transformer should be larger than **2mH**.

Pin 14(GL), Pin 16 (GR):

Gate driving signals output. GL and GR are 180 degree phase shifted driving signals. With its enhanced driving capability, GL and GR are able to directly drive the externally MOSFET in the off-line system through a gate driving transformer, as shown in figure 2.

Connect two 5.1Ω resistors in series with GL and GR to eliminate the EMI noise injected to the IC.
GL and GR can also drive the external MOSFETs in the push-pull circuit and some other possible applications.

4. START UP SEQUENCE

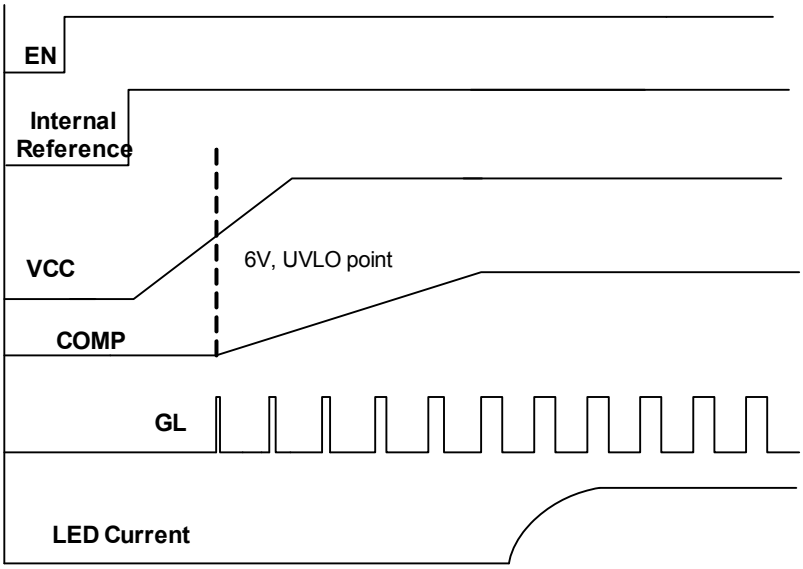


Figure 15— MP4651 Start Up Sequence

Figure 15 shows MP4651 start up sequence at normal operation, about 40μs delay time after EN is powered on, the internal reference voltage is established and the VCC voltage begins to increase, after about 220μs (depending on the capacitor on the VCC pin), the VCC voltage passes its internal UVLO point at about 6V, and then the COMP voltage starts to rise, the duty cycle of the driving signal increases proportionally to the COMP voltage. Before the UVLO point of VCC, the COMP pin is pulled down, and no driving signals are output on GL and GR pin.