Jameco Part Number 48039

MOTOROLA

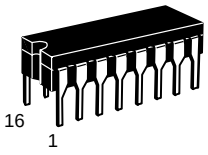
# SN54/74LS76A

# DUAL JK FLIP-FLOP WITH SET AND CLEAR

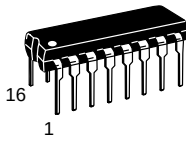
The SN54/74LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW clock transitions.

**DUAL JK FLIP-FLOP WITH SET AND CLEAR**

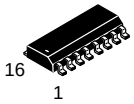
**LOW POWER SCHOTTKY**




**J SUFFIX**
CERAMIC
CASE 620-09




**N SUFFIX**
PLASTIC
CASE 648-08




**D SUFFIX**
SOIC
CASE 751B-03

**ORDERING INFORMATION**

| | |
|---|---|
| SN54LSXXJ | Ceramic |
| SN74LSXXN | Plastic |
| SN74LSXXD | SOIC |

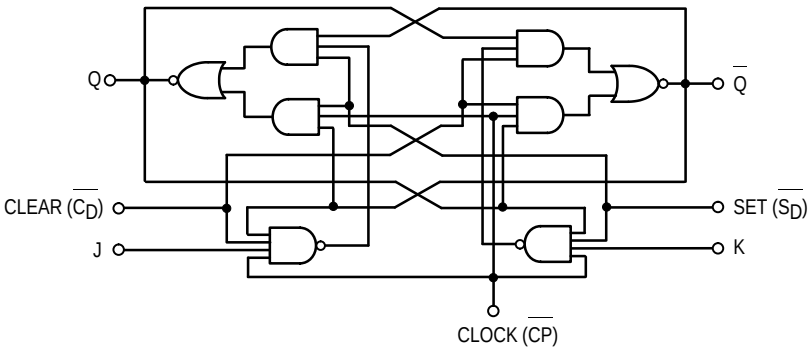
**MODE SELECT — TRUTH TABLE**

| OPERATING MODE | INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| | $\overline{S}_D$ | $\overline{C}_D$ | J | K | Q | $\overline{Q}$ |
| Set | L | H | X | X | H | L |
| Reset (Clear) | H | L | X | X | L | H |
| *Undetermined | L | L | X | X | H | H |
| Toggle | H | H | h | h | q | q |
| Load “0” (Reset) | H | H | l | h | L | H |
| Load “1” (Set) | H | H | h | l | H | L |
| Hold | H | H | l | l | q | q |

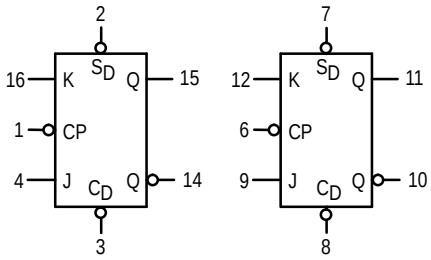
*Both outputs will be HIGH while both $S_D$ and $C_D$ are LOW, but the output states are unpredictable if $S_D$ and $C_D$ go HIGH simultaneously.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Immaterial
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the HIGH-to-LOW clock transition

**LOGIC DIAGRAM**




**LOGIC SYMBOL**




$V_{CC}$ = PIN 5
GND = PIN 13

## GUARANTEED OPERATING RANGES

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V |
| $T_A$ | Operating Ambient Temperature Range | 54<br>74 | −55<br>0 | 25<br>25 | 125<br>70 | °C |
| $I_{OH}$ | Output Current — High | 54, 74 | | | −0.4 | mA |
| $I_{OL}$ | Output Current — Low | 54<br>74 | | | 4.0<br>8.0 | mA |

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | | Limits Min | Limits Typ | Limits Max | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | 54 | | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | | 0.8 | | | |
| $V_{IK}$ | Input Clamp Diode Voltage | | | −0.65 | −1.5 | V | $V_{CC}$ = MIN, $I_{IN}$ = −18 mA | |
| $V_{OH}$ | Output HIGH Voltage | 54 | 2.5 | 3.5 | | V | $V_{CC}$ = MIN, $I_{OH}$ = MAX, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table | |
| | | 74 | 2.7 | 3.5 | | V | | |
| $V_{OL}$ | Output LOW Voltage | 54, 74 | | 0.25 | 0.4 | V | $I_{OL}$ = 4.0 mA | $V_{CC}$ = $V_{CC}$ MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | $I_{OL}$ = 8.0 mA | |
| $I_{IH}$ | Input HIGH Current | J, K<br>Clear<br>Clock | | | 20<br>60<br>80 | µA | $V_{CC}$ = MAX, $V_{IN}$ = 2.7 V | |
| | | J, K<br>Clear<br>Clock | | | 0.1<br>0.3<br>0.4 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 7.0 V | |
| $I_{IL}$ | Input LOW Current | J, K<br>Clear, Clock | | | −0.4<br>−0.8 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V | |
| $I_{OS}$ | Short Circuit Current (Note 1) | | −20 | | −100 | mA | $V_{CC}$ = MAX | |
| $I_{CC}$ | Power Supply Current | | | | 6.0 | mA | $V_{CC}$ = MAX | |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ($T_A$ = 25°C, $V_{CC}$ = 5.0 V)

| Symbol | Parameter | Limits Min | Limits Typ | Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | 30 | 45 | | MHz | $V_{CC}$ = 5.0 V<br>$C_L$ = 15 pF |
| $t_{PLH}$<br>$t_{PHL}$ | Clock, Clear, Set to Output | | 15 | 20 | ns | |
| | | | 15 | 20 | ns | |

## AC SETUP REQUIREMENTS ($T_A$ = 25°C)

| Symbol | Parameter | Limits Min | Limits Typ | Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_W$ | Clock Pulse Width High | 20 | | | ns | $V_{CC}$ = 5.0 V |
| $t_W$ | Clear Set Pulse Width | 25 | | | ns | |
| $t_s$ | Setup Time | 20 | | | ns | |
| $t_h$ | Hold Time | 0 | | | ns | |