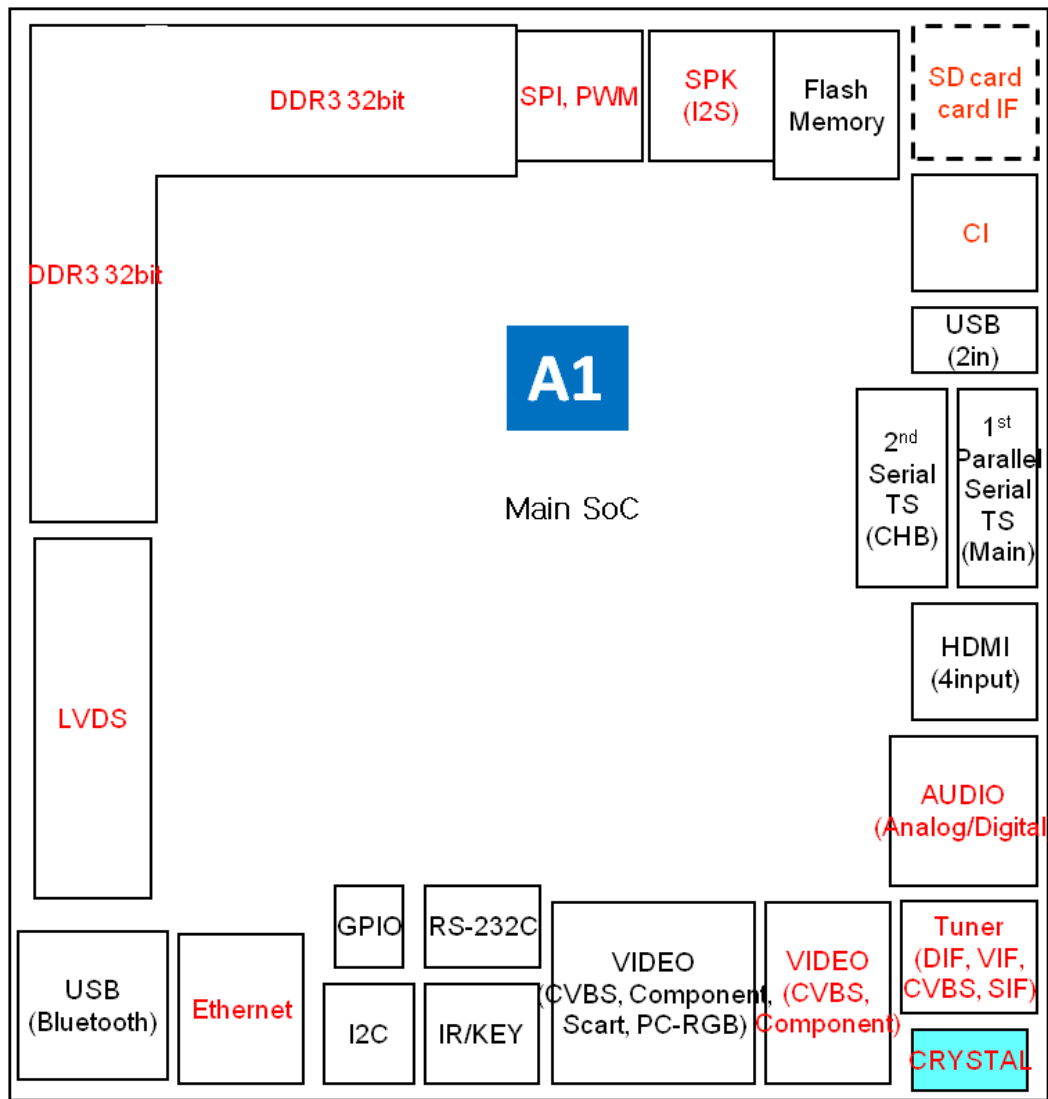


MT5502 (DDR3-1600)

VERSION V1.0

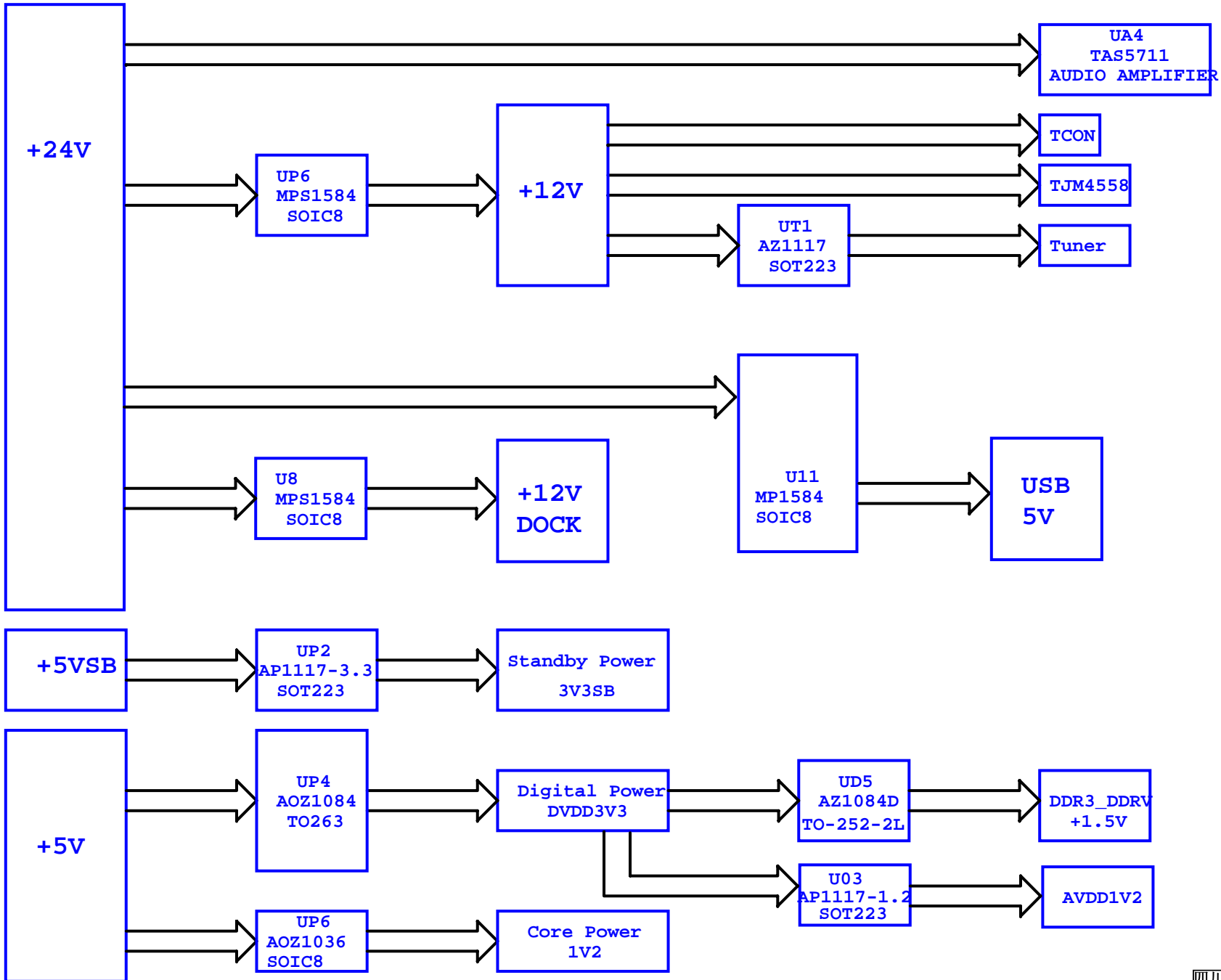


REVISION HISTORY

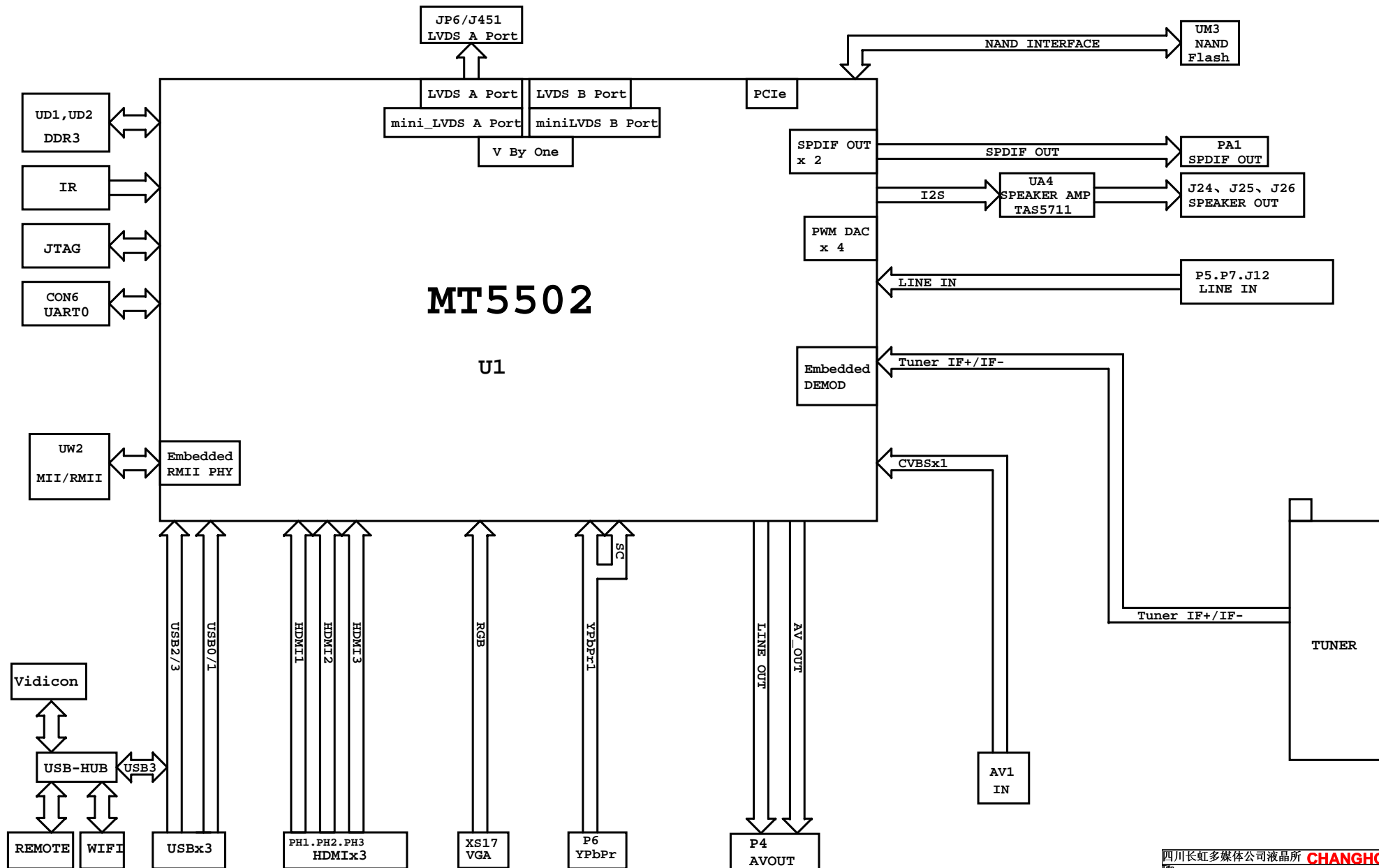
VER.	PAGE#	DESCRIPTION	DATE
1.0		First release	2011/09/13
1.14		增加RB51/RB52/CD63/CD64/C150_pcmcia卡增加4个接地脚	2011/10/13

四川长虹多媒体公司液晶所 CHANGHONG		
Title Placement / Revision history		
Size	Document Number	Rev 1.0
Customer	ChangHong MT5502电路图	
Date: Friday, October 14, 2011	Sheet	0 of 19

POWER TREE



Block Diagram



GPIO LIST

PIN NAME	GPIO Function	Function define
GPIO_0	CI Interface	CI_A0
GPIO_1	CI Interface	CI_A1
GPIO_2	CI Interface	CI_A2
GPIO_3	CI Interface	CI_A3
GPIO_4	CI Interface	CI_A4
GPIO_5	CI Interface	CI_A5
GPIO_6	CI Interface	CI_A6
GPIO_7	CI Interface	CI_A7
GPIO_8	CI Interface	CI_A8
GPIO_9	CI Interface	CI_A9
GPIO_10	CI Interface	CI_A10
GPIO_11	CI Interface	CI_A11
GPIO_12	CI Interface	CI_A12
GPIO_13	CI Interface	CI_A13
GPIO_14	CI Interface	CI_A14
GPIO_15	CI Interface	CI_A15
GPIO_16	CI Interface	CI_A16
GPIO_17	CI Interface	CI_A17
GPIO_18	CI Interface	CI_A18
GPIO_19	CI Interface	CI_A19
GPIO_20	CI Interface	CI_A20
GPIO_21	CI Interface	CI_A21
GPIO_22	CI Interface	CI_A22
GPIO_23	CI Interface	CI_A23
GPIO_24	CI Interface	CI_A24
GPIO_25	CI Interface	CI_A25
GPIO_26	CI Interface	CI_D0
GPIO_27	CI Interface	CI_D1
GPIO_28	CI Interface	CI_D2
GPIO_29	CI Interface	CI_D3
GPIO_30	CI Interface	CI_D4
GPIO_31	CI Interface	CI_D5
GPIO_32	CI Interface	CI_D6
GPIO_33	CI Interface	CI_D7
GPIO_34	CI Interface	CI_D8
GPIO_35	CI Interface	CI_D9
GPIO_36	CI Interface	CI_D10
GPIO_37	CI Interface	CI_D11
GPIO_38	CI Interface	CI_D12
GPIO_39	CI Interface	CI_D13
GPIO_40	CI Interface	CI_D14
GPIO_41	CI Interface	CI_D15
GPIO_42	3D_ENABLE	3D_ENABLE
GPIO_43	USB Power Enable	USB_PWR_EN0
GPIO_44	USB Power Enable	USB_PWR_EN1
GPIO_45	CA_EN	CA_EN
GPIO_46	SYSTEM EEPROM write protect	SYS_EEPROM_WP
GPIO_47	ATV/DTV_AGC_SECLECT	ATV/DTV_AGC_SECLECT
GPIO_48	SD HOT-PLUG	SD_HPD
GPIO_49	SD WP	SD_WP
GPIO_50	AMP RESET	AMP_RESET#
GPIO_51	Audio mute	MUTE_CTL
GPIO_52	OPC_ON/OFF	OPC_ON/OFF
GPIO_53	3D	3D_L/R_SYNC
GPIO_54	2D_SCAN_EN	2D_SCAN_EN
GPIO_55	BOARD CONTROL GLASS	3D_SYNC_GLASS

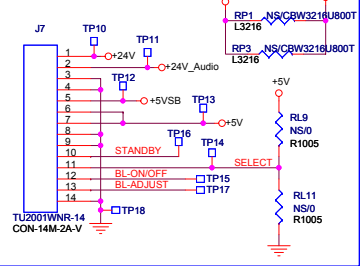
PIN NAME	GPIO Function	Function define
ADIN0_SRV	FHD/HD SELECT	FHD/HD SELECT
ADIN1_SRV		
ADIN2_SRV	USB over current detect	USB_OC_P0/P1
ADIN3_SRV	USB over current detect	USB_OC_P2/P3
ADIN4_SRV	KEY0 DETECT	KEY0
ADIN5_SRV	KEY1 DETECT	KEY1
ADIN6_SRV	Demo RF AGC	RF_AGC
ADIN7_SRV	CI Card Power Control	CI_PWR_EN

PIN NAME	GPIO Function	Function define
OPCTRL0	LED0 INDICATOR	OPCTRL0_LED0
OPCTRL1	LED1 INDICATOR	OPCTRL1_LED1
OPCTRL2	NAND_WP#	NAND_WP#
OPCTRL3	Strapping	Strap[0]
OPCTRL4	BL CONTROL	BL_ON/OFF
OPCTRL5	CI_OCP	CI_OCP
OPCTRL6	3D_SYNC_IN	3D_SYNC_IN
OPCTRL7	USB HUB RESET	USB2_RST
OPCTRL8	WIFI CONTROL	WIFI_CTRL
OPCTRL9	LVDS Power Control	LVDS_PWR_EN
OPCTRL10	LNA\$ON/OFF	LNA\$ON/OFF
OPCTRL11	USB Power Enable	USB_PWR_EN2

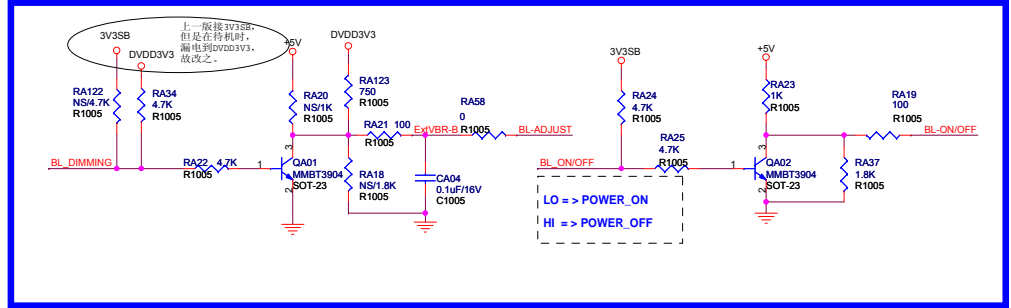
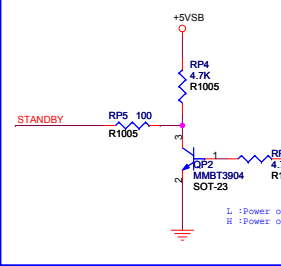
PIN NAME	GPIO Function	Function define
LED_PWM0	Strap[2]	3D_SYNC_CODE_OUT
LED_PWM1	Strap[1]	Strap[1]

PIN NAME	GPIO Function	Function define
OPWM0	ODSEL	ODSEL
OPWM1	Back light DIMMING	BL_DIMMING
OPWM2		

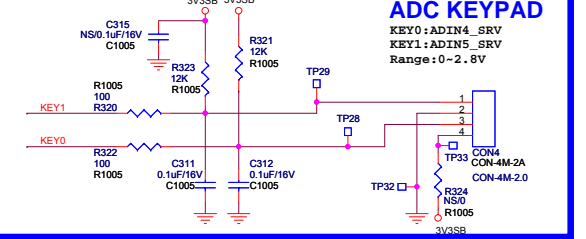
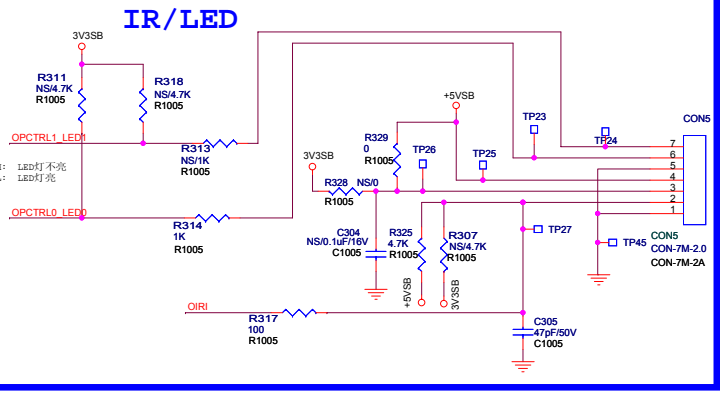
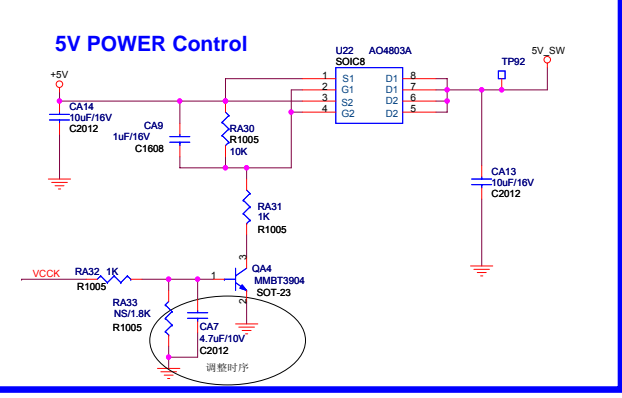
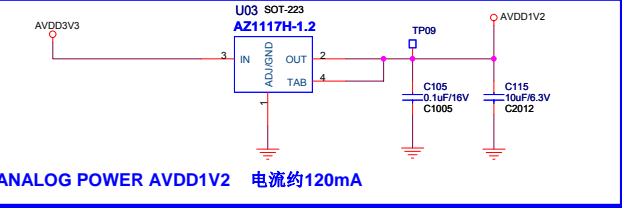
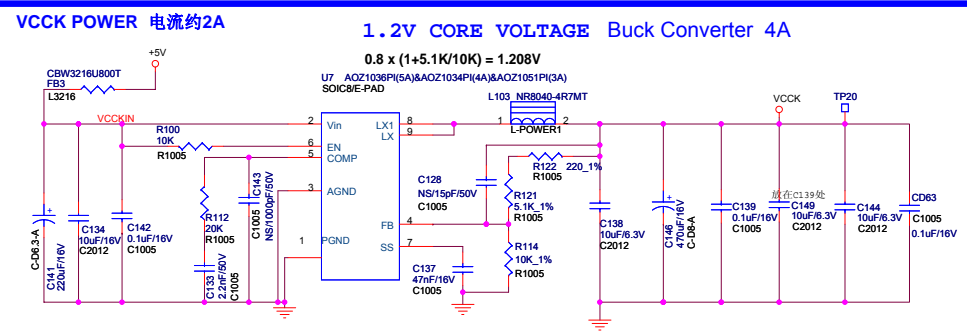
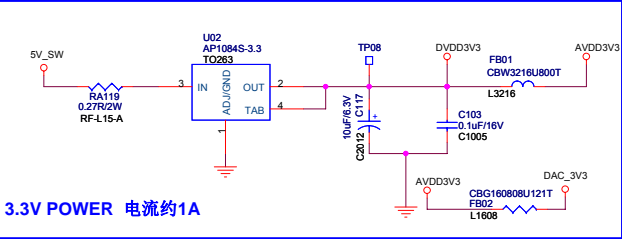
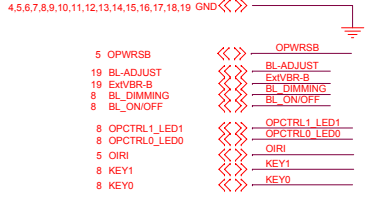
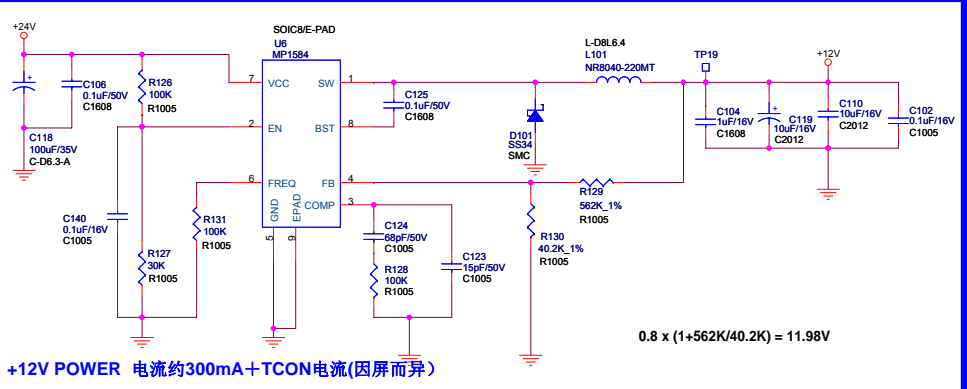
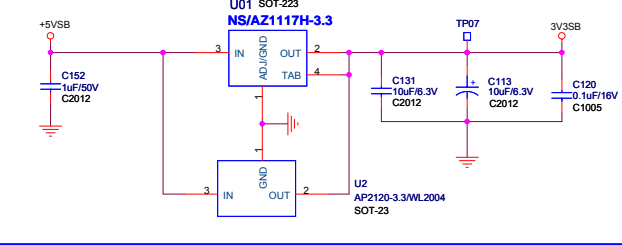
LCD MAIN POWER

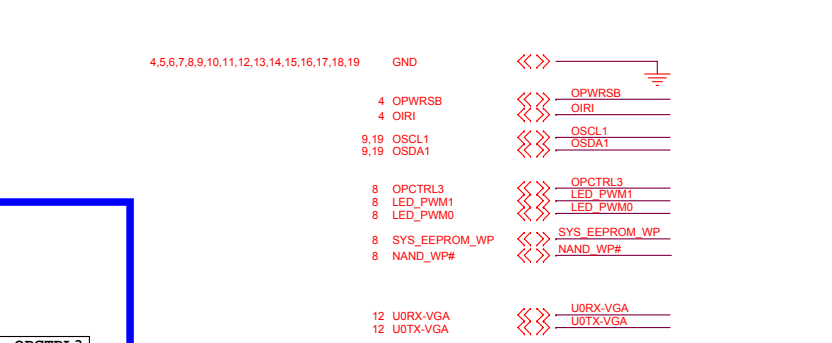
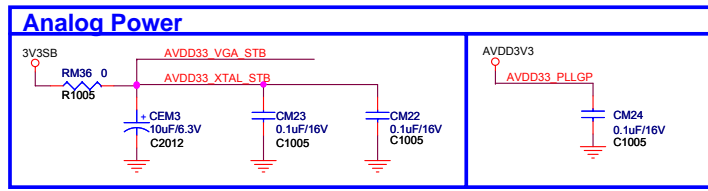
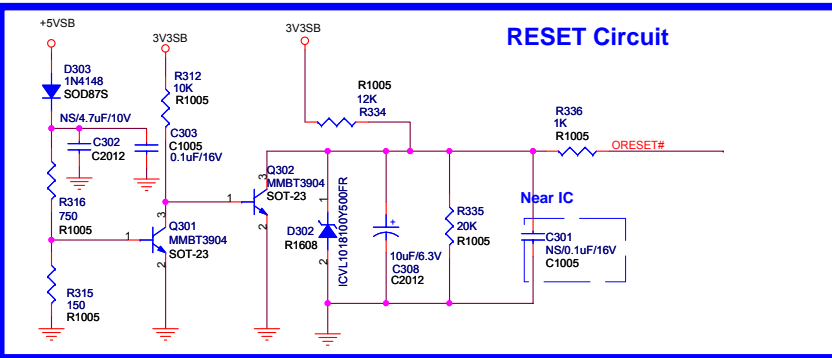
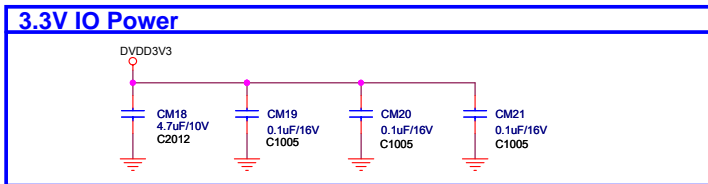
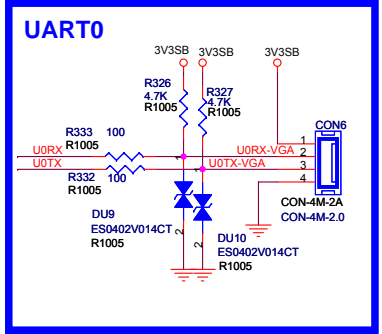
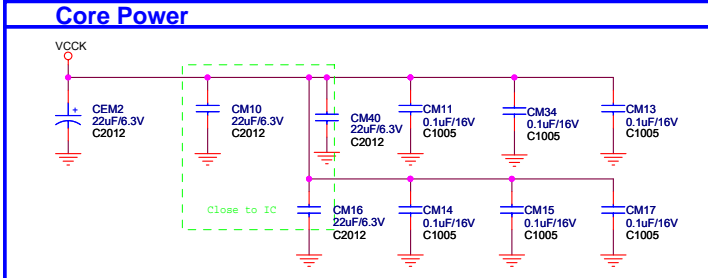
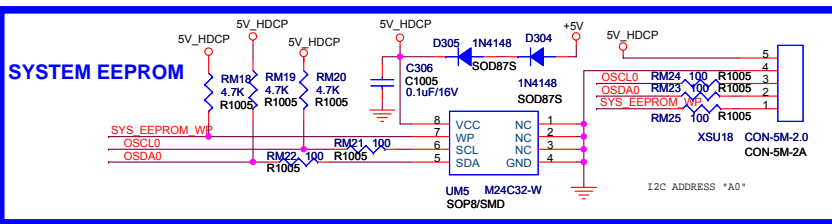
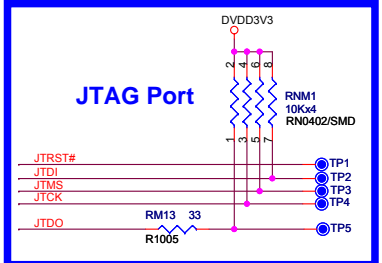
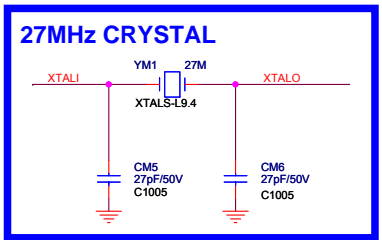
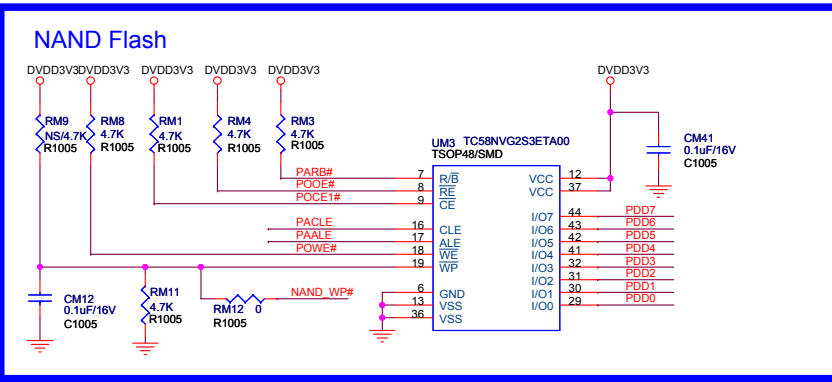
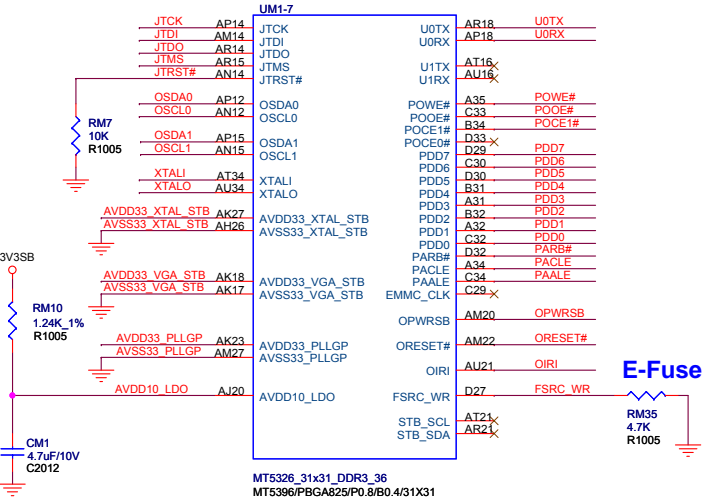


Standby controller



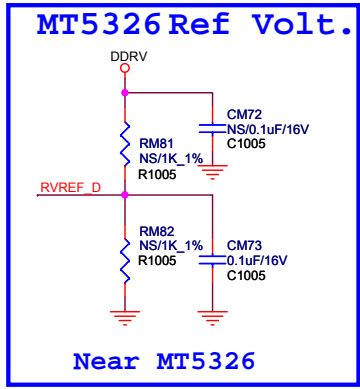
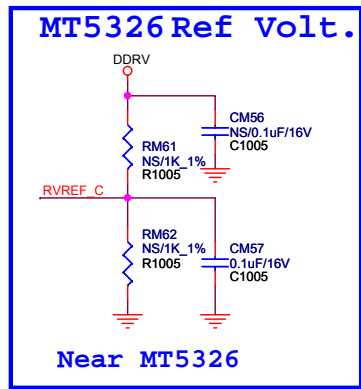
STANDBY POWER 3V3SB 电流约25mA



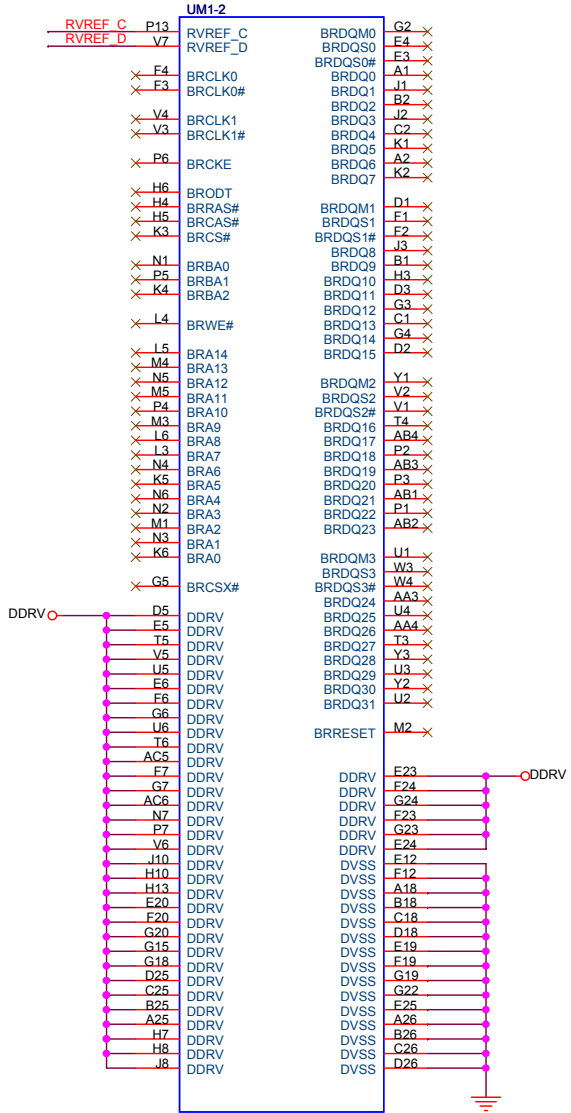
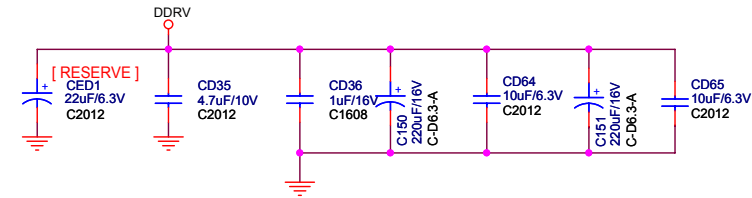
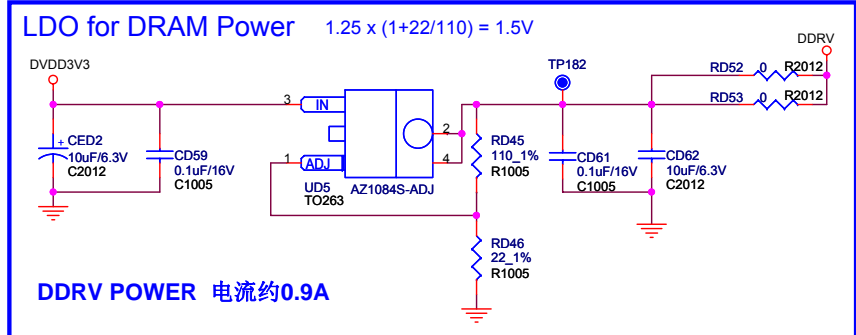


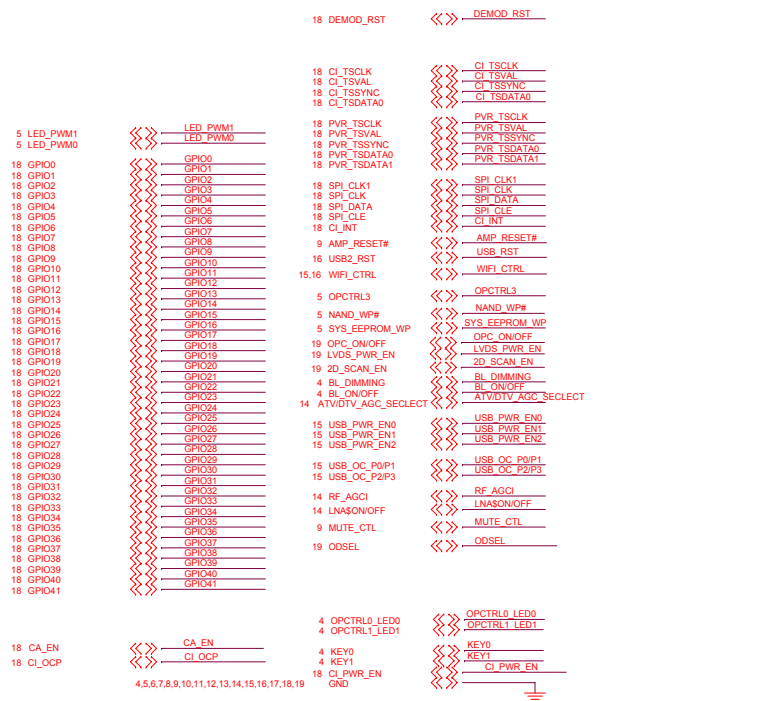
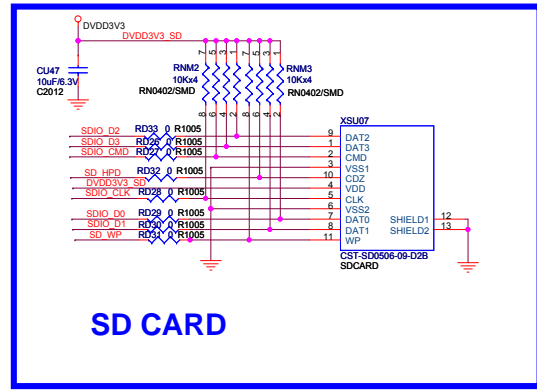
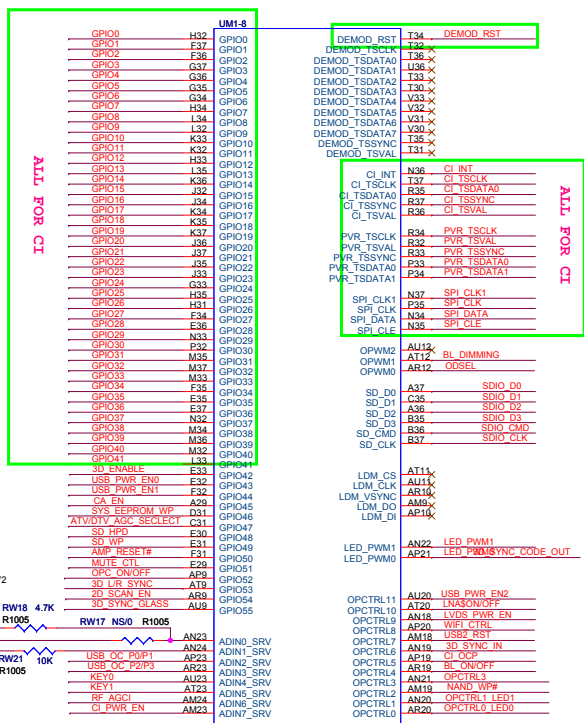
STRAPPING

STRAPPING	LED_PWM0	LED_PWM1	OPCTRL3
ICE mode + 27M + serial boot	0	0	0
ICE mode + 27M + ROM to Nand boot	0	0	1
ICE mode + 27M + ROM to eMMC boot from eMMC pins (share pins w/s NAND)	0	1	0
ICE mode + 27M + ROM to eMMC boot from SDIO pins	0	1	1

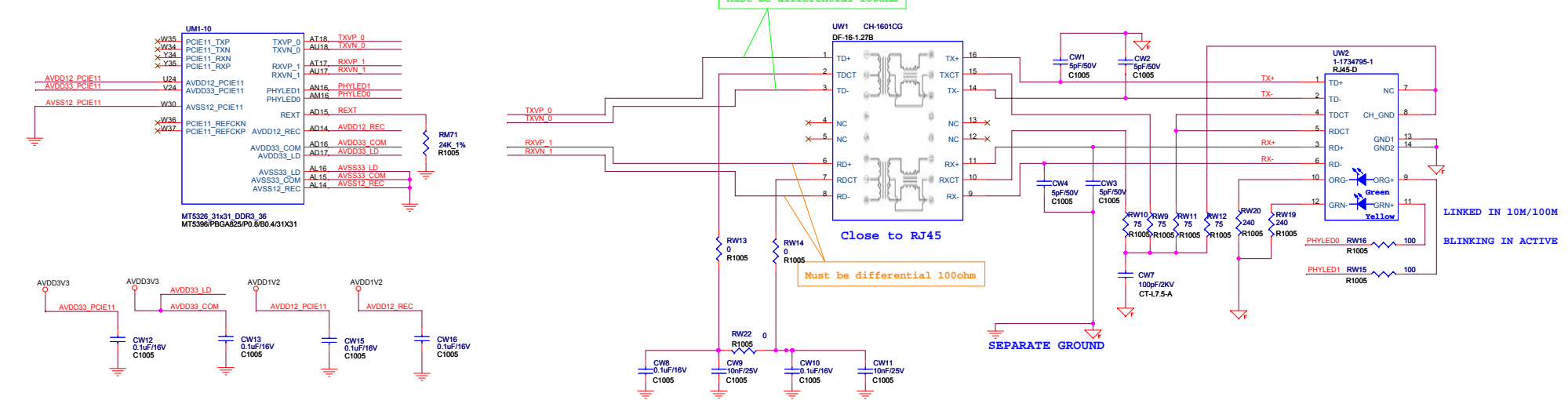


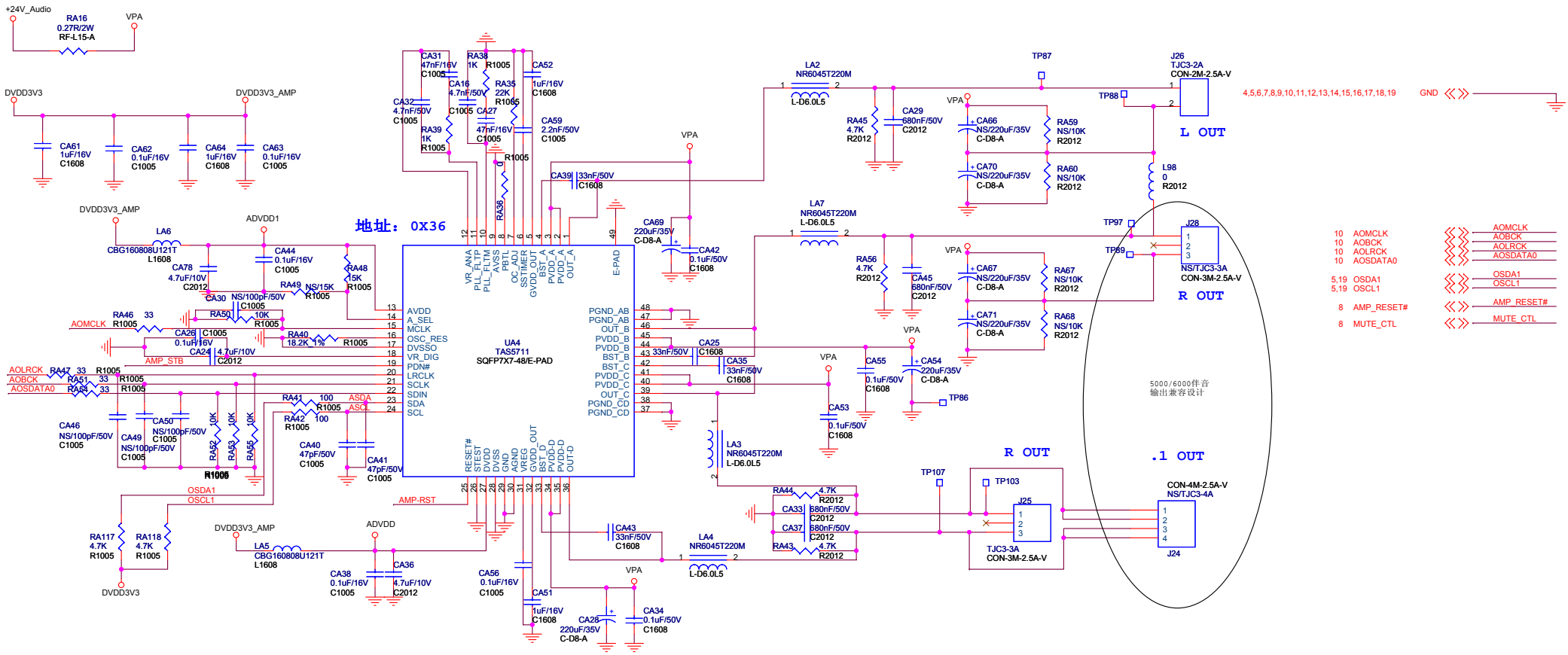
4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19 GND <<>> GND
 6 RVREF_C <<>> RVREF_C
 6 RVREF_D <<>> RVREF_D





ETHERNET PHY





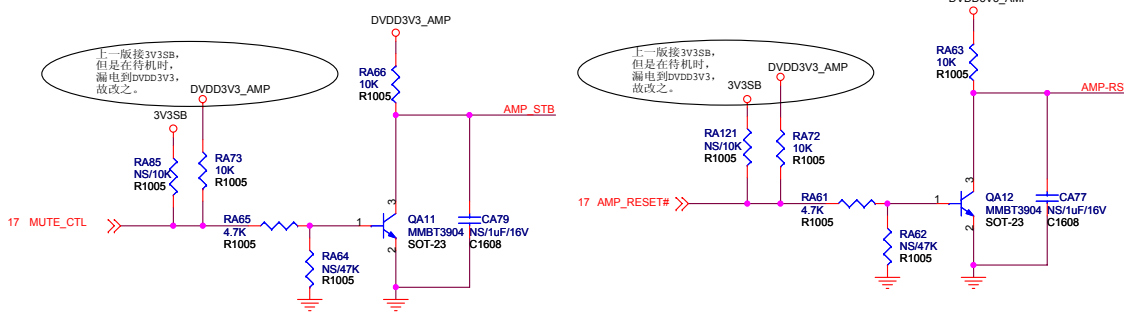
地址: 0X36

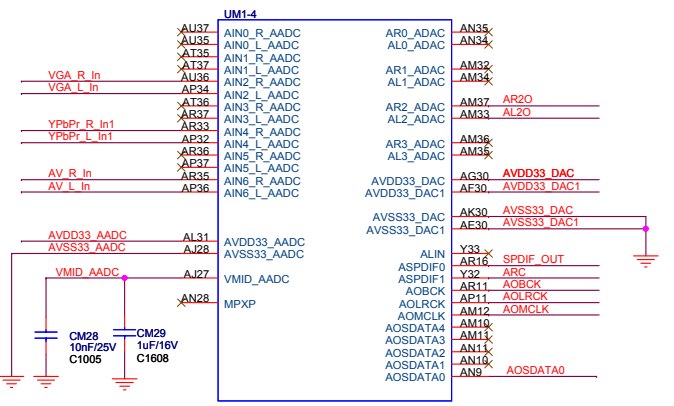
5000/6000件音
输出兼容设计

- 10 AOMCLK <<<<<< AOMCLK
- 10 AOBCK <<<<<< AOBCK
- 10 AOLRCK <<<<<< AOLRCK
- 10 AOSDATA0 <<<<<< AOSDATA0
- 5,19 OSDA1 <<<<<< OSDA1
- 5,19 OSCL1 <<<<<< OSCL1
- 8 AMP_RESET# <<<<<< AMP_RESET#
- 8 MUTE_CTL <<<<<< MUTE_CTL

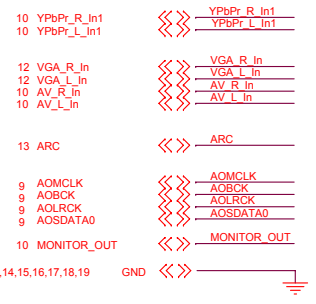
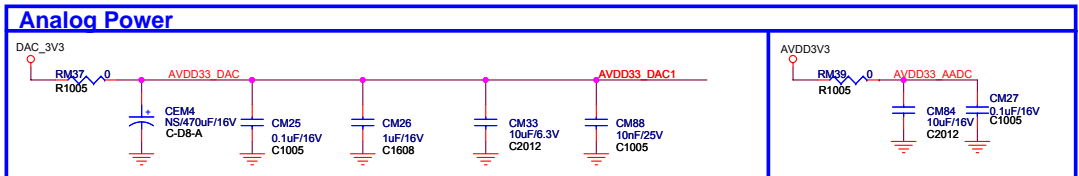
上一版接3V3SB，
但是在待机时，
漏电流到DVDD3V3，
故改之。

上一版接3V3SB，
但是在待机时，
漏电流到DVDD3V3，
故改之。

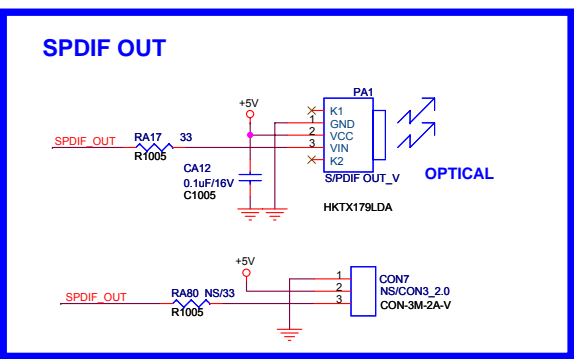
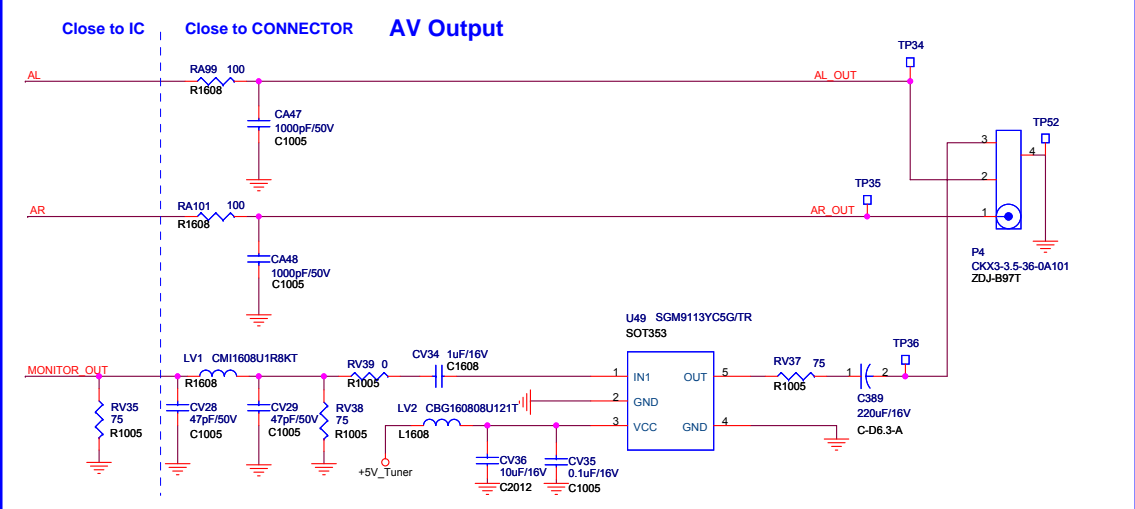
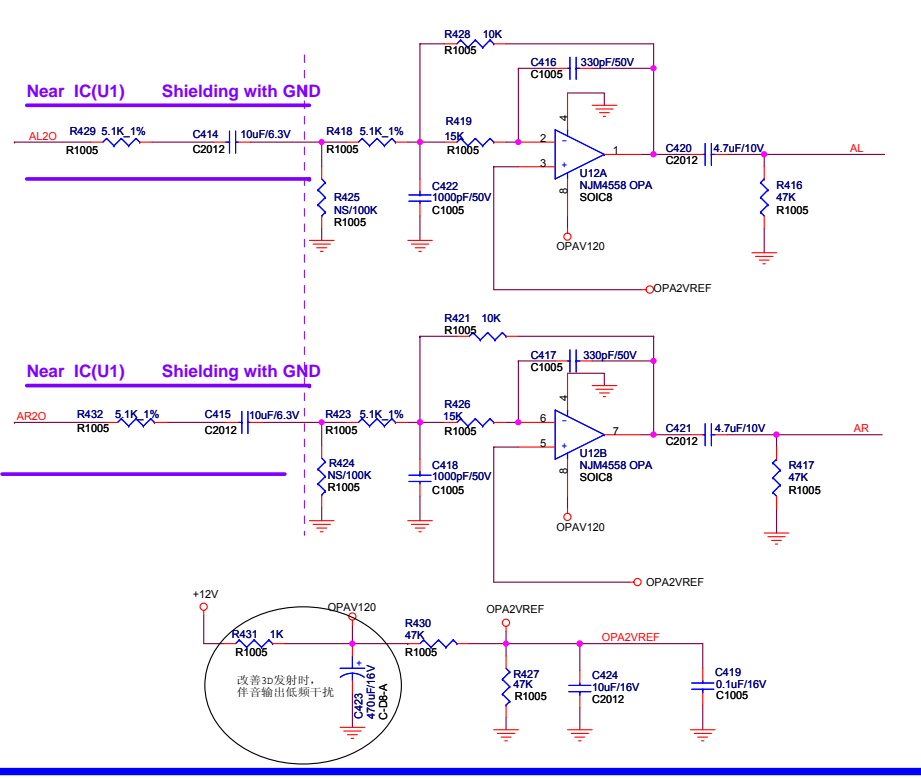


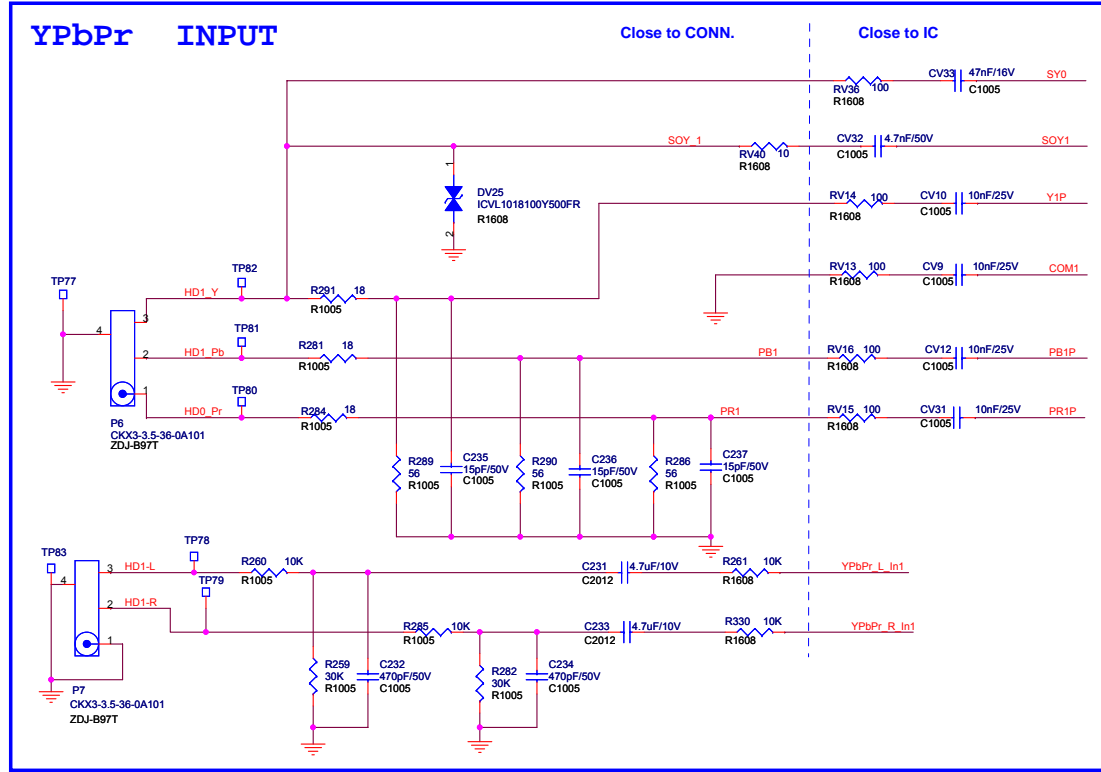
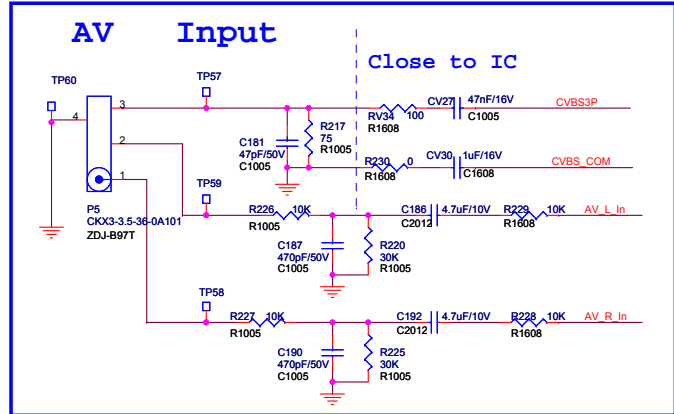
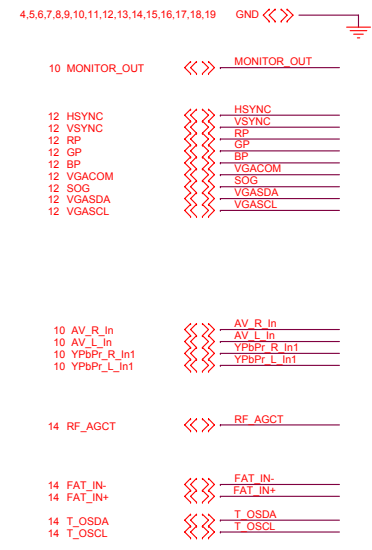
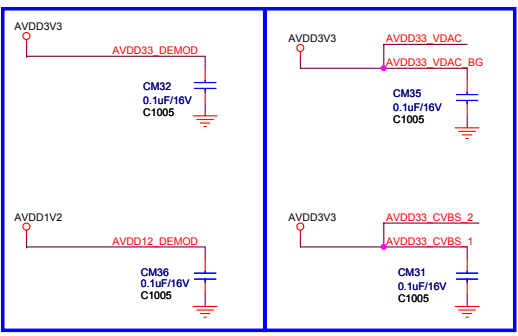
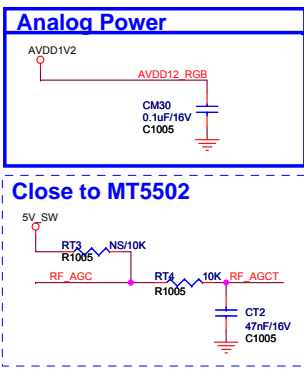
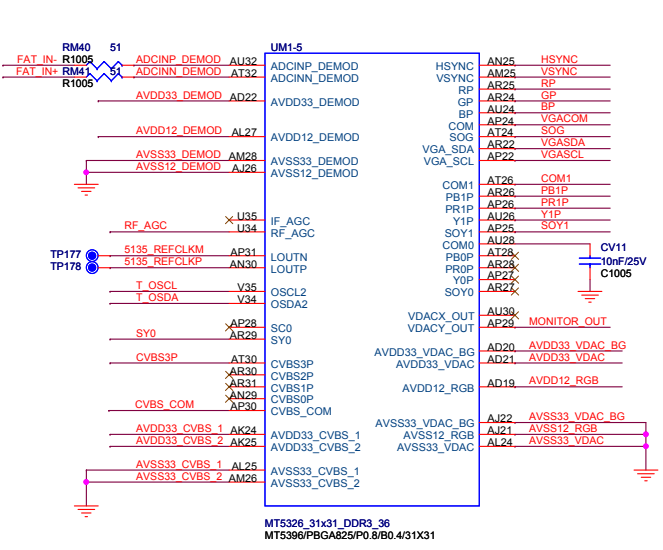


MT5326_31x31_DDR3_36
 MT5396/PBGA825/P0.8/60.4/31X31

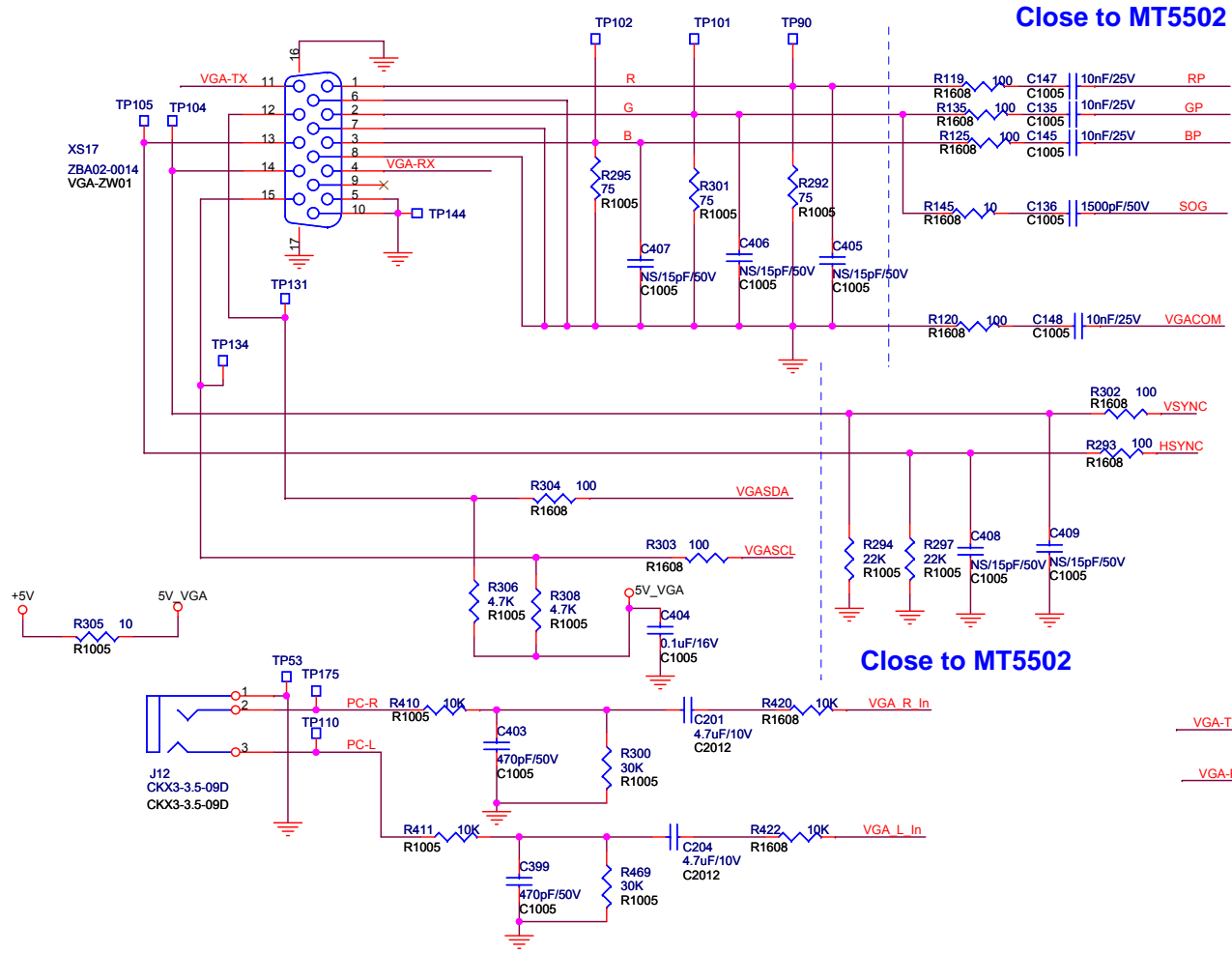


D/A and OP Circuit For AVout



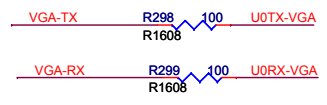


VGA Input



4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19 GND <<>>

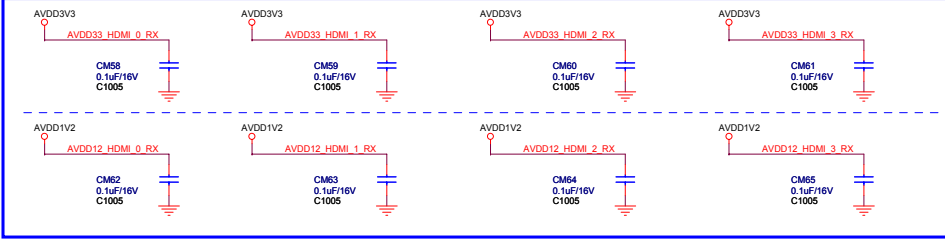
10	VGA_R_In	<<>>	VGA_R_In
10	VGA_L_In	<<>>	VGA_L_In
11	HSYNC	<<>>	HSYNC
11	VSYNC	<<>>	VSYNC
11	RP	<<>>	RP
11	GP	<<>>	GP
11	BP	<<>>	BP
11	VGACOM	<<>>	VGACOM
11	SOG	<<>>	SOG
11	VGASDA	<<>>	VGASDA
11	VGASCL	<<>>	VGASCL
5	U0RX-VGA	<<>>	U0RX-VGA
5	U0TX-VGA	<<>>	U0TX-VGA



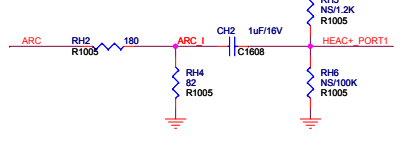
四川长虹多媒体公司液晶所 CHANGHONG		
Title		
VGA Input		
Size	Document Number	Rev
B	ChangHong MT5502电路图	1.0
Date:	Sunday, November 27, 2011	Sheet 12 of 19

UM1-6			
HDMI_CEC	AA32	HDMI_CEC	HDMI_0_RX_0
HDMI_0_SCL	AG33	HDMI_0_SCL	HDMI_0_RX_0B
HDMI_1_SCL	AE33	HDMI_1_SCL	HDMI_0_RX_1
HDMI_3_SCL	AH32	HDMI_3_SCL	HDMI_0_RX_1B
HDMI_0_SDA	AF33	HDMI_0_SDA	HDMI_0_RX_2
HDMI_1_SDA	AD33	HDMI_1_SDA	HDMI_0_RX_2B
HDMI_3_SDA	AH33	HDMI_3_SDA	HDMI_0_RX_C
HDMI_0_PWRSV	AG31	HDMI_0_PWRSV	HDMI_0_RX_CB
HDMI_1_PWRSV	AE31	HDMI_1_PWRSV	HDMI_1_RX_0
HDMI_3_PWRSV	AH31	HDMI_3_PWRSV	HDMI_1_RX_0B
HDMI_0_HPD	AG32	HDMI_0_HPD	HDMI_1_RX_1
HDMI_1_HPD	AE32	HDMI_1_HPD	HDMI_1_RX_1B
HDMI_3_HPD	AH32	HDMI_3_HPD	HDMI_1_RX_2
AVDD12_HDMI_0_RX	AA24	AVDD12_HDMI_0_RX	HDMI_1_RX_2B
AVDD12_HDMI_1_RX	AA24	AVDD12_HDMI_1_RX	HDMI_1_RX_C
AVDD12_HDMI_2_RX	AA24	AVDD12_HDMI_2_RX	HDMI_1_RX_CB
AVDD12_HDMI_3_RX	AA24	AVDD12_HDMI_3_RX	HDMI_2_RX_0
AVDD33_HDMI_0_RX	AB29	AVDD33_HDMI_0_RX	HDMI_2_RX_0B
AVDD33_HDMI_1_RX	AA29	AVDD33_HDMI_1_RX	HDMI_2_RX_1
AVDD33_HDMI_2_RX	Y29	AVDD33_HDMI_2_RX	HDMI_2_RX_1B
AVDD33_HDMI_3_RX	AC29	AVDD33_HDMI_3_RX	HDMI_2_RX_2
AVSS33_HDMI_RX	AB30	AVSS33_HDMI_RX	HDMI_2_RX_2B
AVSS33_HDMI_RX	AD30	AVSS33_HDMI_RX	HDMI_2_RX_C
AVSS33_HDMI_RX	AE31	AVSS33_HDMI_RX	HDMI_2_RX_CB
AVSS33_HDMI_RX	AF32	AVSS33_HDMI_RX	HDMI_3_RX_0
			HDMI_3_RX_0B
			HDMI_3_RX_1
			HDMI_3_RX_1B
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			HDMI_3_RX_2B
			HDMI_3_RX_C
			HDMI_3_RX_CB

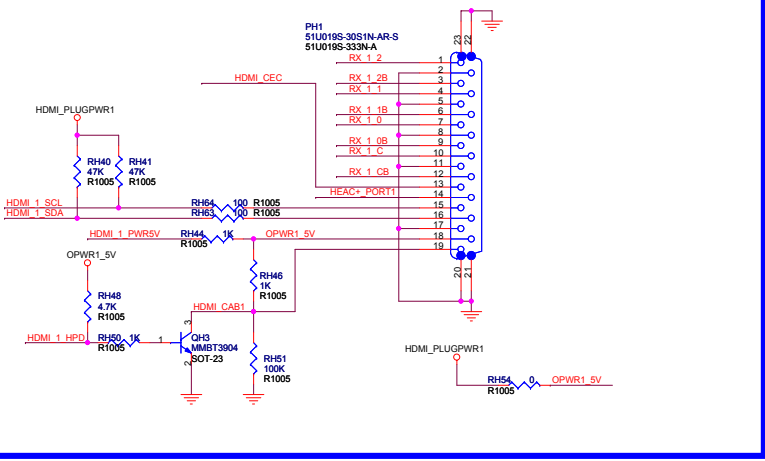
Analog Power



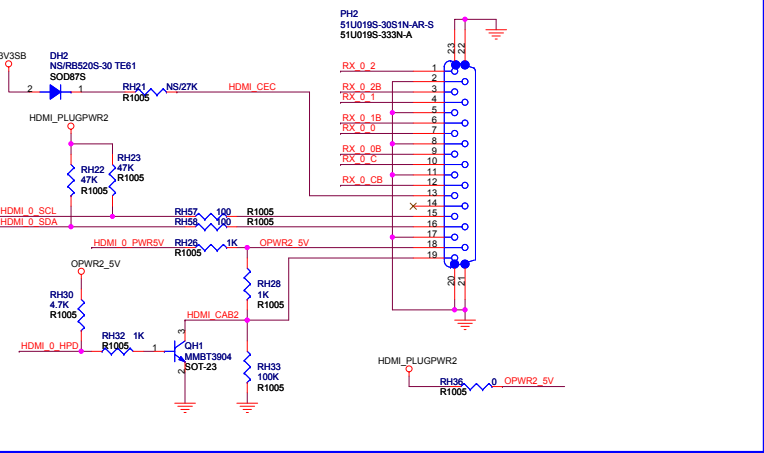
HDMI 1.4 Single mode-ARC



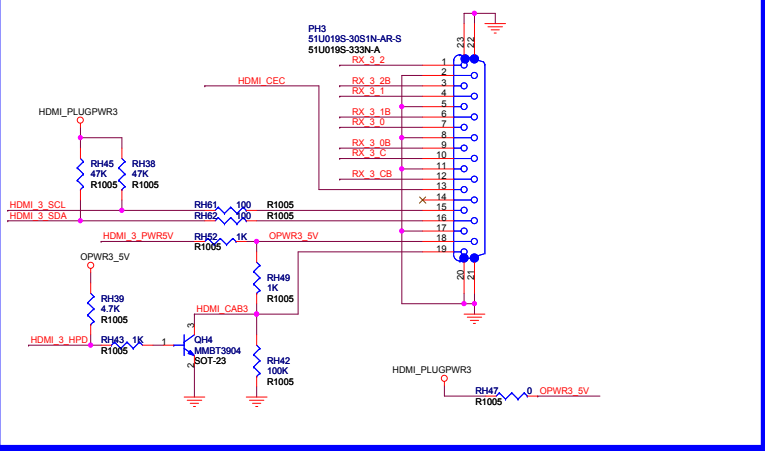
HDMI port 1 (MT5502 Support Embedded EDID)

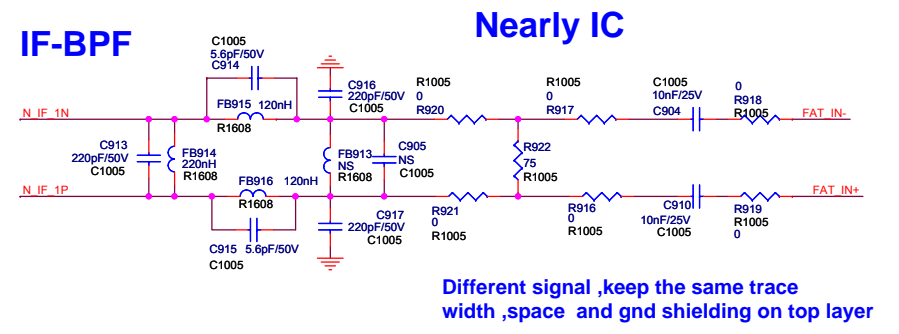
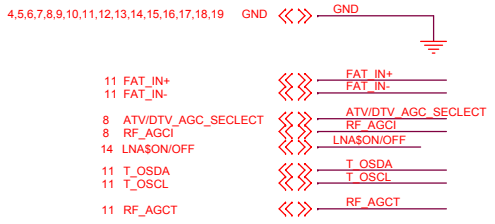
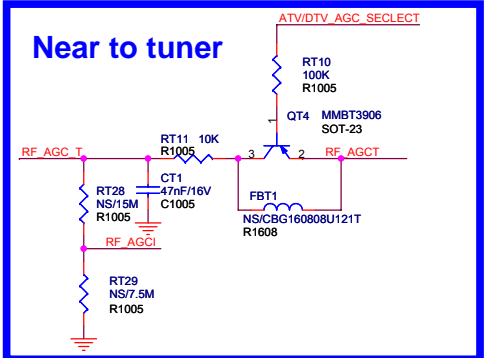
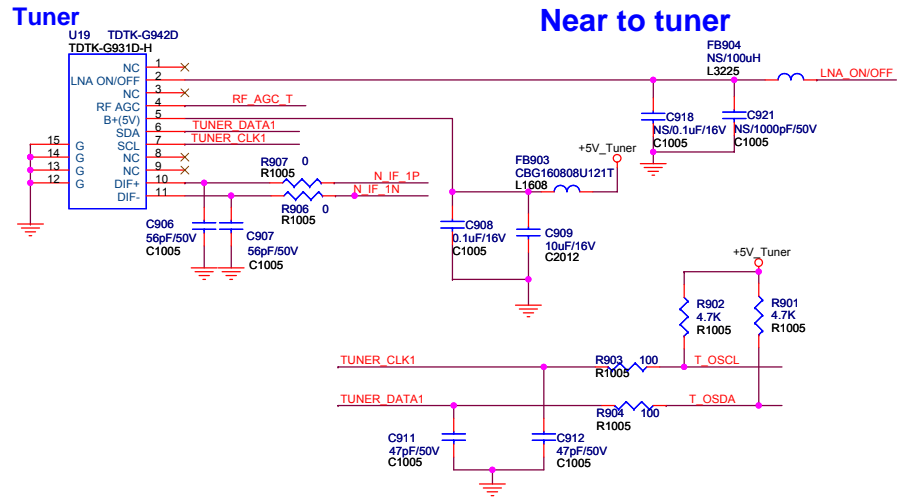


HDMI port 2 (MT5502 Support Embedded EDID)

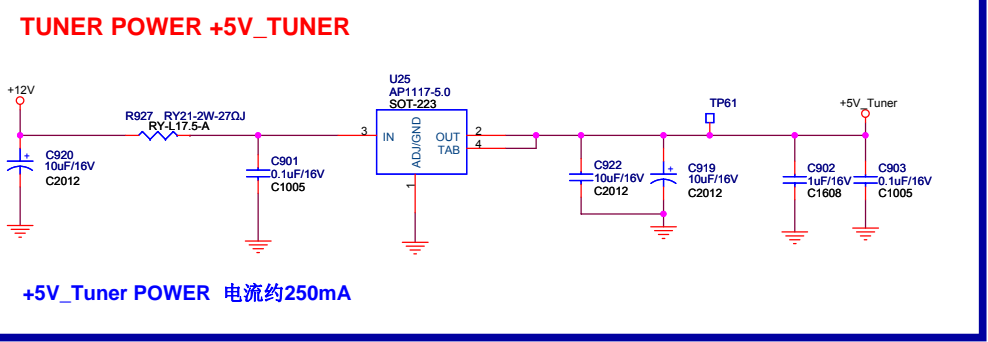
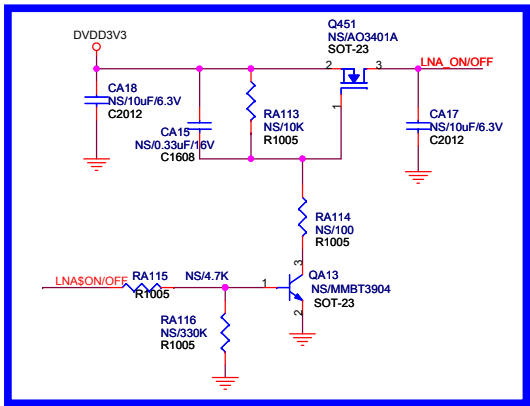


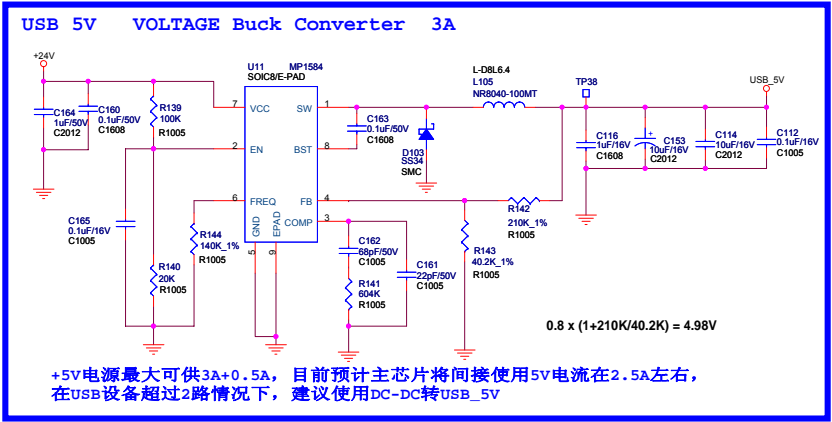
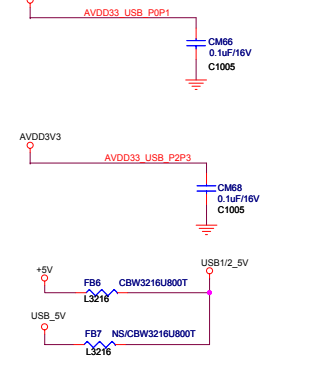
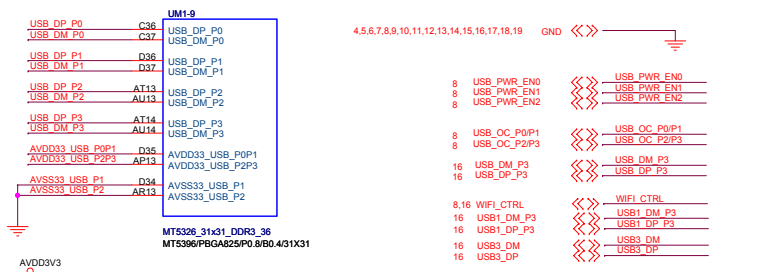
HDMI port 3 (MT5502 Support Embedded EDID)



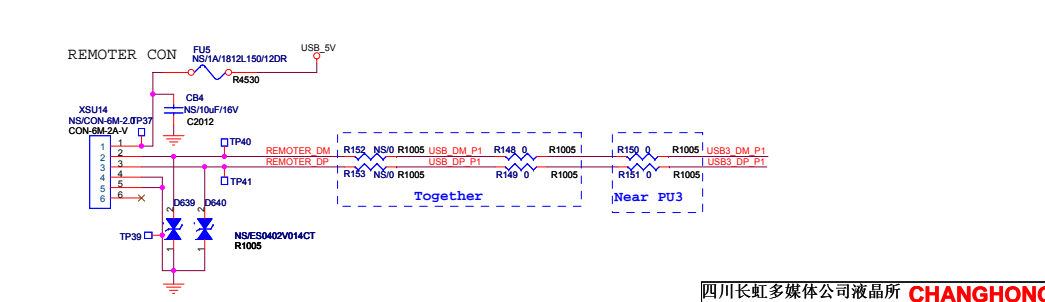
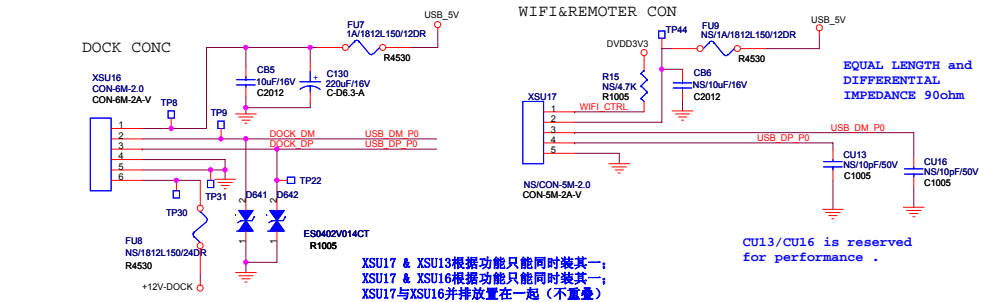
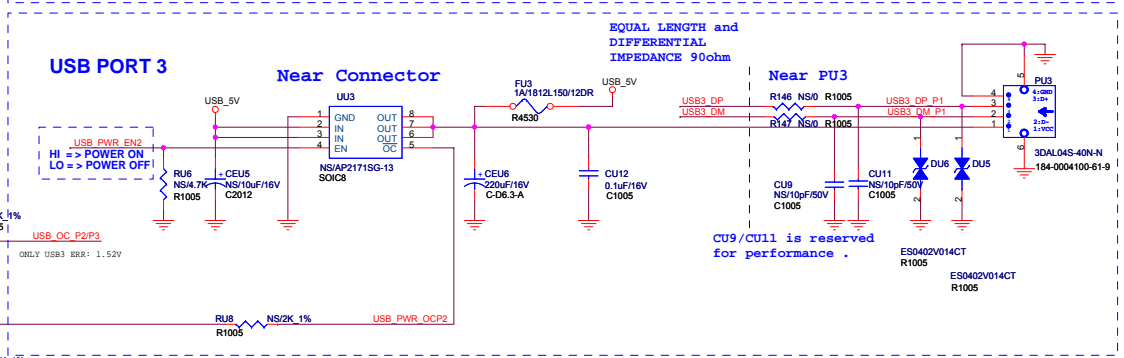
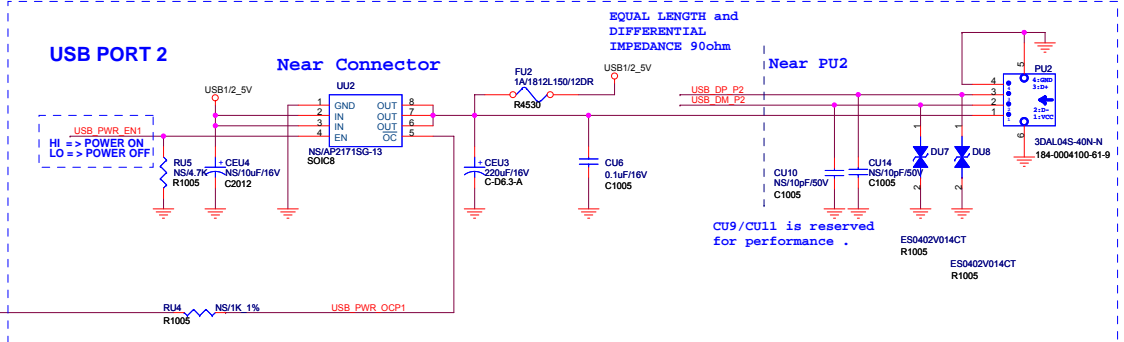
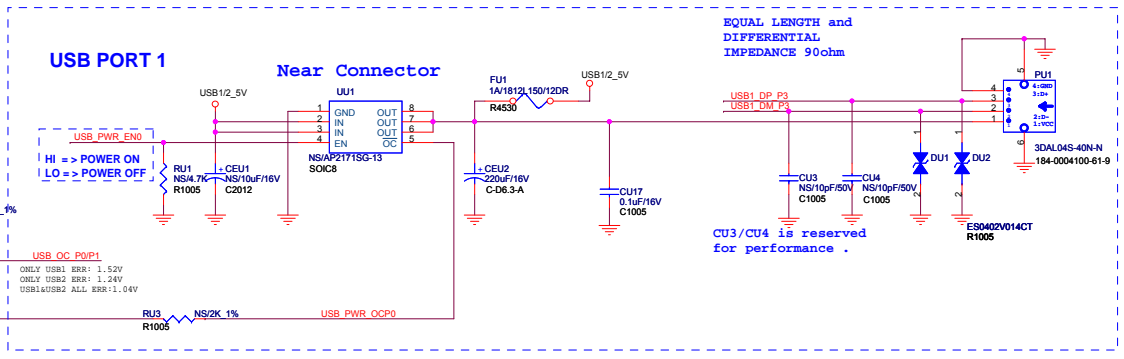


Different signal ,keep the same trace width ,space and gnd shielding on top layer

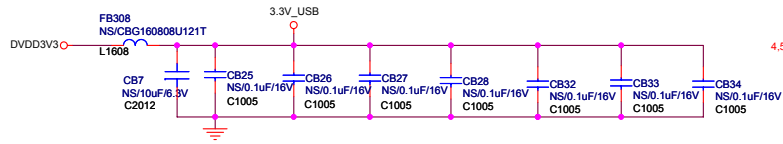
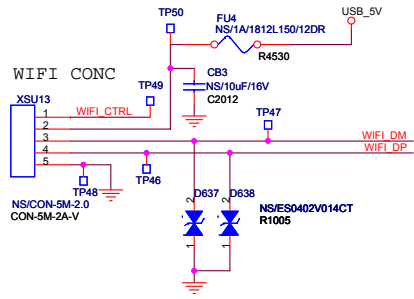




3 Ports of USB

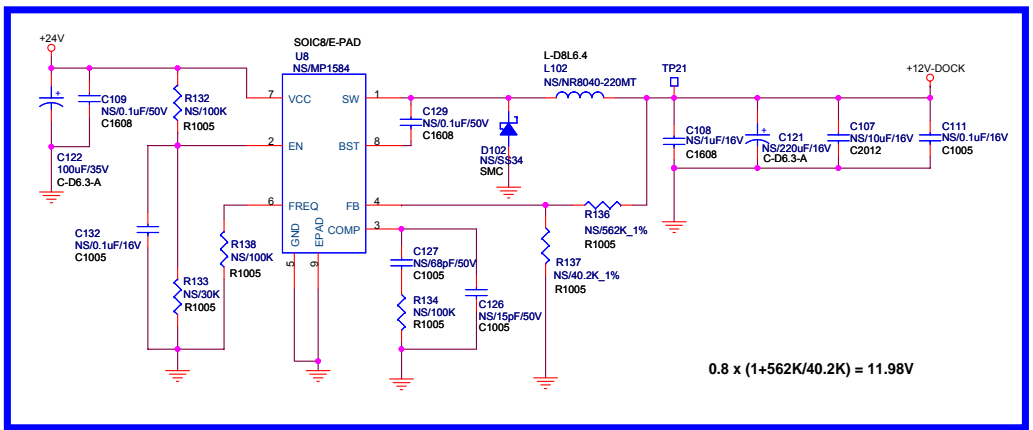
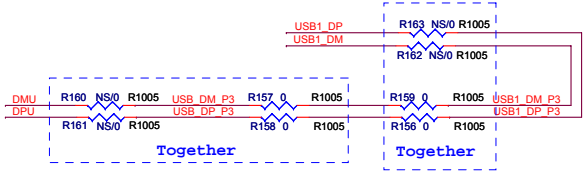
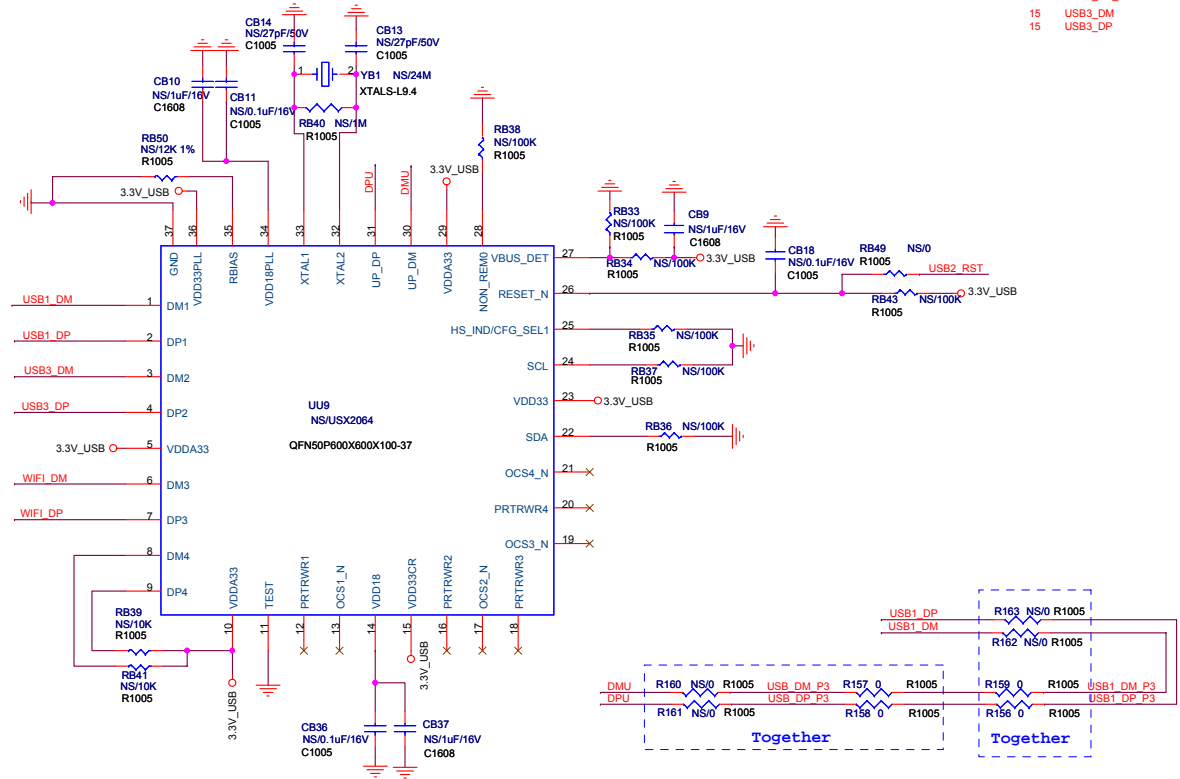


XSU17 & XSU13根据功能只能同时装其一;
XSU17 & XSU16根据功能只能同时装其一;
XSU17与XSU16并排放置在一起(不重叠)



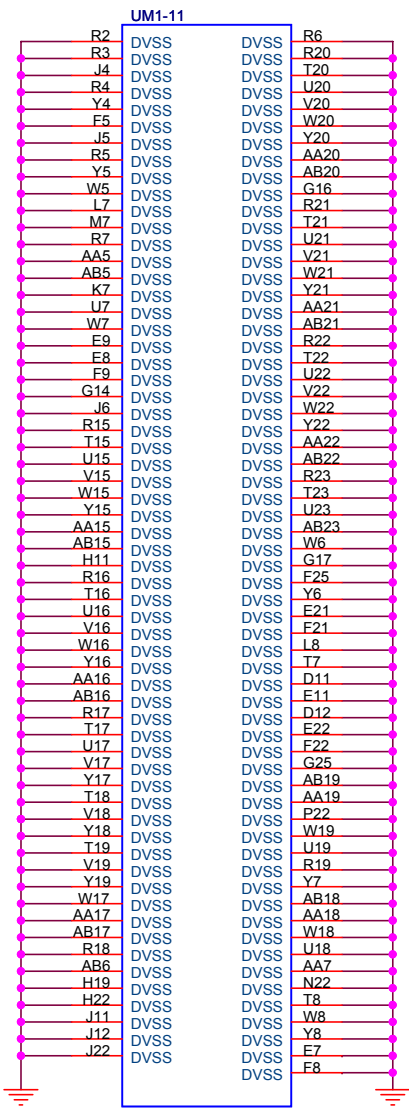
4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19 GND

- 15 USB_DM_P3
- 15 USB_DP_P3
- 8,15 WIFI_CTRL
- 8 USB2_RST
- 15 USB1_DM_P3
- 15 USB1_DP_P3
- 15 USB3_DM
- 15 USB3_DP

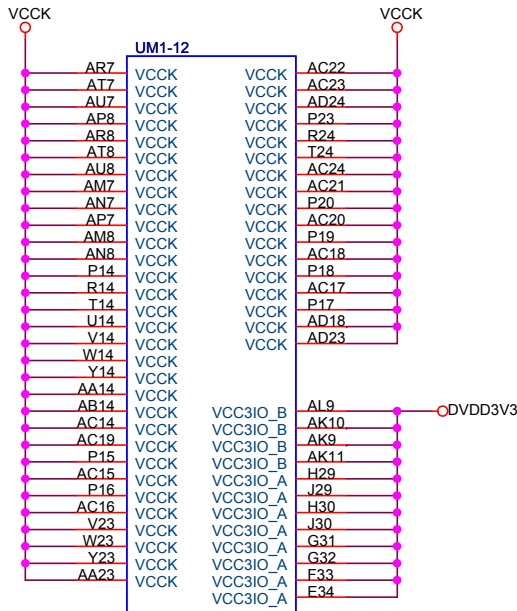


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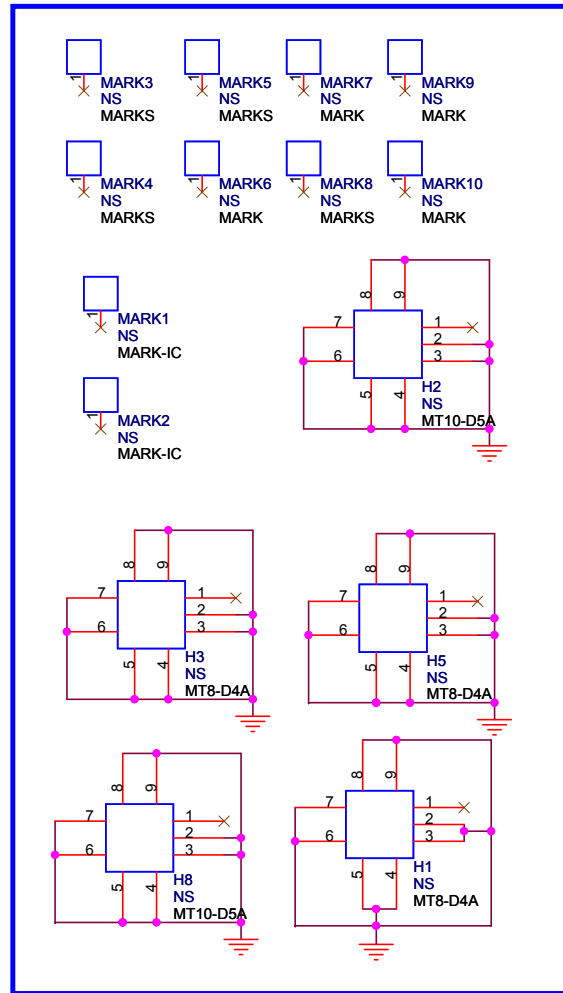
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Size	Document Number	Rev
Customer	ChangHong MT5502	1.0
Date:	Saturday, November 26, 2011	Sheet 16 of 19



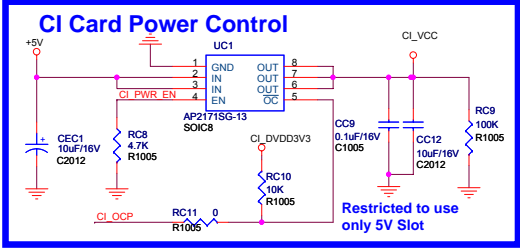
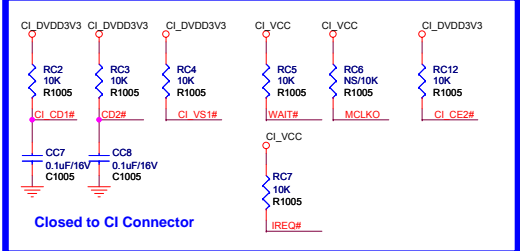
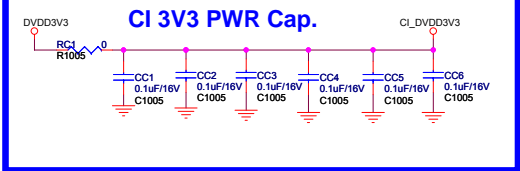
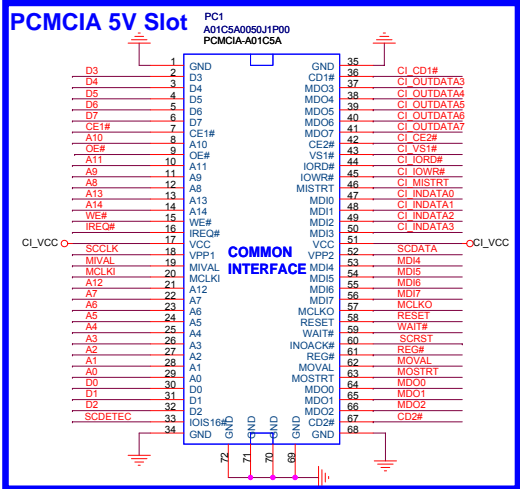
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MT5396/PBGA825/P0.8/B0.4/31X31



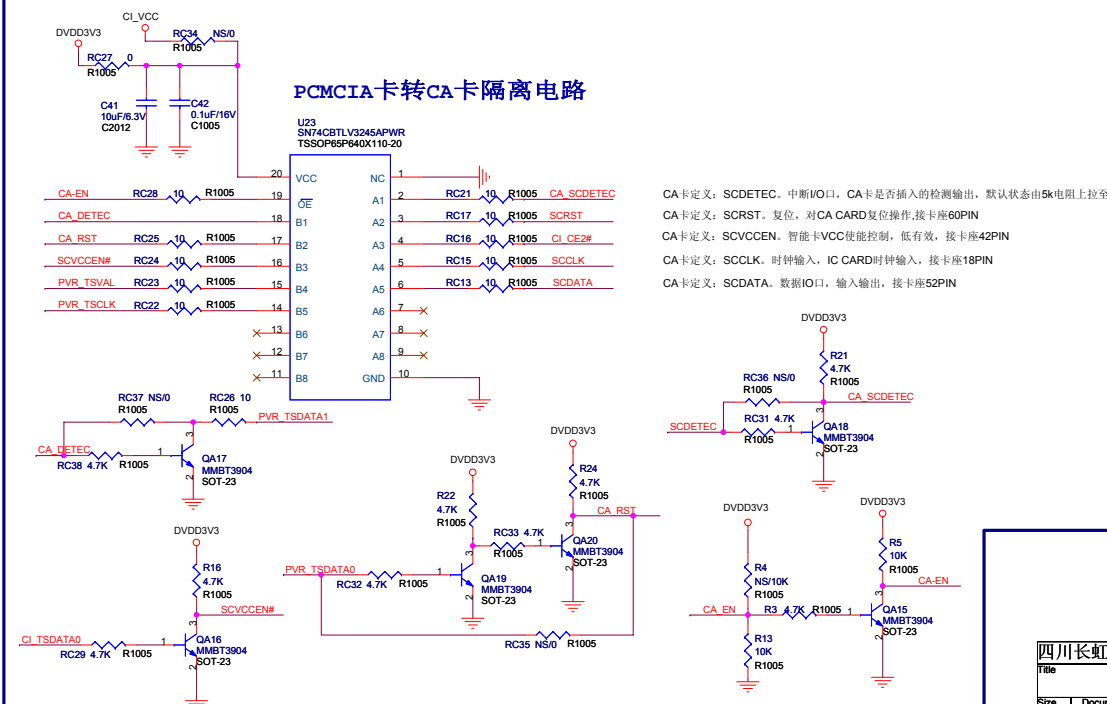
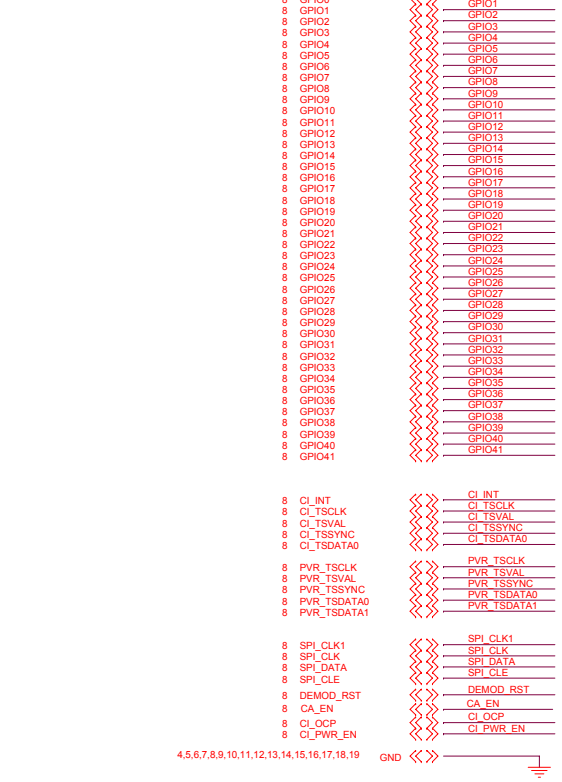
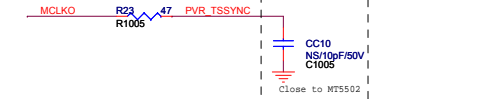
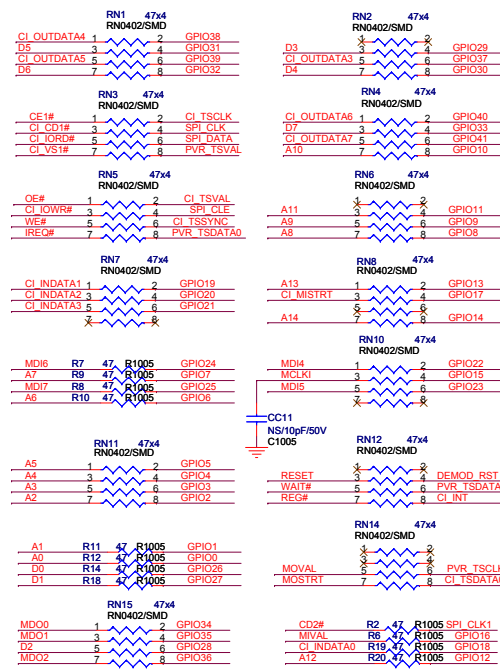
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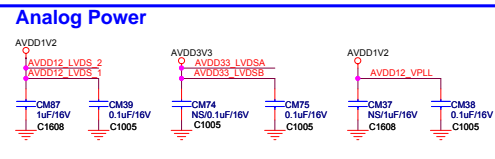
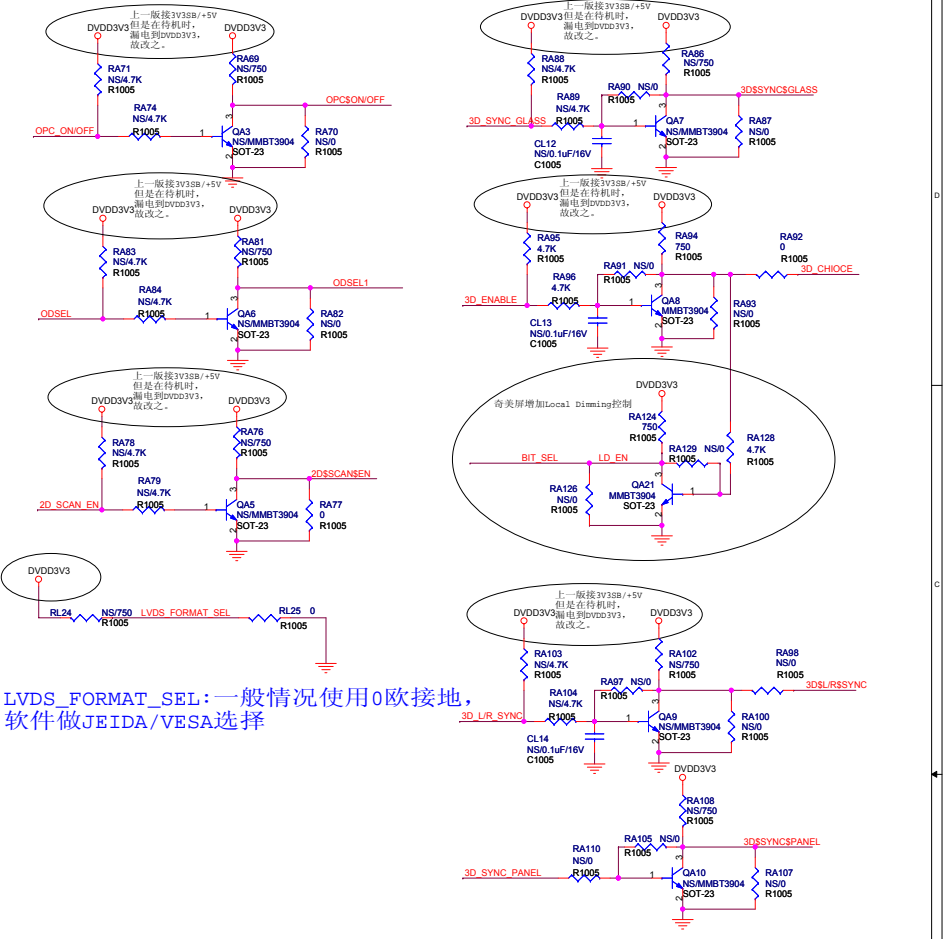
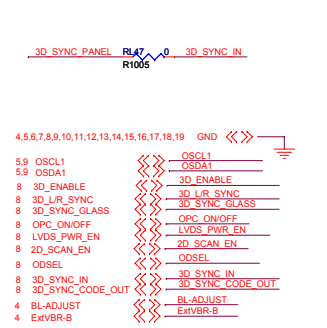
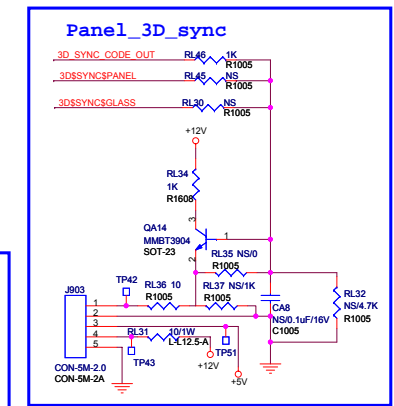
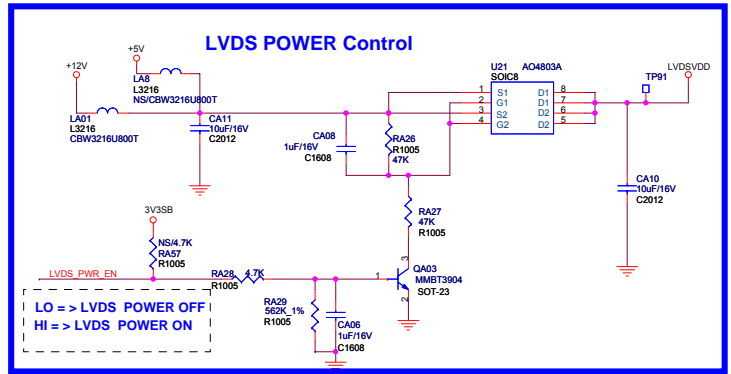
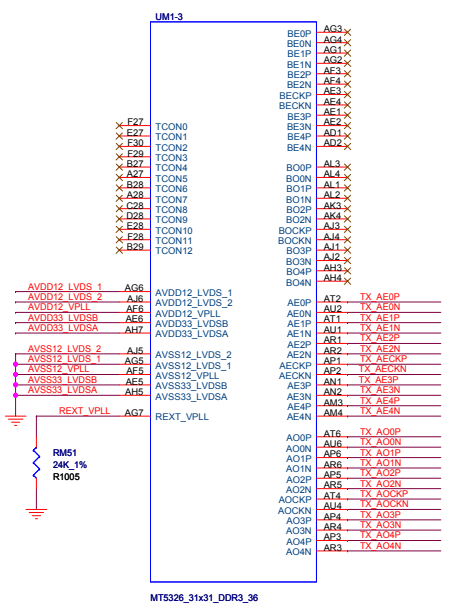
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Title VCCk & DVSS		
Size Custom	Document Number ChangHong MT5502电路图	Rev 1.0
Date: Monday, November 21, 2011	Sheet 17 of 19	



Parrel TS Output to PCMCIA damping close to MT5502	Parrel TS Output to MT5502 damping close to PCMCIA
CI_MISTR	MOVAL
CI_INDATA0	MOSTRT
CI_INDATA1	CI_OUTDATA0
CI_INDATA2	CI_OUTDATA1
CI_INDATA3	CI_OUTDATA2
CI_INDATA4	CI_OUTDATA4
CI_INDATA5	CI_OUTDATA5
CI_INDATA6	CI_OUTDATA6
CI_INDATA7	CI_OUTDATA7
MIVAL	MCLKO
MCLKI	CI_OUTDATA3

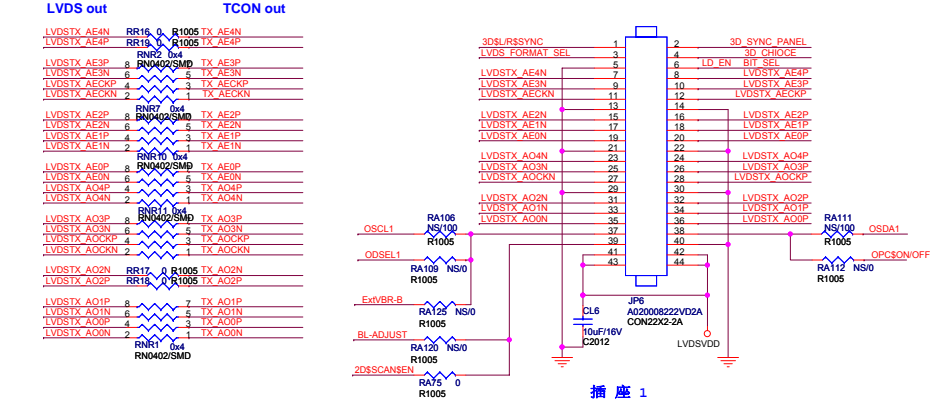


CA卡定义: SCDETEC. 中断I/O口. CA卡是否插入的检测输出, 默认状态由5k电阻上拉至5V, 接卡座33PIN
 CA卡定义: SCRST. 复位, 对CA CARD位操作接卡座60PIN
 CA卡定义: SCVCCEN. 智能卡VCC使能控制, 低有效, 接卡座42PIN
 CA卡定义: SCCLK. 时钟输入, IC CARD时钟输入, 接卡座18PIN
 CA卡定义: SCDATA. 数据I/O口, 输入输出, 接卡座52PIN



LVDS_FORMAT_SEL: 一般情况使用0欧接地, 软件做JEIDA/VESA选择

mini LVDS TX to TC0N connector LVDS 60HZ



5000系列使用的奇美屏: V135H3-LS2(C7)、V420H2-LS2(C7)、V460H1-LS2(C7)为固定8bit屏, 不需BIT_SEL信号;
5000系列控制信号连接关系: 屏端L/R_O ==>板端3D_SYNC_PANEL
屏端SELLVDS ==>板端LVDS_FORMAT_SEL (固定0V)
屏端2D/3D ==>板端3D_CHOICE (初始为2D状态)
屏端L/R ==>板端3DSL/RSSYNC
屏端LD_EN ==>板端BIT_SEL
屏端SCN_EN ==>板端2DSSCANSEN (固定0V)

6000系列使用的奇美屏: V390H1-LS5为固定8bit屏, 不需BIT_SEL信号;
6000系列控制信号连接关系: 屏端L/R_O ==>板端3D_SYNC_PANEL
屏端SELLVDS ==>板端LVDS_FORMAT_SEL (固定0V)
屏端2D/3D ==>板端3D_CHOICE (初始为2D状态)
屏端L/R ==>板端3DSL/RSSYNC
屏端LD_EN ==>板端BIT_SEL
屏端SCN_EN ==>板端2DSSCANSEN (固定0V)

7000系列使用的LG屏: 为固定8bit屏, 不需BIT_SEL信号;
7000系列控制信号连接关系: 屏端SELLVDS ==>板端LVDS_FORMAT_SEL (固定0V)
屏端ExtVBR-B ==>板端ExtVBR-B (初始为0V)
屏端OPC Enable ==>板端OPCSON/OFF (初始为OFF)