MXO45 / MXO45HS

METAL DIP CLOCK OSCILLATOR

FEATURES

- Standard 14 Pin or 8 Pin DIP Footprint
- HCMOS/TTL Compatible
- **Fundamental and 3RD Overtone Crystals**
- Frequency Range 1.0 – 105.561 MHz
- Frequency Stability, ±50 ppm Standard (±25 ppm and ±20 ppm available)
- +5.0Vdc Operation
- Operating Temperature to –40°C to +85°C
- Output Enable Option
- **RoHS / Green Compliant (6 / 6)**

DESCRIPTION

The MXO45/MXO45HS is a DIP packaged Clock oscillator offering reliable performance at an economical cost. The enhanced stability means it is the perfect choice for today's communications applications that require tight frequency control.

ORDERING INFORMATION

MXO □ - □ □ - M

SUPPLY VOLTAGE
45 = 14 Pin DIP/STD Output
45T = 14 Pin DIP/Tristate Output
45HS = 8 Pin DIP/STD Output
45HST = 8 Pin DIP/Tristate Output

FREQUENCY STABILITY
6 = ± 20 ppm *
5 = ± 25 ppm
3 = ± 50 ppm (standard)
2 = ±

* 6I not available.

FREQUENCY IN MHz
M - indicates MHz and decimal point. Frequency is recorded with minimum 4 significant digits to the right of the "M".

OPERATING TEMPERATURE RANGE
C = -20°C to +70°C (standard)
I = -40°C to +85°C *

Not all performance combinations and frequencies may be available.
Consult factory for availability.

Example Part Number: MXO45-3C-32M7680 or MXO45HS-3C-32M7680

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ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Absolute Maximums	Maximum Supply Voltage	V_{CC}	-	-0.5	-	7.0	V
	Storage Temperature	T_{STG}	-	-55	-	125	°C
	Frequency Range	f_O	-	1.0	-	105.561	MHz
	Frequency Stability (See Note 1 and Ordering Information)	$\Delta f/f_O$	-	-	-	20,25,50 or 100	± ppm
	Operating Temperature Commercial Industrial	T_A	-	 -20 -40	 25	 70 85	°C
Electrical and Waveform Parameters	Supply Voltage	V_{CC}	± 10 %	4.5	5.0	5.5	V
	Supply Current	I_{CC}	1.0 MHz to 20 MHz C_L=50pF 20.1 MHz to 80 MHz C_L=30pF 80.1 MHz to 105.561 MHz C_L=15pF	- - -	10 30 40	25 50 100	mA
	Output Load CMOS	C_L	 1.0 MHz to 50 MHz 50.1 MHz to 80 MHz 80.1 MHz to 105.561 MHz	 - - -	 - - -	 50 30 15	pF
	TTL		1.0 MHz to 105.561 MHz	-	-	10	TTL
	Output Voltage Levels Logic '1' Level Logic '0' Level	V_{OH} V_{OL}	 CMOS Load 10 TTL LOAD CMOS TTL Load	 0.9*V_{CC} V_{CC}-0.6V -	 - -	 - 0.1*V_{CC} 0.4	V
	Output Current Logic '1' Level Logic '0' Level	 I_{OH} I_{OL}	 V_{OH} = 3.9V V_{CC} = 4.5V V_{OL} = 0.4V V_{CC} = 4.5V	 - -	 - -	 -16 16	mA
	Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
	Rise and Fall Time	T_R, T_F	@ 10% - 90% Levels 1.0 MHz to 50 MHz C_L=50pF 50.1 MHz to 80 MHz C_L=30pF 80.1 MHz to 105.561 MHz C_L=15pF	 - - -	 8 4 2.5	 10 8 5	ns
	Start Up Time	T_S	Application of V_{CC}	-	-	10	ms
	Enable Function (See Note 2) Enable Input Voltage Disable Input Voltage	 V_{IH} V_{IL}	 Pin 1 Logic '1', Output Enabled Pin 1 Logic '0', Output Disabled	 2.0 -	 - -	 - 0.8	V
	Enable Time	T_{PLZ}	Pin 1 Logic '1'	-	-	100	ns
	Period Jitter, Pk-Pk	-	-	-	-	50	ps
	Period Jitter, RMS	-	-	-	-	5	
	Phase Jitter, RMS	-	Bandwidth 12 kHz - 20 MHz	-	-	1	

Notes:
1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and first year aging.
2. Reference CTS Application Note 014-0002-0.

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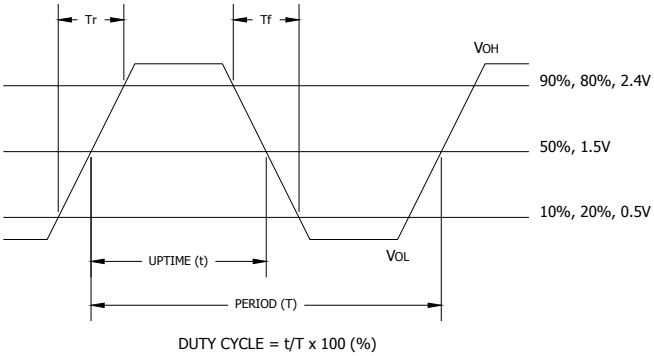
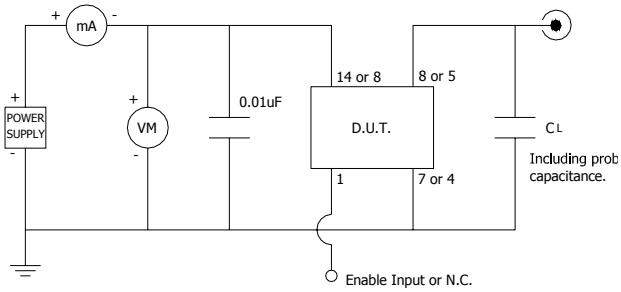
CMOS/TTL OUTPUT WAVEFORM



DUTY CYCLE = t/T x 100 (%)

TEST CIRCUIT, CMOS LOAD



ENABLE TRUTH TABLE

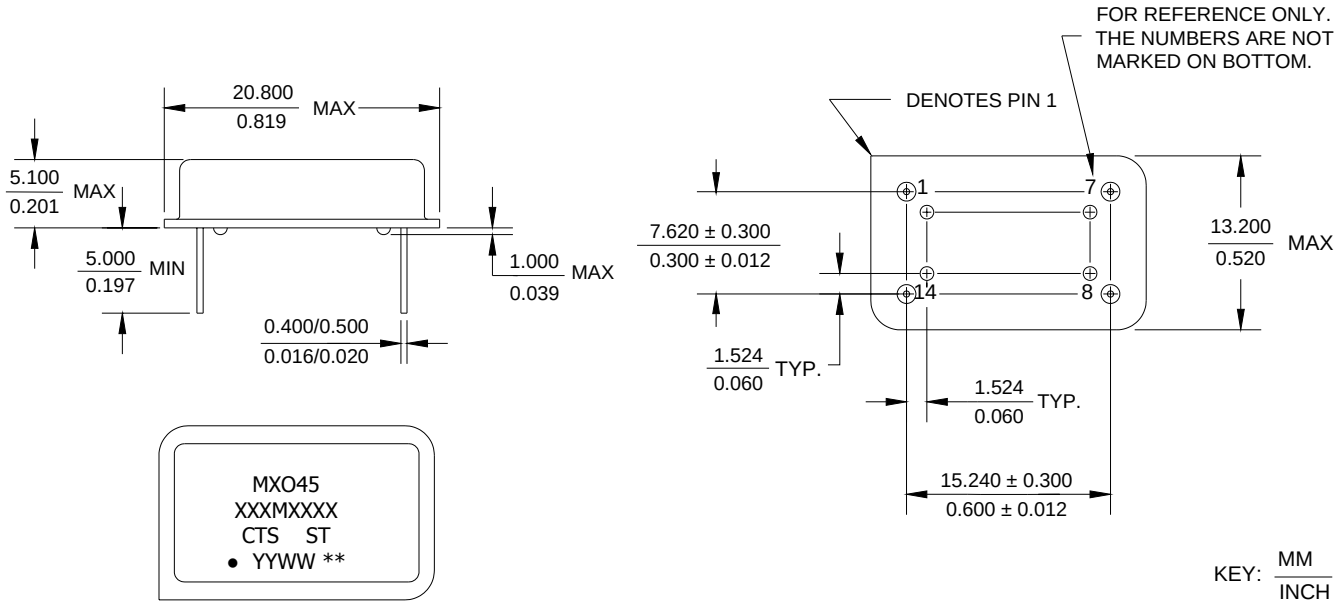
PIN 1	PIN 5 or PIN 8
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable Input or No Connect
7 or 4	GND	Circuit & Package Ground
8 or 5	Output	RF Output
14 or 8	V_{CC}	Supply Voltage

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING
DIP-14



MARKING INFORMATION

1. Model Name: MXO45 or MXO45T.
2. XXXMXXXX - Frequency marked with 4 significant digits after the 'M'.
3. ST – Frequency stability/temperature code. (Reference Ordering Information.)
4. YYWW – Date code, YY – year, WW – week.
5. ** - Manufacturing Site Code.

NOTES

1. Lead finish (e1), SnAgCu.
2. Reflow conditions per JEDEC J-STD-020.

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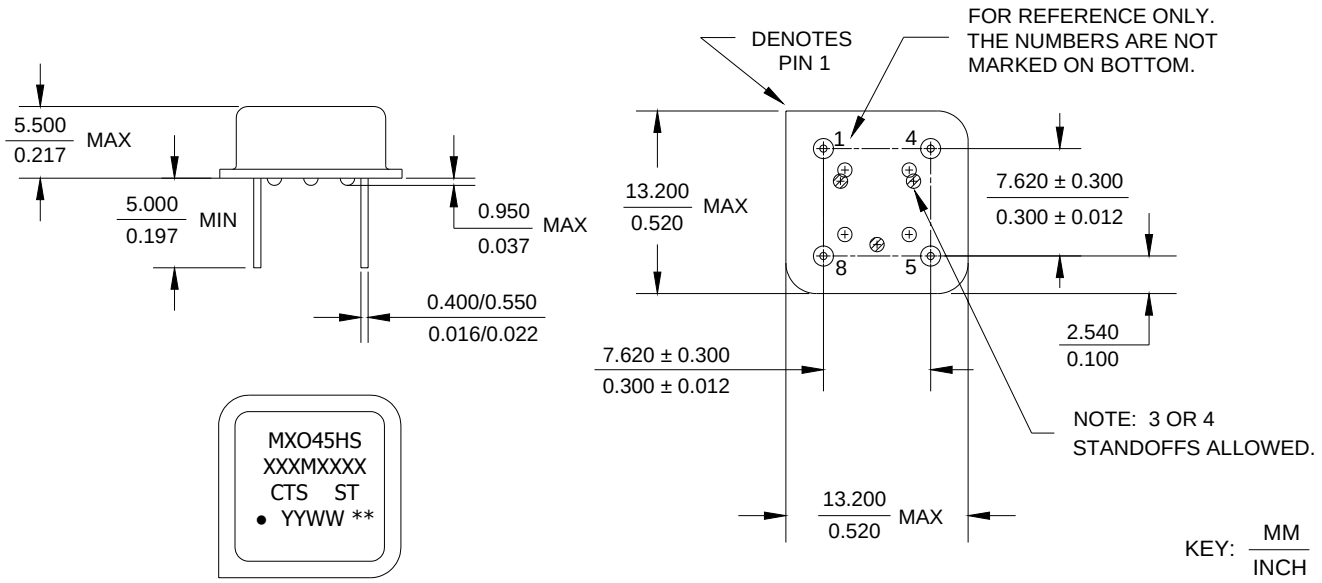
PACKAGE DRAWING
DIP-8



MARKING INFORMATION

1. Model Name: MXO45HS or MXO45HST.
2. XXXMXXXX - Frequency marked with 4 significant digits after the 'M'.
3. ST – Frequency stability/temperature code.
   (Reference Ordering Information.)
4. YYWW – Date code, YY – year, WW – week.
5. ** - Manufacturing Site Code.

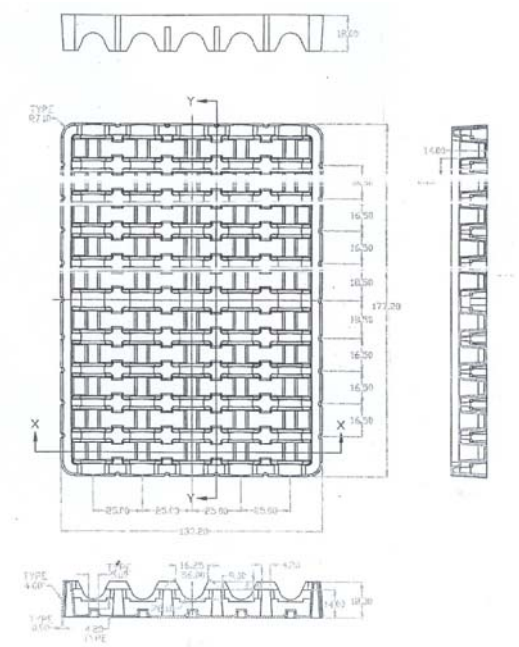
NOTES

1. Lead finish (e1), SnAgCu.
2. Reflow conditions per JEDEC J-STD-020.

PACKAGING

Product is packaged in plastic trays.
Typical packaging format is as follows:

- 50 pcs./Plastic Tray.
  Tray size is approximately 180x136x18mm (LxWxH).
- 2 Trays/Anti-Static Bag (100 pcs.)
  or
  10 Trays/Anti-Static Bag (500 pcs.).
  Bag height for 10 Trays is approximately 175mm.
- 1 Anti-Static Bag/Cardboard Carton.
- Master-pack multiple Cardboard Cartons in a larger carton.
  8 Cardboard Cartons (10 trays per carton) is approximately 460x380x400mm (LxWxH).



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ENVIRONMENTAL SPECIFICATIONS

Temperature Cycle:	400 cycles from –55°C to +125°C, 10 minute dwell at each temperature, 1 minute transfer time between temperatures.
Mechanical Shock:	1,500g's, 0.5mS duration, ½ sinewave, 3 shocks each direction along 3 mutually perpendicular planes (18 total shocks).
Sinusoidal Vibration:	0.06 inches double amplitude, 10 to 55 Hz and 20g's, 55 to 2,000 Hz, 3 cycles each in 3 mutually perpendicular planes (9 times total).
Gross Leak:	No leak shall appear while immersed in an FC40 or equivalent liquid at +125°C for 20 seconds.
Fine Leak:	Mass spectrometer leak rates less than $2x10^{-8}$ ATM cc/sec air equivalent.
Resistance to Solder Heat:	Product must survive 3 reflows of +260°C peak, 10 seconds maximum.
High Temperature Operating Bias:	2,000 hours at +125°C, maximum bias, disregarding frequency shift.
Frequency Aging:	1,000 hours at +85°C, full bias, less than ±5 ppm shift.
Moisture Sensitivity Level:	Level 1 per JEDEC J-STD-020.

QUALITY AND RELIABILITY

Quality systems meet or exceed the requirements of ISO 9000:2000 standards.

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