

NS9210/NS9215

32-bit NET+ARM Processor Family

Cost-efficient, small footprint ARM926EJ-S processor with integrated encryption and unique interface flexibility.



Overview

The NS9210/NS9215 processor family offers a cost-efficient, small-footprint 32-bit ARM9 solution that combines high performance, integrated Ethernet networking, strong security, and unique interface flexibility. It is the ideal choice for a broad range of applications such as security/access control, medical, industrial/building automation, transportation and remote monitoring.

Two independent Flexible Interface Modules (FIMs) with 300 MHz DRP1655X processor cores provide a growing list of application-specific peripheral interface options. The NIST-compliant 256-bit hardware AES accelerator combines state-of-the-art data privacy services with superior performance, and Digi's patented dynamic power management addresses the needs of today's power budget-conscious designs.

The complete and easy-to-use development kits for NET+OS[®] are based on the field-proven ThreadX[®] Real-Time Operating System and deliver a true and IPv6-ready turnkey embedded development solution with the Eclipse-based Digi ESP[™] IDE.

Platforms and Services



Design Services



Accessory Kits

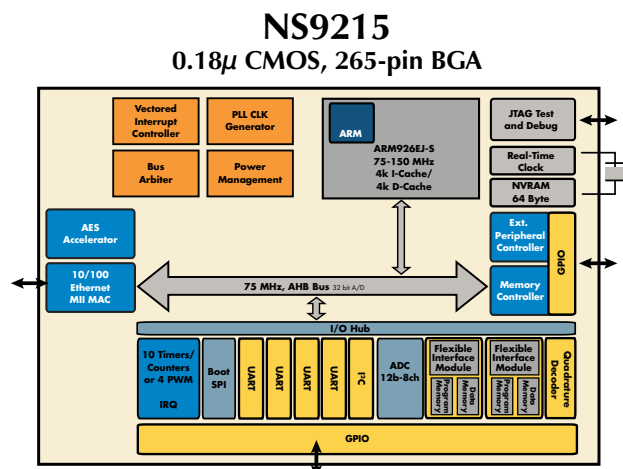


Support

NET + OS

Supported Software Platforms

Block Diagram



Features/Benefits

- High-performance 150 MHz ARM926EJ-S core
- 10/100 Mbit Ethernet MAC integration
- On-chip hardware AES accelerator
- Software-configurable I/O flexibility through FIMs
- Power management modes with dynamic clock scaling
- Rich set of integrated peripheral interfaces
- Complete and royalty-free NET+OS development platform for network-enabled embedded devices
- Upgrade path to ARM9 core performance for existing NS7520 designs through pin-compatible NS9210



Development Kits

Development Kit Overview

Development Kit for NET+OS®



NET+OS is a royalty-free turnkey solution for embedded software development based on the ThreadX Real-Time Operating System (RTOS), which is one of the most reliable and field-proven RTOS solutions available. In addition to ThreadX, NET+OS provides a complete set of integrated building blocks needed to create product solutions with leading network security using Digi embedded microprocessors and modules.

For professional embedded software development, the Eclipse based Digi ESP™ Integrated Development Environment (IDE) for Microsoft Windows with graphical user interface and a high-speed USB 2.0 hardware debugger is provided out-of-the-box. A Green Hills MULTI IDE option is also available.

Digi professional design and support services are also part of the development kit. The included professional design review service improves time-to-market by minimizing the traditional design risk for prototyping and production units. In addition, one year of premium support service covers any software development related questions through the assistance of Digi's technical support experts.

- Royalty-free turn-key solution for embedded development
- Built on field-proven and compact ThreadX RTOS
- Fully integrated support for secure, IPv4/IPv6 networking applications
- Eclipse-based Digi ESP IDE for Windows software development
- Professional hardware design review included

Development Kit Contents

| | NS9210 | NS9215 |
|---------------------------------------|--|--|
| Processor Module | NS9210 processor module with 150 MHz, 4 MB Flash, 8 MB SDRAM | NS9215 processor module with 150 MHz, 4 MB Flash, 8 MB SDRAM |
| Development Board | Ethernet connector, 4 serial ports (1 x RS-232/422/485, 1 x RS-232, 2 x TTL), User/Application connectors, I ² C/SPI headers, ADC header, Screw terminal for access to 8 GPIO signals, 2 user push-buttons, 2 user LEDs, Wake-up button, Reset button, 802.3af PoE module connector, Prototyping area, Battery backup, 9-30VDC power supply, Power switch, Mounting holes | |
| CD/DVD | Digi NET+OS CD: NET+OS 7, Digi ESP IDE, BSP source code, Sample code, Green Hills MULTI support option, User documentation | |
| Documentation | Quick start guide, Digi ESP tutorial, NET+OS programmer's guide, NET+OS API documentation, Advanced Web Server, Hardware reference manual, Complete design schematics and bill of material | |
| Power Supplies and Accessories | External wall power supply (110/240VAC) with interchangeable outlet adapters (North America, EU, UK and Australia), Ethernet cable, Serial cable | |
| Other | Digi JTAG Link USB 2.0 hardware debugger, 802.3af PoE module, Professional Hardware Design Review, 1 year of Premium Support Service | |
| Kit Part Numbers | NS-9210-NET | NS-9215-NET |

Please refer to the feature specs on our website for detailed information about the NET+OS software platform capabilities.

| Platform | | | NS9210 | NS9215 |
|--|---|--|---|--------|
| General | | | | |
| Processor | ARM926EJ-S | | | |
| Speed Grades | 75/150 MHz | | | |
| Cache | 4 KB I-cache / 4 KB D-cache | | | |
| Process | 0.18μ CMOS | | | |
| 32-bit ARMv5TEJ Instruction Set | • | | | |
| 16-bit Thumb Instruction Set | • | | | |
| MMU | • | | | |
| DSP Instruction Extensions | • (Improved divide, Single cycle multiply accumulate) | | | |
| ARM Jazelle® Java Accelerator | • | | | |
| Embedded ICE-RT Debug Unit | • | | | |
| JTAG Boundary Scan, BSDL | • | | | |
| Power Management Modes | • | | | |
| AES Accelerator | | | | |
| Key Length | 128-, 192-, 256-bit | | | |
| Cipher Modes | ECB, CBC, OFB, CTR, CCM | | | |
| Hardware Key Expander | • | | | |
| DMA-Enabled | • | | | |
| NIST-Compliant | • | | | |
| FIM (Flexible Interface Module) | | | | |
| FIMs | 1/2; Availability depending on application-specific use of external 16-/32-bit memory bus | | 2 | |
| Cores | 8-bit DRP1C1655X | | | |
| Speed | Up to 300 MHz (4x bus speed) | | | |
| Data Memory (SRAM) | 192 Bytes | | | |
| Program Memory (SRAM) | 2 KB | | | |
| Interface Options | SD/SDIO, UART, 1-Wire, CAN, USB device (low-speed), Other; Please contact us for custom interface implementation options. | | | |
| Power Management | | | | |
| Dynamic Clock Scaling (patent pending) | Full, /2, /4, /8, /16 speeds, with hardware clock scale control (wake-up events) | | | |
| Low-Power Sleep Modes | • | | | |
| Configurable Wake-Up Conditions | External IRQ, I²C, SPI, UART, Ethernet | | External IRQ, I²C, SPI, UART, Ethernet, RTC | |
| Disabling of Unused System Modules | • | | | |
| Memory Controller | | | | |
| Glue-less Interface | • (SDRAM, SRAM, Buffered DIMM, EEPROM, Flash) | | | |
| Self-Refresh (Sleep Mode) | • | | | |
| Dynamic/Static Memory Chip Selects | Selection of 5 | | 4/4 | |
| Wait States Per Memory Chip Select | 0-32 | | | |
| Static Memory Controller Extended Waits (EW) | Up to 16,368 | | | |
| Automatic Dynamic Bus Sizing | • | | | |
| Burst Support | 8-transfer, with automatic data width adjustment | | | |
| External DMA Channels | 2 | | | |

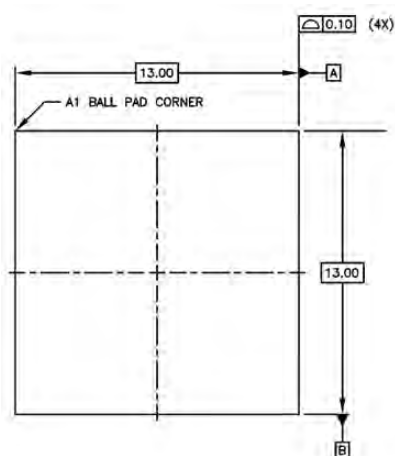
| Platform | | NS9210 | | NS9215 | |
|--|---|--------|---------------------|--------|--|
| System Bus DMA | | | | | |
| High-Speed Rotating AHB arbiter | 16 channels | | | | |
| Deterministic Bus Bandwidth Allocation | • | | | | |
| Multiple Bus Masters | Ethernet Tx/Rx, I/O Hub, Ext DMA, ARM core | | | | |
| External DMA | | | | | |
| Independent DMA Channels | 2 | | | | |
| Transfer Modes | External peripherals, External memory, AHB peripherals | | | | |
| AES DMA Support | • | | | | |
| AHB Master | • | | | | |
| I/O Hub | | | | | |
| Low Latency | • | | | | |
| DMA | 8 channels | | | | |
| DMA or Direct Access Mode | UART, SPI, FIM | | UART, SPI, ADC, FIM | | |
| Direct Access Mode Only | I²C | | I²C, RTC | | |
| AHB Master | • | | | | |
| External Interrupts | | | | | |
| External Programmable Interrupts | 4 | | | | |
| Advanced Vectored Interrupt Controller | | | | | |
| Two-Tier Priority | • (FIRQ/IRQ) | | | | |
| Low-Latency FIRQ | • | | | | |
| Interrupt Sources | 32 | | | | |
| Ethernet MAC | | | | | |
| Data Rates | 10 / 100 Mbit/s | | | | |
| Duplex | Full and Half | | | | |
| PHY Interface | MII | | | | |
| Address Filtering | Station, Broadcast, Multicast | | | | |
| FIFO | 2 KB Rx / 256 Bytes Tx | | | | |
| Separate Tx and Rx DMA Channels | • | | | | |
| Programmable 8-Entry Restrictive Multicast Filtering | • | | | | |
| Access Modes | Interrupt and DMA | | | | |
| AHB Master | • | | | | |
| UART | | | | | |
| Ports | 2 / 4; Availability depending on application-specific use of external 16-/32-bit memory bus | | | 4 | |
| Bit Rates | Up to 1.8432 Mbps | | | | |
| Data Format | 5 to 8 data bits; Odd, Even, or No parity; 1 or 2 stop bits; MSB or LSB first | | | | |
| Channel Modes | Normal, Local loopback, Remote loopback | | | | |
| Modem Control Signals | RTS, CTS, DTR, DSR, DCD, RI | | | | |
| Maskable Interrupt Conditions | Receiver idle; Transmitter idle; Receive error conditions; Character gap timeout; Character match events; State change detection: CTS, DSR, DCD, RI | | | | |
| FIFO | 2 KB Rx / 256 Bytes Tx | | | | |
| Transmit FIFO Bypass | • | | | | |

| Platform | | NS9210 | NS9215 |
|--|---|------------------|--------|
| I ² C v1.0 | | | |
| Master/Slave | • | | |
| Bit Rates | 100 kbit/s and 400 kbit/s modes | | |
| Address Modes | 7-bit, 10-bit | | |
| Bus Arbitration | • | | |
| SPI (with Boot) | | | |
| Master/Slave | • | | |
| Bit Rates | 33 Mps (Master) / 7.5 Mbps (Slave) max | | |
| SPI Modes | 0, 1, 2, 3 | | |
| Maskable Interrupt Conditions | • | | |
| Boot Support | Serial EEPROM, High-speed ROM/flash | | |
| Patent Pending Serial Boot Circuit | Automatic configuration, Internal register setup, Boot code transfer to external memory | | |
| POR | | | |
| 3.3V Voltage Monitoring | - | • | |
| Early Power-Loss Comparator with Alert for Main Power Shutdown | - | • | |
| Auxiliary Analog Comparator | - | 2.4V trip point | |
| ADC | | | |
| Resolution/Conversion | - | 12 bit/1 MHz | |
| Multiplexed Inputs | - | Single-ended 8:1 | |
| Rail-to-Rail Input Range | - | • | |
| 12-Bit Output | - | DMA/Direct | |
| External Reference | - | • | |
| Timers/Counters/PWM | | | |
| General Purpose Timers/Counters | 10 (32-bit) | | |
| PWM | Up to 4 with basic or enhanced functionality | | |
| Quadrature Decoder | • | | |
| Software Watchdog Timer | IRQ, FIQ, RESET | | |
| GPIO | | | |
| Multiplexed GPIOs | Up to 54 | Up to 108 | |
| Real-Time Clock | | | |
| Alarm Masks and Event Detection | - | • | |
| Calendar | - | 1900-2999 | |
| Resolution | - | 10 ms | |
| Integrated NVRAM | - | 64 Bytes | |
| External Battery Backup | - | • | |
| External Clock Source | - | • | |
| Operating Voltage | | | |
| Core | 1.8V | | |
| I/O Ring | 3.3V | | |
| 5V-Tolerant GPIO and Memory Inputs | • | | |

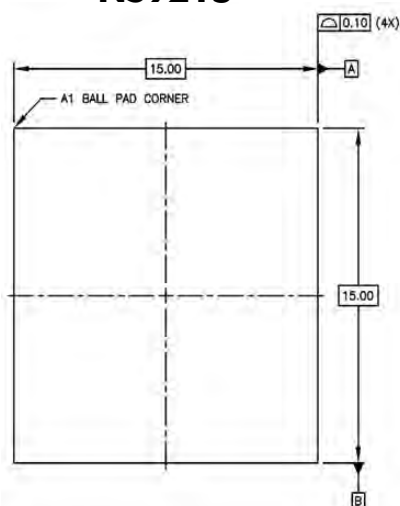
| Platform | | NS9210 | NS9215 |
|-------------------------------|--|---------------------------|-------------|
| Operating Temperature | | | |
| 75/150 MHz | -40° C to +85° C | | |
| Power Dissipation | | | |
| 150 MHz Core/75 MHz Bus | 1.019 W | | |
| 75 MHz Core/75 MHz Bus | 0.828 W | | |
| 112 MHz Core/56 MHz Bus | 0.638 W | | |
| 56 MHz Core/56 MHz Bus | 0.499 W | | |
| Sleep Mode, Wake on Ethernet | 0.073 W | | |
| Sleep Mode, Wake on Ext IRQ | 0.055 W | | |
| Main Power Down, Battery Draw | - | 3.0V – 32 µA; 1.8V – 6 µA | |
| Package | | | |
| Type | 177-pin BGA (Pin-compatible with NS7520) | | 265-pin BGA |
| Ball Pitch | 0.8 mm | | |
| Size | 13 x 13 mm | | 15 x 15 mm |
| Lead-Free, RoHS Compliant | • | | |

- Chip Feature

NS9210



NS9215



You can purchase with confidence knowing that Digi is always available to serve you with expert technical support and our industry leading warranty. For detailed information visit www.digi.com/support

91001450
B3/1209

Digi International
Worldwide HQ
877-912-3444
952-912-3444
www.digi.com

Digi International
France
+33-1-55-61-98-98
www.digi.fr

Digi International
Japan
+81-3-5428-0261
www.digi-intl.co.jp

Digi International
Singapore
+65-6213-5380

Digi International
China
+86-21-50492199
www.digi.com.cn



www.digi.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Digi International:

[NS9210B-0-I150](#) [NS9210B-0-I75](#) [NS9215B-0-I150](#) [NS9215B-0-I75](#) [NS-9210-NET](#)