

P2 Series

P2010 and P2020 single- and dual-core communications processors

Freescal QorIQ™ communications platforms are the next-generation evolution of our leading PowerQUICC® communications processors. Built using high-performance Power Architecture® cores, Freescale QorIQ platforms enable a new era of networking innovation where the reliability, security and quality of service for every connection matters.

QorIQ P2020 and P2010 Communications Processors

The QorIQ P2 platform series, which includes the P2020 (dual-core processor) and P2010 (single-core processor) communications processors, delivers high single-threaded performance per watt for a wide variety of applications in the networking, telecom, military and industrial markets. The series delivers dual- and single-core frequencies up to 1.2 GHz on a 45 nm technology low-power platform.

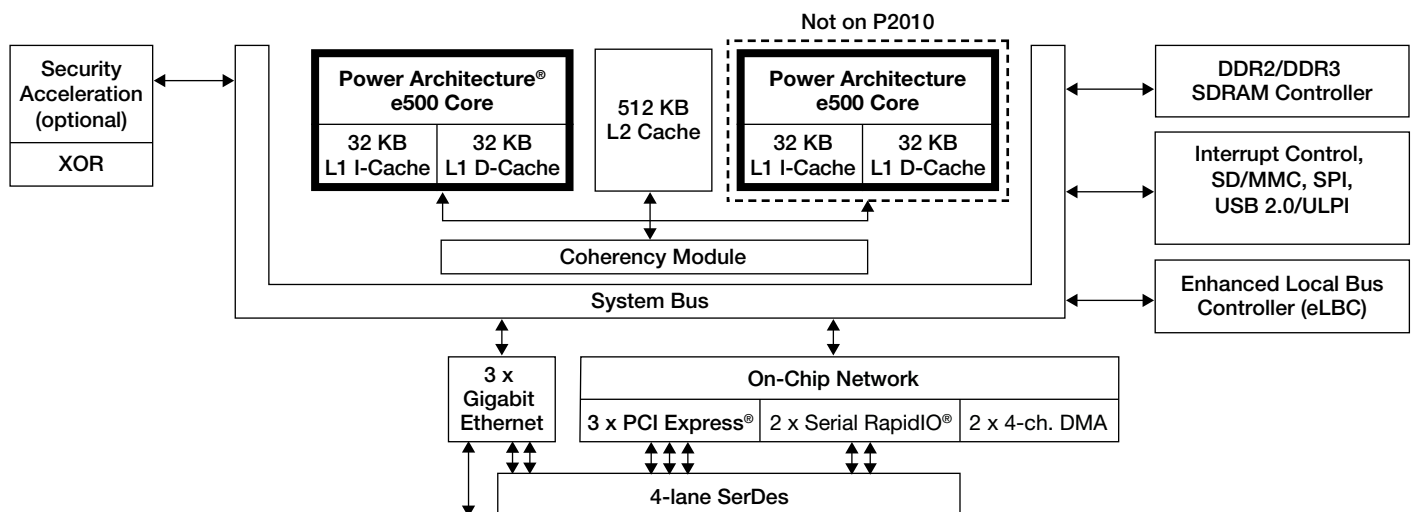
The QorIQ P2020 and P2010 dual- and single-core products are pin-compatible with the QorIQ P1 platform products, offering four interchangeable cost-effective solutions. Scaling from a single-core processor at 533 MHz (P1011) to a dual-core processor at 1.2 GHz (P2020), the two QorIQ platforms together deliver an impressive 4.5x aggregate frequency range within the same pinout.

The devices in these two series are software-compatible, sharing the e500 Power Architecture core and peripherals, as well as being fully software compatible with the existing PowerQUICC processors. This enables customers to create a product with multiple performance points from a single board design. The P2020 and P1020 dual-core processors support symmetric and asymmetric multi-processing, enabling customers to scale performance through either thread-level or application-level parallelism.

The P2020 and P2010 communications processors both have an advanced set of features for ease of use. The optional integrated security engine supports the cryptographic algorithms commonly used in IPsec, SSL, 3GPP and other networking and wireless security protocols. The 64-bit memory controller offers future-proofing against memory technology migration with support for both DDR2 and DDR3. It also supports error correction codes, a baseline requirement for any high-reliability system. Other memory types such as flash are supported through the 16-bit local bus, USB, SD/MMC and SPI.

The P2010 and P2020 processors integrate a rich set of interfaces, including SerDes, Gigabit Ethernet, PCI Express®, RapidIO® technology and USB. The three 10/100/1000 Ethernet ports support advanced packet parsing, flow control and quality of service features, as well as IEEE® 1588 time stamping.

QorIQ™ P2020 and 2010 Block Diagram



■ Cores

Target Applications

The P2010 and P2020 processors serve in a wide range of applications, especially those that have tight thermal constraints. With an available junction temperature range of -40°C to +125°C, the devices can be used in power-sensitive defense, aerospace and industrial applications, and less-protected outdoor environments. They enable various combinations of data plane and control plane workloads in networking and telecom applications that require higher performance but want to avoid the complexity of partitioning the application across many cores. The devices' primary target applications are networking and telecom linecards. The P2 devices, with their low power budget and high single-threaded performance, are uniquely well-suited for control plane applications. Control plane applications tend to be more sequential in nature and thus lose scaling efficiency with increasing number of threads or cores. The P2 series, with its low power, efficient dual-issue out-of-order e500 core, Power Architecture technology, and high 1.2 GHz frequency, offers a level of single-threaded performance that is a perfect fit for control plane applications.

The networking linecard requires an optimal combination of good performance to manage a large amount of control plane traffic balanced against low power and cost. With convenient I/O, flexible core configurations and an on-board security block, the P2010 and P2020 processors are well-suited for this application, which involves controlling ASICs, managing exceptions and routing table maintenance.

The P2010 and P2020 processors are also well-suited for Long Term Evolution (LTE) and WiMAX channel card applications. With dual-core performance in single-core power budgets, the P2 series facilitates the "flattening" of the wireless network hierarchy. The dual Serial RapidIO interfaces allow direct connection to the DSPs (such as Freescale's MSC8156 DSP) that implement Layer 1 processing as well as redundant backplane connections.

Technical Specifications

- Dual (P2020) or single (P2010) high-performance Power Architecture e500 cores
 - 36-bit physical addressing
 - Double-precision floating-point support
 - 32 KB L1 instruction cache and 32 KB L1 data cache for each core
 - 800 MHz to 1.2 GHz clock frequency
- 512 KB L2 cache with ECC. Also configurable as SRAM and stashing memory.
- Three 10/100/1000 Mbps enhanced three-speed Ethernet controllers (eTSECs)
 - TCP/IP acceleration and classification capabilities
 - IEEE 1588 support
 - Lossless flow control
 - R/G/MII, R/TBI, SGMII
 - FIFO interfaces
- High-speed interfaces supporting various multiplexing options
 - Four SerDes to 3.125 GHz multiplexed across controllers
 - Three PCI Express interfaces
 - Two Serial RapidIO interfaces
 - Two SGMII interfaces
- High-Speed USB controller (USB 2.0)
 - Host and device support
 - Enhanced host controller interface (EHCI)
 - ULPI interface to PHY
- Enhanced secure digital host controller (SD/MMC)
- Serial peripheral interface
- Integrated security engine (SEC 3.1) (optional)
 - Crypto algorithm support includes 3DES, AES, RSA/ECC, MD5/SHA, ARC4, Kasumi, Snow 3G and FIPS deterministic RNG
 - Single pass encryption/message authentication for common security protocols (IPsec, SSL, SRTP, WiMAX)
 - XOR acceleration
- 64-bit DDR2/DDR3 SDRAM memory controller with ECC support
- Programmable interrupt controller (PIC) compliant with OpenPIC standard
- Two four-channel DMA controllers
- Two I²C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- 16 general-purpose I/O signals
- Package: 689-pin wirebond power-BGA (TEPBGA2)

QorIQ™ Platform	Device	Cores	Top Core Frequency	L2 Size	DDR 2/3 Support	GE Ports	SerDes	PCI Express®	Serial RapidIO®	TDM
P1	P1011	1	800 MHz	256 KB	32-bit with ECC	3	4	2	N/A	Yes
P1	P1020	2	800 MHz	256 KB	32-bit with ECC	3	4	2	N/A	Yes
P2	P2010	1	1200 MHz	512 KB	64-bit with ECC	3	4	3	2	N/A
P2	P2020	2	1200 MHz	512 KB	64-bit with ECC	3	4	3	2	N/A

Learn More:

For current information about Freescale products and documentation, please visit www.freescale.com/QorIQ.



Freescale, QorIQ, CoreNet and the Freescale logo are trademarks or registered trademarks of Freescale Semiconductor, Inc. in the U.S. and other countries. All other product or service names are the property of their respective owners. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. © Freescale Semiconductor, Inc. 2009.

Document Number: QP20XXFS
REV 3

