

# TQP3M9009

## High Linearity LNA Gain Block



### Applications

- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / EDGE / CDMA
- General Purpose Wireless

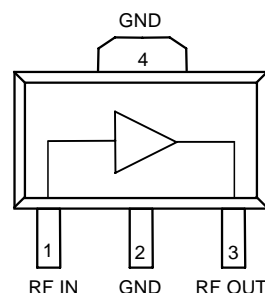


3-pin SOT-89 Package

### Product Features

- 50-4000 MHz
- 21.8 dB Gain @ 1.9 GHz
- +39.5 dBm Output IP3
- 1.3 dB Noise Figure @ 1.9 GHz
- 50 Ohm Cascadable Gain Block
- Unconditionally stable
- High input power capability
- +5V Single Supply, 125 mA Current
- SOT-89 Package

### Functional Block Diagram



### General Description

The TQP3M9009 is a cascadable, high linearity gain block amplifier in a low-cost surface-mount package. At 1.9 GHz, the amplifier is targeted to provide 21.8 dB gain, +39.5 dBm OIP3, and 1.3 dB Noise Figure while only drawing 125 mA current. The device is housed in a leadfree/green/RoHS-compliant industry-standard SOT-89 package using a NiPdAu plating to eliminate the possibility of tin whiskering.

The TQP3M9009 has the benefit of having high gain across a broad range of frequencies while also providing very low noise. This allows the device to be used in both receiver and transmitter chains for high performance systems. The amplifier is internally matched using a high performance E-pHEMT process and only requires an external RF choke and blocking/bypass capacitors for operation from a single +5V supply. The internal active bias circuit also enables stable operation over bias and temperature variations.

The TQP3M9009 covers the 0.05-4 GHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.

### Pin Configuration

Pin #	Symbol
1	RF Input
3	RF Output / Vcc
2, 4	Ground

### Ordering Information

Part No.	Description
TQP3M9009	High Linearity LNA Gain Block
TQP3M9009-PCB IF	TQP3M9009 EVB 0.05-0.5 GHz
TQP3M9009-PCB RF	TQP3M9009 EVB 0.5-4 GHz

Standard T/R size = 1000 pieces on a 7" reel.

### Specifications

#### Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150 °C
RF Input Power, CW, 50 Ω, T = 25°C	+23 dBm
Device Voltage, V <sub>dd</sub>	+7 V
Reverse Device Voltage	-0.3 V
Thermal Resistance (junction to case)	34 °C/W
Junction Temperature, T <sub>j</sub> For 10 <sup>6</sup> hours MTTF	190 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

#### Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V <sub>dd</sub>	+4.75	+5	+5.25	V
T(case)	-40		85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

#### Electrical Specifications

Test conditions unless otherwise noted: +25°C, +5V Vsupply, 50 Ω system.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		50		4000	MHz
Test Frequency			1900		MHz
Gain			21.8		dB
Input Return Loss			13		dB
Output Return Loss			14		dB
Output P1dB			+22		dBm
Output IP3	See Note 1.		+39.5		dBm
Noise Figure			1.3		dB
V <sub>dd</sub>			+5		V
Current, I <sub>dd</sub>			125		mA

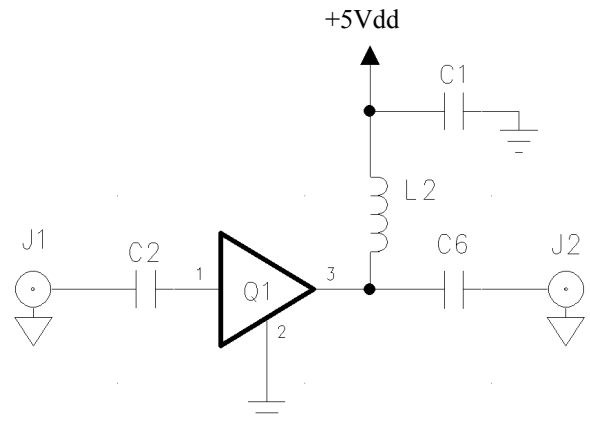
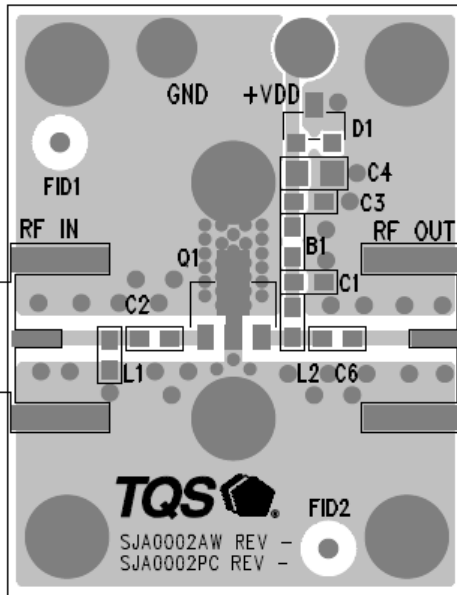
#### Notes

- OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.

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## Application Circuit Configuration



### Notes:

1. See PC Board Layout, page 8 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. B1 (0  $\Omega$  jumper) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.

## Bill of Material

Reference Designation	Frequency (MHz)	
	TQP3M9009-PCB_IF	TQP3M9009-PCB_RF
	50 - 500	500 - 4000
Q1	TQP3M9009	
C2, C6	1000 pF	100 pF
C1	0.01 uF	0.01 uF
L2	330 nH	68 nH
L1, D1, C3, C4	Do Not Place	
B1	0 $\Omega$	

### Notes:

1. Performances can be optimized at frequency of interest by using recommended component values shown in the table below.

Reference Designation	Frequency (MHz)			
	500	2000	2500	3500
C2, C6	100 pF	22 pF	22 pF	22 pF
L2	82 nH	22 nH	18 nH	15 nH

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### Typical Performance 500-4000 MHz

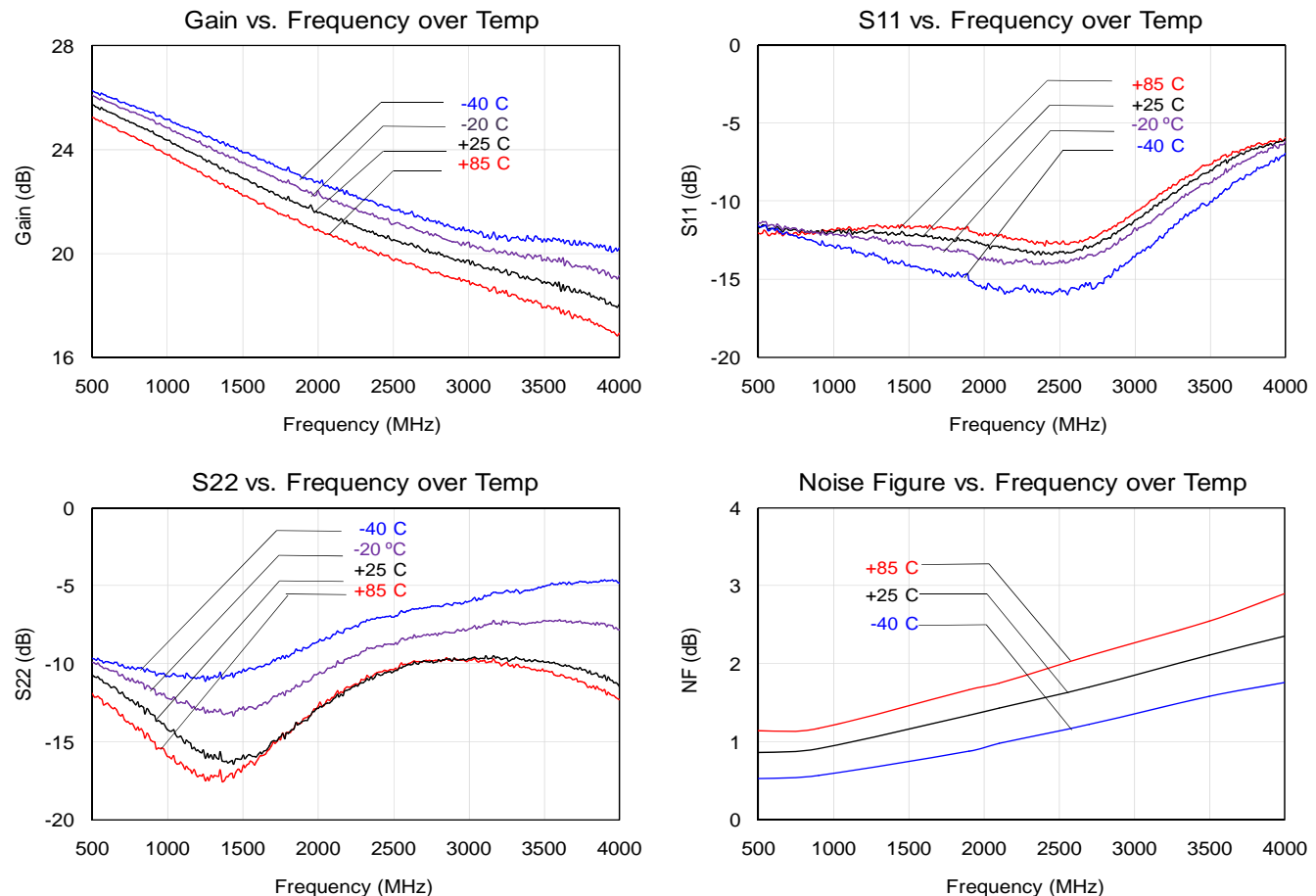
Test conditions unless otherwise noted: +25°C, +5V, 125 mA, 50  $\Omega$  system. The data shown below is measured on TQP3M9009-PCB\_RF.

Frequency	MHz	500	900	1900	2700	3500	4000
Gain	dB	25.5	24.7	21.8	20	18.9	17.9
Input Return Loss	dB	11.5	12	13	13	8	6
Output Return Loss	dB	10.8	13	14	10	10	11.3
Output P1dB	dBm	+22.5	+21.8	+22	+21.6	+21.8	+20.7
OIP3 [1]	dBm	+41.4	+40.5	+39.5	+39	+37.9	+35.8
Noise Figure [2]	dB	0.9	0.9	1.3	1.7	2.1	2.4

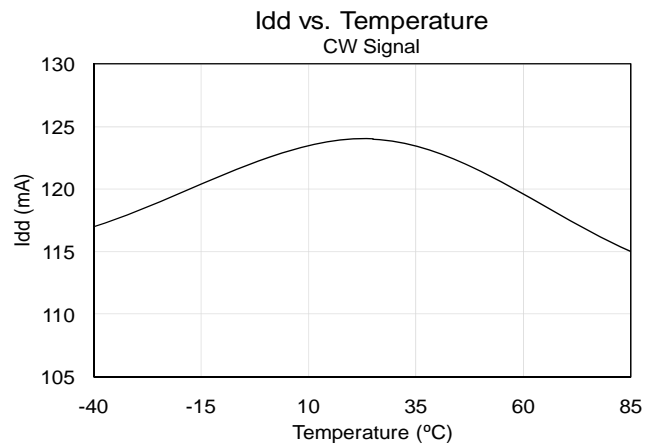
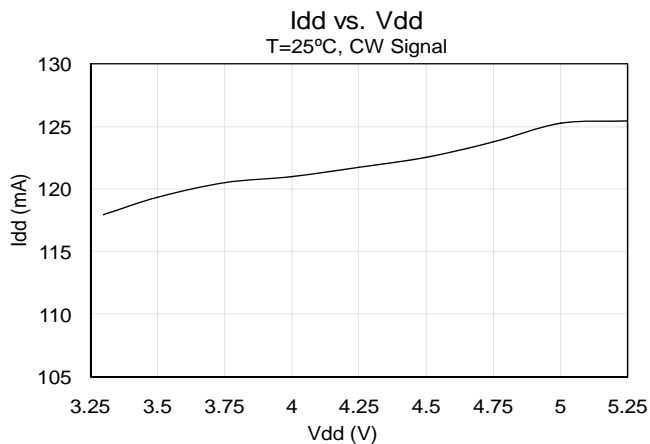
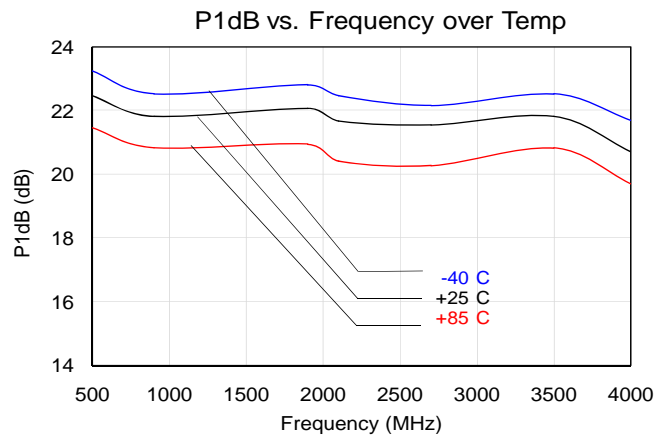
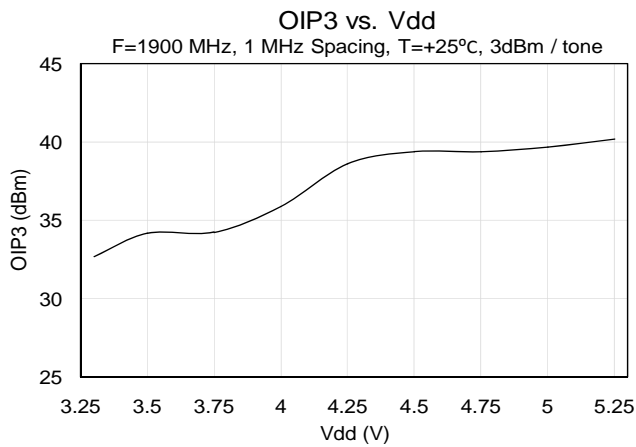
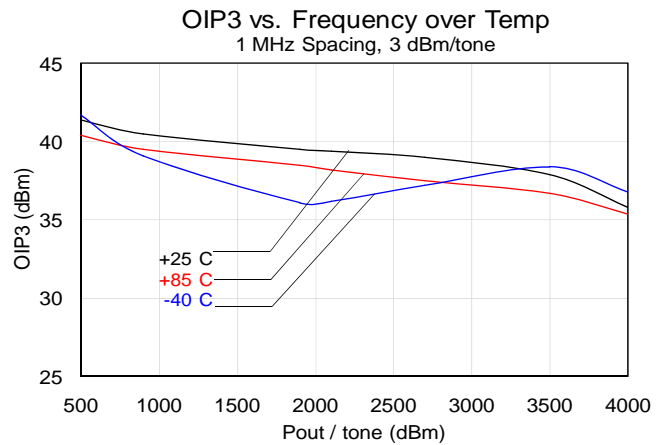
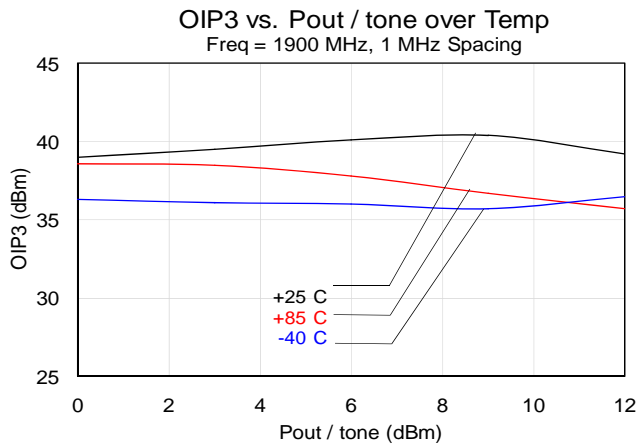
Notes:

- OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
- Noise figure data shown in the table above is measured on evaluation board which includes board losses of around 0.1 dB @ 2 GHz.

### RF Performance Plots



### RF Performance Plots



# TQP3M9009

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### Typical Performance 50-500 MHz

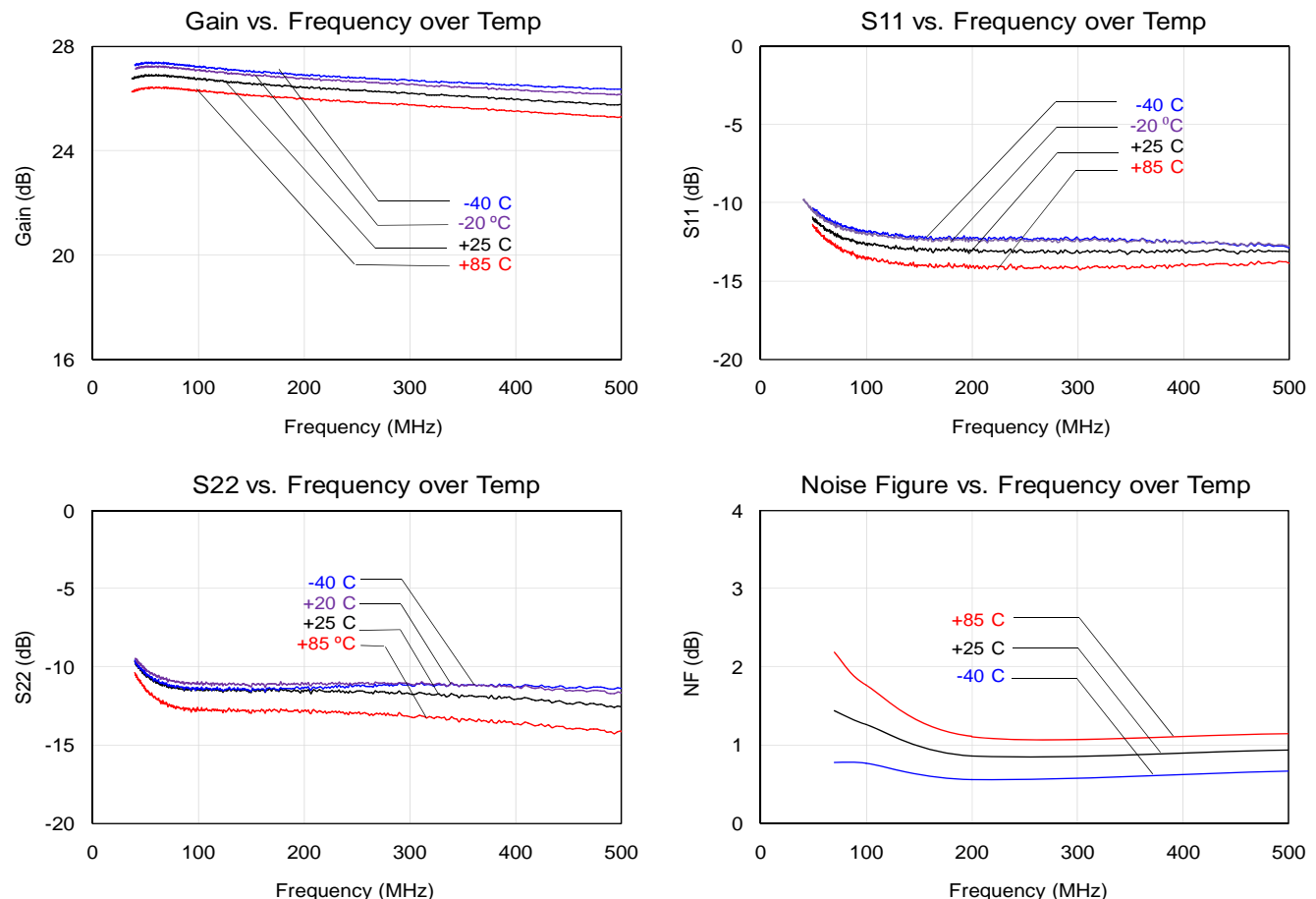
Test conditions unless otherwise noted: +25°C, +5V, 125 mA, 50  $\Omega$  system. The data shown below is measured on TQP3M9009-PCB\_IF.

Frequency	MHz	70	100	200	500
Gain	dB	27	26.8	26.4	25.8
Input Return Loss	dB	12	13	13	13
Output Return Loss	dB	11	12	12	13
Output P1dB	dBm	+21.6	+21.9	+21.9	+22.2
OIP3 [1]	dBm	+37.6	+38.8	+39	+41.4
Noise Figure [2]	dB	1.4	1.3	0.9	0.9

Notes:

- OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
- Noise figure data shown in the table above is measured on evaluation board which includes board losses of around 0.1 dB @ 2 GHz.

### IF Performance Plots

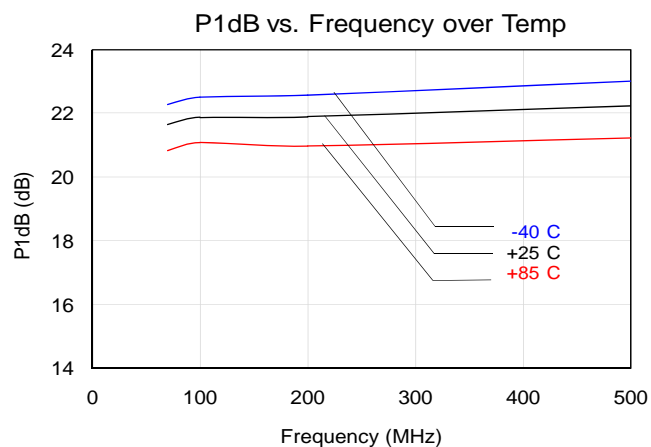
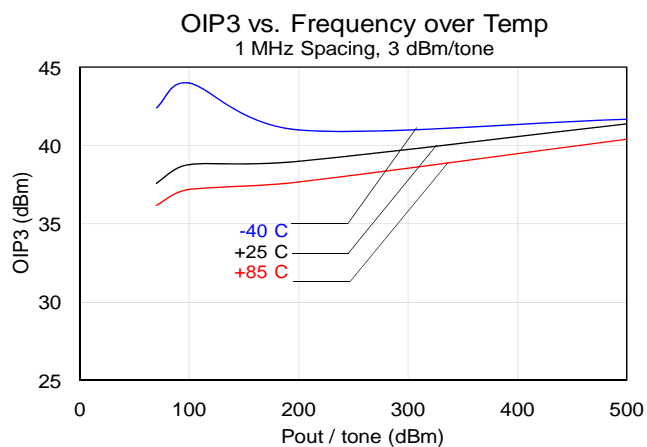


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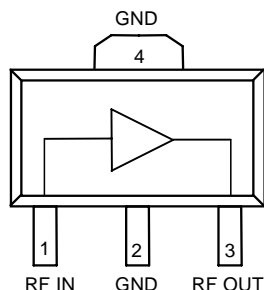
## High Linearity LNA Gain Block



### IF Performance Plots



### Pin Configuration and Description



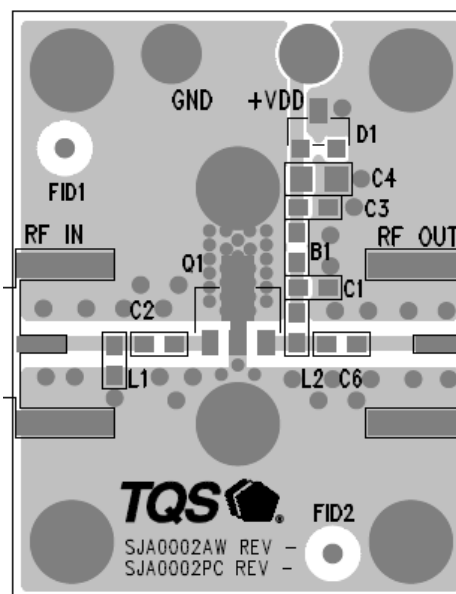
Pin	Symbol	Description
1	RF IN	Input, matched to 50 ohms, External DC block is required.
2, 4	GND	Needed for RF and the thermal path
3	RFout / Vdd	Output, matched to 50 ohms, External DC Block is required and supply voltage

### Applications Information

#### PC Board Layout

Top RF layer is .014" NELCO N4000-13,  $\epsilon_r = 3.9$ , 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. 50 ohm Microstrip line details: width = .029", spacing = .035".

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from supplier to supplier, careful process development is recommended.







### Product Compliance Information

#### ESD Information



#### Caution! ESD-Sensitive Device

ESD Rating: Class 1A  
Value: Passes  $\geq 250$  V to  $< 500$  V.  
Test: Human Body Model (HBM)  
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV  
Value: Passes  $\geq 1000$  V  
Test: Charged Device Model (CDM)  
Standard: JEDEC Standard JESD22-C101

#### MSL Rating

Level 3 at  $+260$  °C convection reflow  
The part is rated Moisture Sensitivity Level 3 at  $260^{\circ}\text{C}$  per  
JEDEC standard IPC/JEDEC J-STD-020.

#### Solderability

Compatible with the latest version of J-STD-020, Lead free solder,  $260^{\circ}$

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ( $\text{C}_{15}\text{H}_{12}\text{Br}_4\text{O}_2$ ) Free
- PFOS Free
- SVHC Free

### Contact Information

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