



# PBSM5240PFH

40 V, 2 A PNP low  $V_{CEsat}$  (BISS) transistor with N-channel Trench MOSFET

Rev. 1 — 20 June 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Combination of PNP low  $V_{CEsat}$  Breakthrough In Small Signal (BISS) transistor and N-channel Trench Metal-Oxide Semiconductor Field- Effect Transistor (MOSFET). The device is housed in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package.

### 1.2 Features and benefits

- Very low collector-emitter saturation voltage  $V_{CEsat}$
- High collector current capability  $I_C$  and  $I_{CM}$
- High energy efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

### 1.3 Applications

- Load switch
- Power management
- Power switches (e.g. motors, fans)
- Battery-driven devices
- Charging circuits

### 1.4 Quick reference data

Table 1. Quick reference data

| Symbol  | Parameter                               | Conditions                         | Min    | Typ | Max  | Unit      |
|---|---|------------------------------------|--------|-----|------|-----------|
| <b>PNP low <math>V_{CEsat}</math> (BISS) transistor</b> |   |                                    |        |     |      |           |
| $V_{CEO}$   | collector-emitter voltage               | open base                          | -      | -   | -40  | V         |
| $I_C$   | collector current                       |                                    | [1]    | -   | -1.8 | A         |
| $I_{CRM}$   | repetitive peak collector current       |                                    | [1][5] | -   | -2   | A         |
| $I_{CM}$  | peak collector current                  | single pulse; $t_p \leq 1$ ms      | [1]    | -   | -3   | A         |
| $R_{CEsat}$   | collector-emitter saturation resistance | $I_C = -500$ mA;<br>$I_B = -50$ mA | [2]    | -   | 240  | 340<br>mΩ |

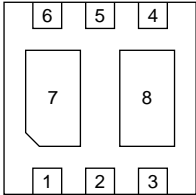
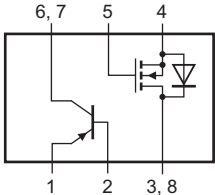
Table 1. Quick reference data ...continued

| Symbol                  | Parameter                        | Conditions   | Min | Typ | Max  | Unit   |
|-------------------------|----------------------------------|--|-----|-----|------|--------|
| N-channel Trench MOSFET |                                  |  |     |     |      |        |
| V <sub>DS</sub>         | drain-source voltage             | T <sub>amb</sub> = 25 °C   | -   | -   | 30   | V      |
| V <sub>GS</sub>         | gate-source voltage              | T <sub>amb</sub> = 25 °C   | -   | -   | ±8   | V      |
| I <sub>D</sub>          | drain current                    | T <sub>amb</sub> = 25 °C;<br>V <sub>GS</sub> = 10 V                        | [3] | -   | 0.66 | A      |
| R <sub>DSon</sub>       | drain-source on-state resistance | T <sub>j</sub> = 25 °C; V <sub>GS</sub> = 4.5 V;<br>I <sub>D</sub> = 0.2 A | [4] | -   | 370  | 580 mΩ |

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.  
[2] Pulse test: t<sub>p</sub> ≤ 300 μs; δ ≤ 0.02.  
[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.  
[4] Pulse test: t<sub>p</sub> ≤ 300 μs; δ ≤ 0.01.  
[5] Pulse test: t<sub>p</sub> ≤ 20 ms; δ ≤ 0.10.

2. Pinning information

Table 2. Pinning

| Pin | Description | Simplified outline   | Graphic symbol   |
|-----|-------------|--|--|
| 1   | emitter     | <br>Transparent top view | <br>017aaa079 |
| 2   | base        |  |  |
| 3   | drain       |  |  |
| 4   | source      |  |  |
| 5   | gate        |  |  |
| 6   | collector   |  |  |
| 7   | collector   |  |  |
| 8   | drain       |  |  |

3. Ordering information

Table 3. Ordering information

| Type number | Package   |  |         |
|-------------|-----------|--|---------|
|             | Name      | Description  | Version |
| PBSM5240PFH | DFN2020-6 | plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 × 2 × 0.65 mm | SOT1118 |

4. Marking

Table 4. Marking code

| Type number | Marking code |
|-------------|--------------|
| PBSM5240PFH | 1T           |

## 5. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

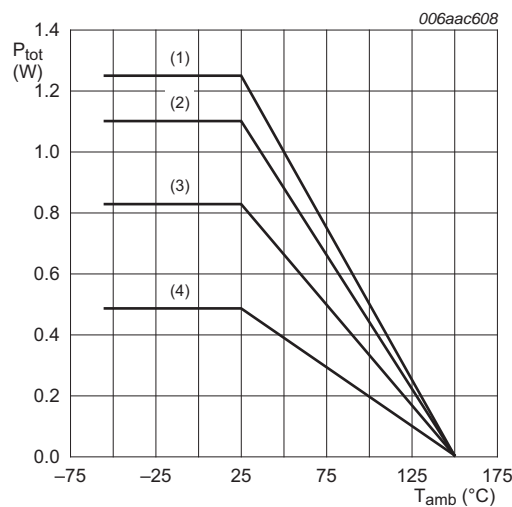
| Symbol                                | Parameter                         | Conditions   | Min      | Max     | Unit |
|---------------------------------------|-----------------------------------|--|----------|---------|------|
| PNP low $V_{CEsat}$ (BISS) transistor |                                   |  |          |         |      |
| $V_{CBO}$                             | collector-base voltage            | open emitter   | -        | -40     | V    |
| $V_{CEO}$                             | collector-emitter voltage         | open base  | -        | -40     | V    |
| $V_{EBO}$                             | emitter-base voltage              | open collector   | -        | -5      | V    |
| $I_C$                                 | collector current                 |  | [1] -    | -1.8    | A    |
| $I_{CRM}$                             | repetitive peak collector current |  | [1][4] - | -2      | A    |
| $I_{CM}$                              | peak collector current            | single pulse;<br>$t_p \leq 1$ ms                             | [1] -    | -3      | A    |
| $I_B$                                 | base current                      |  | [1] -    | -300    | mA   |
| $I_{BM}$                              | peak base current                 | single pulse;<br>$t_p \leq 1$ ms                             | [1] -    | -1      | A    |
| $P_{tot}$                             | total power dissipation           | $T_{amb} \leq 25$ °C   | [1] -    | 1.1     | W    |
|                                       |                                   |  | [2] -    | 1.25    | W    |
| N-channel Trench MOSFET               |                                   |  |          |         |      |
| $V_{DS}$                              | drain-source voltage              | $T_{amb} = 25$ °C  | -        | 30      | V    |
| $V_{DG}$                              | drain-gate voltage                | $T_{amb} = 25$ °C;<br>$R_{GS} = 20$ k $\Omega$               | -        | 30      | V    |
| $V_{GS}$                              | gate-source voltage               | $T_{amb} = 25$ °C  | -        | $\pm 8$ | V    |
| $I_D$                                 | drain current                     | $V_{GS} = 10$ V  | [3]      |         |      |
|                                       |                                   | $T_{amb} = 25$ °C  | -        | 660     | mA   |
|                                       |                                   | $T_{amb} = 100$ °C   | -        | 420     | mA   |
| $I_{DM}$                              | peak drain current                | $T_{amb} = 25$ °C;<br>single pulse;<br>$t_p \leq 10$ $\mu$ s | -        | 3.56    | A    |
| $P_{tot}$                             | total power dissipation           | $T_{amb} = 25$ °C  | [3] -    | 760     | mW   |
| Source-drain diode                    |                                   |  |          |         |      |
| $I_S$                                 | source current                    | $T_{amb} = 25$ °C  | -        | 660     | mA   |
| Per device                            |                                   |  |          |         |      |
| $T_j$                                 | junction temperature              |  | -        | 150     | °C   |
| $T_{amb}$                             | ambient temperature               |  | -55      | +150    | °C   |
| $T_{stg}$                             | storage temperature               |  | -65      | +150    | °C   |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.

[2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>

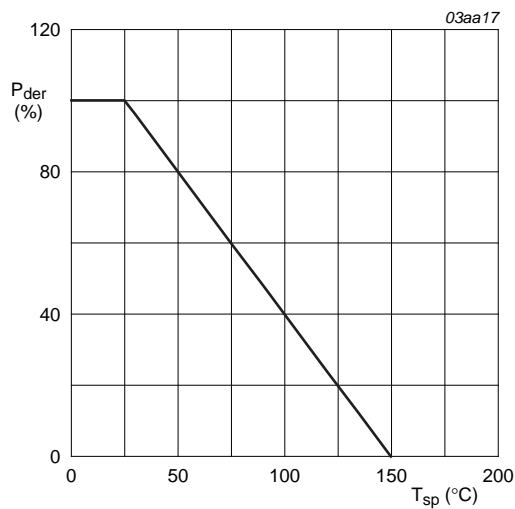
[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

[4] Pulse test:  $t_p \leq 20$  ms;  $\delta \leq 0.10$ .



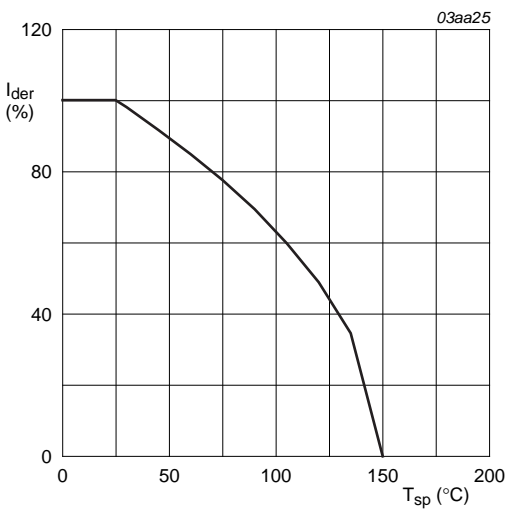
- (1) FR4 PCB, 4-layer copper, mounting pad for collector 1 cm<sup>2</sup>
- (2) FR4 PCB, single-sided copper, mounting pad for collector 6 cm<sup>2</sup>
- (3) FR4 PCB, single-sided copper, mounting pad for collector 1 cm<sup>2</sup>
- (4) FR4 PCB, single-sided copper, standard footprint

Fig 1. BISS transistor: Power derating curves



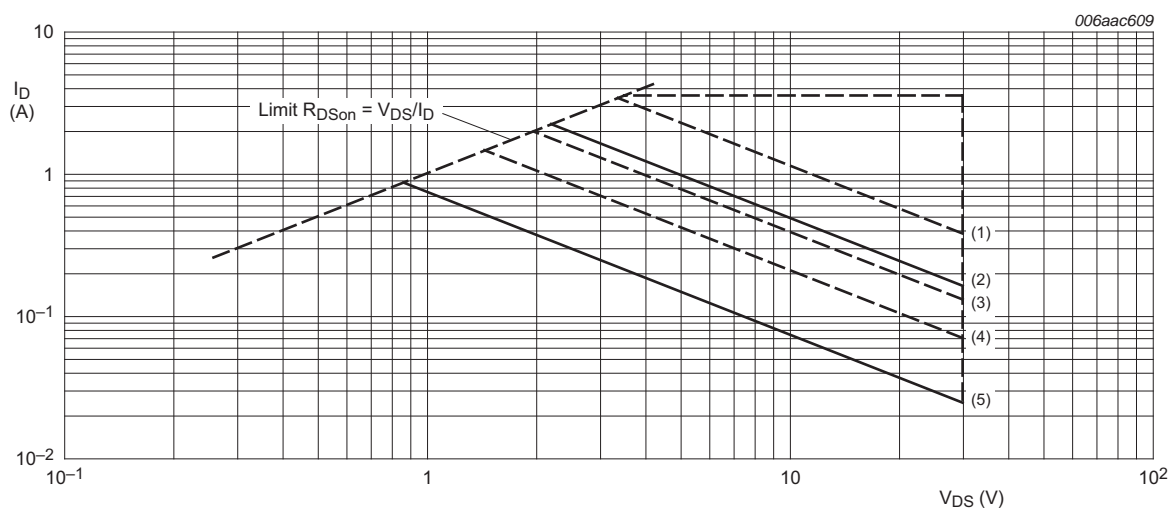
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig 2. MOSFET: Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

Fig 3. MOSFET: Normalized continuous drain current as a function of solder point temperature



$I_{DM}$  = single pulse

- (1)  $t_p = 1$  ms
- (2) DC;  $T_{sp} = 25$  °C
- (3)  $t_p = 10$  ms
- (4)  $t_p = 100$  ms
- (5) DC;  $T_{amb} = 25$  °C; drain mounting pad  $1$  cm<sup>2</sup>

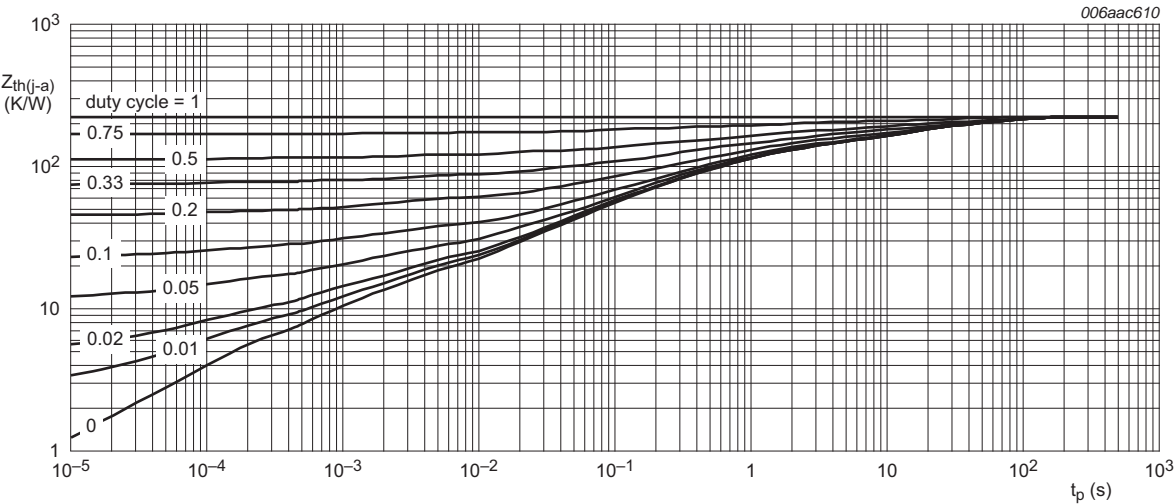
**Fig 4. MOSFET: Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage**

6. Thermal characteristics

Table 6. Thermal characteristics

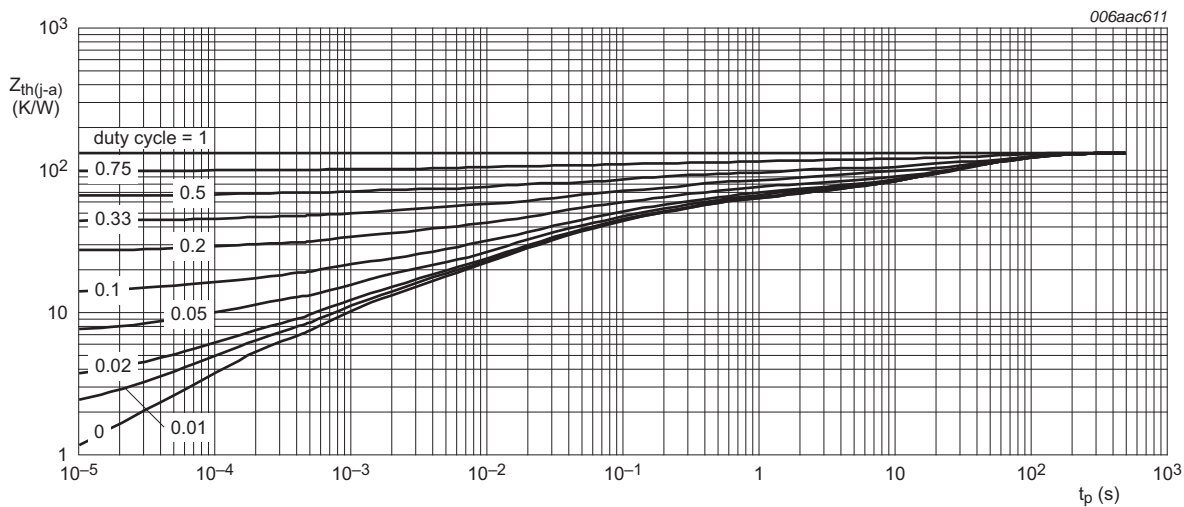
| Symbol                                | Parameter                                   | Conditions  | Min   | Typ | Max | Unit |
|---------------------------------------|---|-------------|-------|-----|-----|------|
| PNP low $V_{CEsat}$ (BISS) transistor |   |             |       |     |     |      |
| $R_{th(j-a)}$                         | thermal resistance from junction to ambient | in free air | [1] - | -   | 115 | K/W  |
|                                       |   |             | [2] - | -   | 100 | K/W  |
| N-channel Trench MOSFET               |   |             |       |     |     |      |
| $R_{th(j-a)}$                         | thermal resistance from junction to ambient | in free air | [3] - | -   | 165 | K/W  |

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.  
[2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.  
[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.



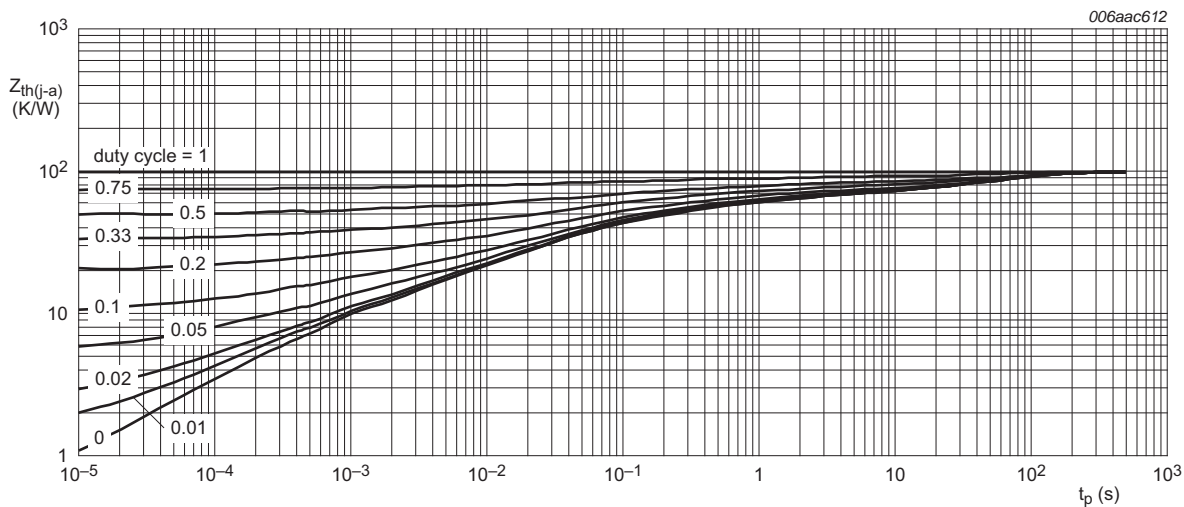
FR4 PCB, single-sided copper, standard footprint

Fig 5. PNP transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



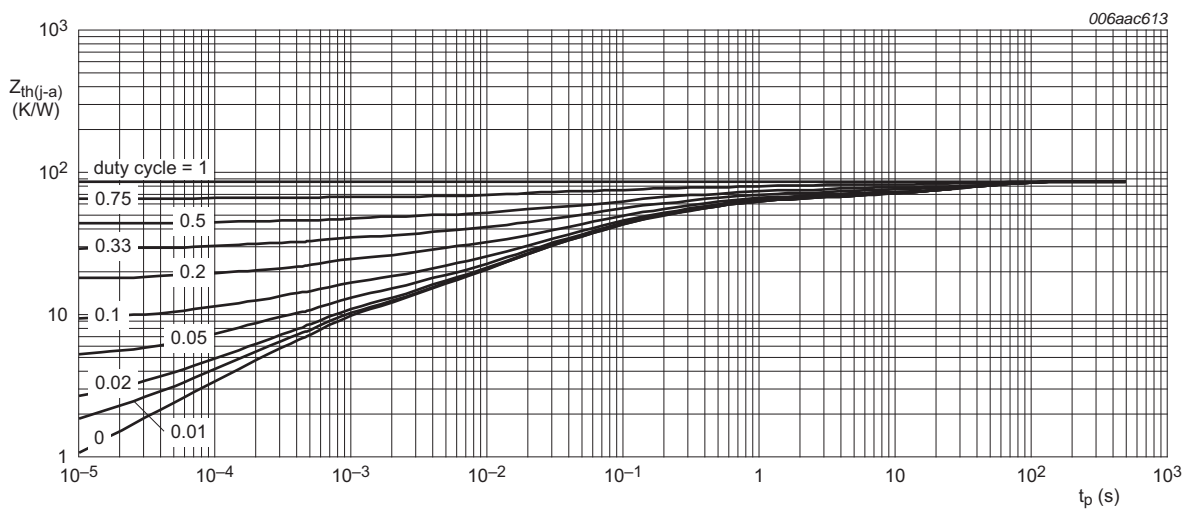
FR4 PCB, single-sided copper, mounting pad for collector 1 cm<sup>2</sup>

Fig 6. PNP transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



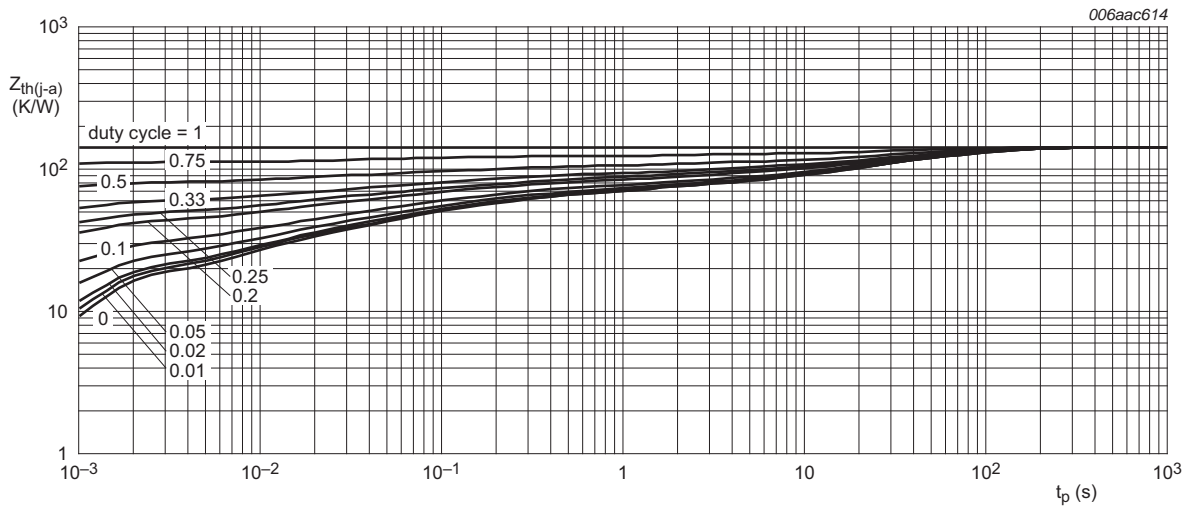
FR4 PCB, single-sided copper, mounting pad for collector 6 cm<sup>2</sup>

Fig 7. PNP transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, mounting pad for collector 1 cm<sup>2</sup>

Fig 8. PNP transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, single-sided copper, mounting pad for drain 1 cm<sup>2</sup>

Fig 9. MOSFET: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



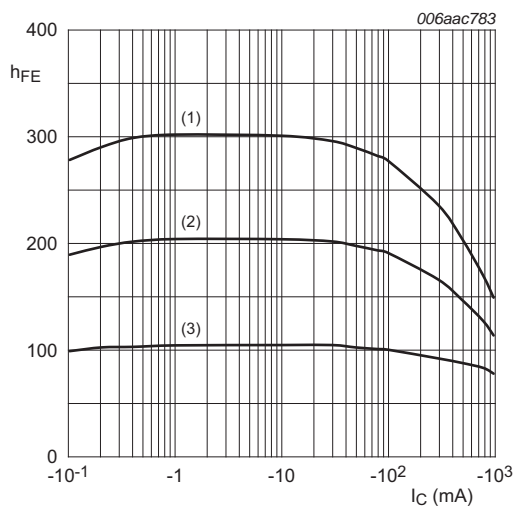
## 7. Characteristics

**Table 7. Characteristics for PNP low  $V_{CEsat}$  transistor**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

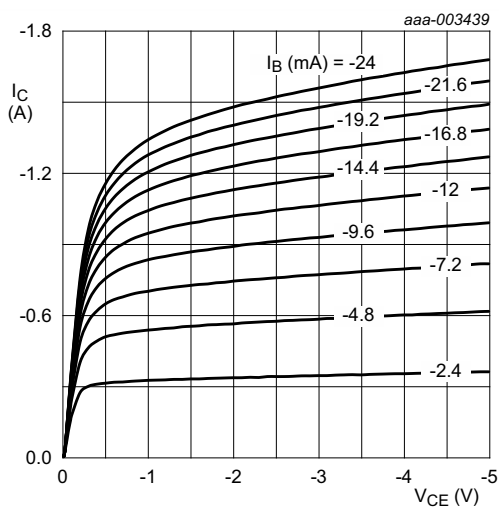
| Symbol      | Parameter                               | Conditions   | Min | Typ | Max  | Unit                 |
|-------------|---|--|-----|-----|------|----------------------|
| $I_{CBO}$   | collector-base cut-off current          | $V_{CB} = -30\text{ V}; I_E = 0\text{ A}$                                    | -   | -   | -100 | nA                   |
|             |   | $V_{CB} = -30\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$ | -   | -   | -50  | $\mu\text{A}$        |
| $I_{CES}$   | collector-emitter cut-off current       | $V_{CE} = -30\text{ V}; I_B = 0\text{ A}$                                    | -   | -   | -100 | nA                   |
| $I_{EBO}$   | emitter-base cut-off current            | $V_{EB} = -5\text{ V}; I_C = 0\text{ A}$                                     | -   | -   | -100 | nA                   |
| $h_{FE}$    | DC current gain                         | $V_{CE} = -5\text{ V}$   | [1] |     |      |                      |
|             |   | $I_C = -1\text{ mA}$   | 100 | -   | -    |                      |
|             |   | $I_C = -100\text{ mA}$   | 100 | -   | -    |                      |
|             |   | $I_C = -1\text{ A}$  | 75  | -   | -    |                      |
| $V_{CEsat}$ | collector-emitter saturation voltage    | $I_C = -100\text{ mA}; I_B = -1\text{ mA}$                                   | [1] | -   | -85  | -140 mV              |
|             |   | $I_C = -500\text{ mA}; I_B = -50\text{ mA}$                                  | [1] | -   | -120 | -170 mV              |
|             |   | $I_C = -1\text{ A}; I_B = -100\text{ mA}$                                    | [1] | -   | -200 | -310 mV              |
| $R_{CEsat}$ | collector-emitter saturation resistance | $I_C = -500\text{ mA}; I_B = -50\text{ mA}$                                  | [1] | -   | 240  | 340 $\text{m}\Omega$ |
| $V_{BEsat}$ | base-emitter saturation voltage         | $I_C = -1\text{ A}; I_B = -100\text{ mA}$                                    | [1] | -   | -    | -1.1 V               |
| $V_{BEon}$  | base-emitter turn-on voltage            | $V_{CE} = -5\text{ V}; I_C = -1\text{ A}$                                    | [1] | -   | -    | -1 V                 |
| $f_T$       | transition frequency                    | $V_{CE} = -10\text{ V}; I_C = -50\text{ mA}; f = 100\text{ MHz}$             | 100 | -   | -    | MHz                  |
| $C_c$       | collector capacitance                   | $V_{CB} = -10\text{ V}; I_E = I_e = 0\text{ A}; f = 1\text{ MHz}$            | -   | -   | 15   | pF                   |

[1] Pulse test:  $t_p \leq 300\text{ }\mu\text{s}$ ;  $\delta \leq 0.02$ .



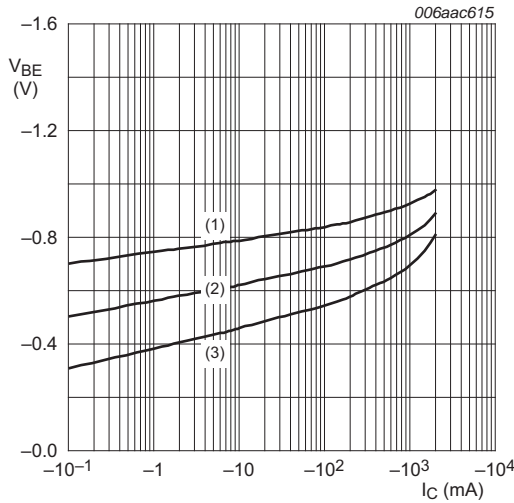
$V_{CE} = -5\text{ V}$   
(1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$   
(2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
(3)  $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 10. PNP transistor: DC current gain as a function of collector current; typical values



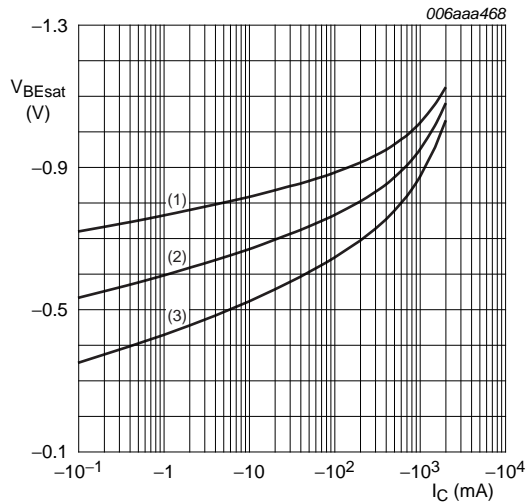
$T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 11. PNP transistor: Collector current as a function of collector-emitter voltage; typical values



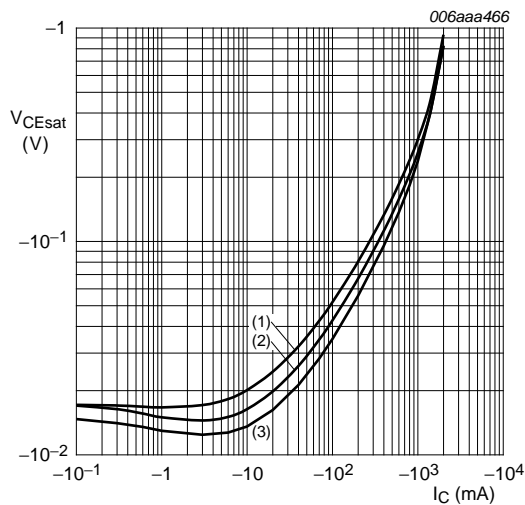
$V_{CE} = -5\text{ V}$   
(1)  $T_{amb} = -55\text{ }^{\circ}\text{C}$   
(2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
(3)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 12. PNP transistor: Base-emitter voltage as a function of collector current; typical values



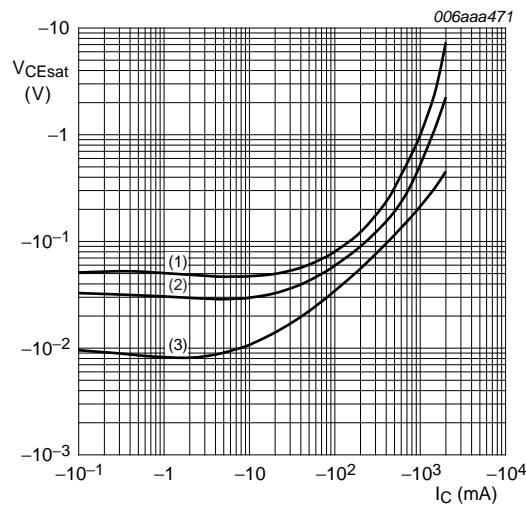
$I_C/I_B = 20$   
(1)  $T_{amb} = -55\text{ }^{\circ}\text{C}$   
(2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
(3)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 13. PNP transistor: Base-emitter saturation voltage as a function of collector current; typical values



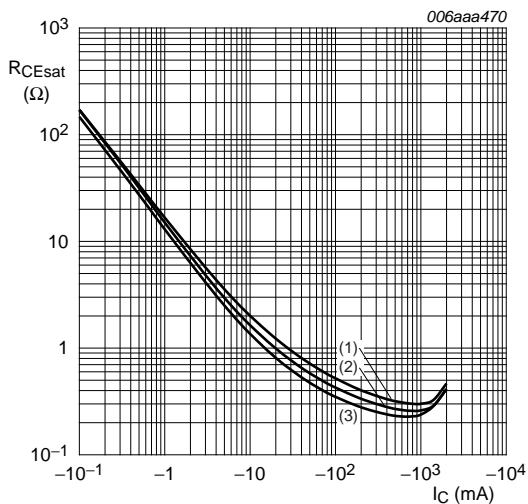
- $I_C/I_B = 20$
- (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$
  - (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
  - (3)  $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 14. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values



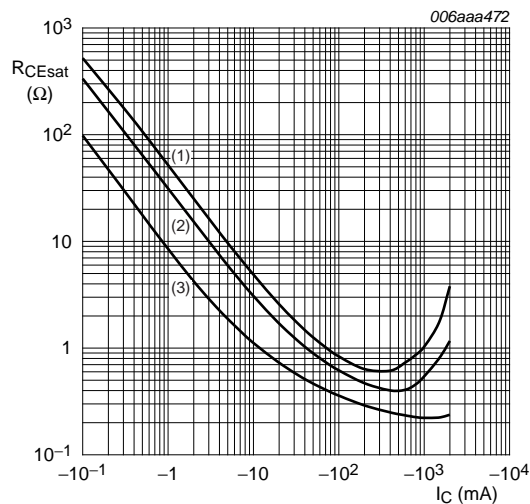
- $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (1)  $I_C/I_B = 100$
  - (2)  $I_C/I_B = 50$
  - (3)  $I_C/I_B = 10$

Fig 15. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values



- $I_C/I_B = 20$
- (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$
  - (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
  - (3)  $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 16. PNP transistor: Collector-emitter saturation resistance as a function of collector current; typical values



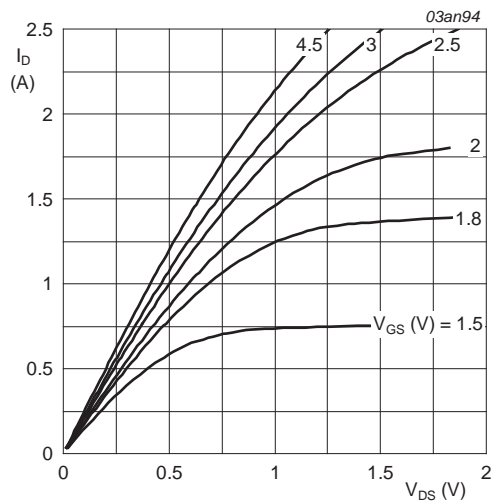
- $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (1)  $I_C/I_B = 100$
  - (2)  $I_C/I_B = 50$
  - (3)  $I_C/I_B = 10$

Fig 17. PNP transistor: Collector-emitter saturation resistance as a function of collector current; typical values

**Table 8. Characteristics for N-channel Trench MOSFET** $T_j = 25\text{ °C}$  unless otherwise specified.

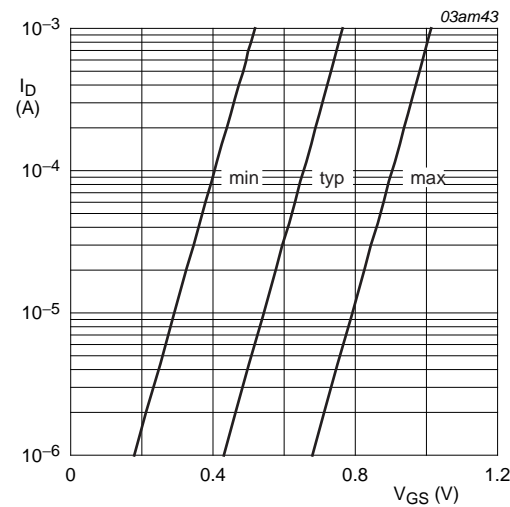
| Symbol                  | Parameter                        | Conditions   | Min  | Typ  | Max  | Unit |
|-------------------------|----------------------------------|--|------|------|------|------|
| Static characteristics  |                                  |  |      |      |      |      |
| V <sub>(BR)DSS</sub>    | drain-source breakdown voltage   | I <sub>D</sub> = 10 μA; V <sub>GS</sub> = 0 V              |      |      |      |      |
|                         |                                  | T <sub>j</sub> = 25 °C                                     | 30   | -    | -    | V    |
|                         |                                  | T <sub>j</sub> = −55 °C                                    | 27   | -    | -    | V    |
| V <sub>GS(th)</sub>     | gate-source threshold voltage    | I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> |      |      |      |      |
|                         |                                  | T <sub>j</sub> = 25 °C                                     | 0.45 | 0.7  | 0.95 | V    |
|                         |                                  | T <sub>j</sub> = 150 °C                                    | 0.25 | -    | -    | V    |
|                         |                                  | T <sub>j</sub> = −55 °C                                    | -    | -    | 1.15 | V    |
| I <sub>DSS</sub>        | drain leakage current            | V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V              |      |      |      |      |
|                         |                                  | T <sub>j</sub> = 25 °C                                     | -    | -    | 1    | μA   |
|                         |                                  | T <sub>j</sub> = 150 °C                                    | -    | -    | 100  | μA   |
| I <sub>GSS</sub>        | gate leakage current             | V <sub>GS</sub> = ±8 V; V <sub>DS</sub> = 0 V              | -    | 10   | ±100 | nA   |
| R <sub>DSon</sub>       | drain-source on-state resistance | V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 0.2 A            | [1]  |      |      |      |
|                         |                                  | T <sub>j</sub> = 25 °C                                     | -    | 370  | 580  | mΩ   |
|                         |                                  | T <sub>j</sub> = 150 °C                                    | -    | 663  | 985  | mΩ   |
|                         |                                  | V <sub>GS</sub> = 2.5 V; I <sub>D</sub> = 0.1 A            | -    | 440  | 690  | mΩ   |
|                         |                                  | V <sub>GS</sub> = 1.8 V; I <sub>D</sub> = 75 mA            | -    | 540  | 920  | mΩ   |
| Dynamic characteristics |                                  |  |      |      |      |      |
| Q <sub>G(tot)</sub>     | total gate charge                | I <sub>D</sub> = 1 A; V <sub>DS</sub> = 15 V;              | -    | 0.89 | -    | nC   |
| Q <sub>GS</sub>         | gate-source charge               | V <sub>GS</sub> = 4.5 V                                    | -    | 0.1  | -    | nC   |
| Q <sub>GD</sub>         | gate-drain charge                |  | -    | 0.2  | -    | nC   |
| C <sub>iss</sub>        | input capacitance                | V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V;             | -    | 43   | -    | pF   |
| C <sub>oss</sub>        | output capacitance               | f = 1 MHz  | -    | 7.7  | -    | pF   |
| C <sub>rss</sub>        | reverse transfer capacitance     |  | -    | 4.8  | -    | pF   |
| t <sub>d(on)</sub>      | turn-on delay time               | V <sub>DS</sub> = 15 V; R <sub>L</sub> = 15 Ω;             | -    | 4.0  | -    | ns   |
| t <sub>r</sub>          | rise time                        | V <sub>GS</sub> = 10 V; R <sub>G</sub> = 6 Ω               | -    | 7.5  | -    | ns   |
| t <sub>d(off)</sub>     | turn-off delay time              |  | -    | 18   | -    | ns   |
| t <sub>f</sub>          | fall time                        |  | -    | 4.5  | -    | ns   |
| Source-drain diode      |                                  |  |      |      |      |      |
| V <sub>SD</sub>         | source-drain voltage             | I <sub>S</sub> = 0.3 A; V <sub>GS</sub> = 0 V              | -    | 0.76 | 1.2  | V    |

[1] Pulse test:  $t_p \leq 300\text{ }\mu\text{s}$ ;  $\delta \leq 0.01$ .



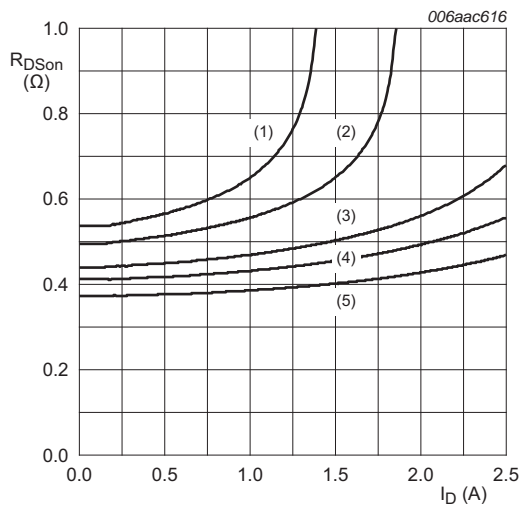
$T_j = 25\text{ }^{\circ}\text{C}$

Fig 18. MOSFET: Output characteristics: drain current as a function of drain-source voltage; typical values



$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

Fig 19. MOSFET: Subthreshold drain current as a function of gate-source voltage



$T_j = 25\text{ }^{\circ}\text{C}$

- (1)  $V_{GS} = 1.8\text{ V}$
- (2)  $V_{GS} = 2.0\text{ V}$
- (3)  $V_{GS} = 2.5\text{ V}$
- (4)  $V_{GS} = 3.0\text{ V}$
- (5)  $V_{GS} = 4.5\text{ V}$

Fig 20. MOSFET: Drain-source on-state resistance as a function of drain current; typical values

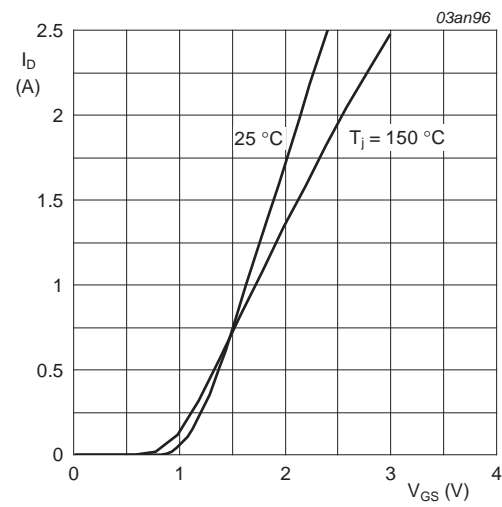
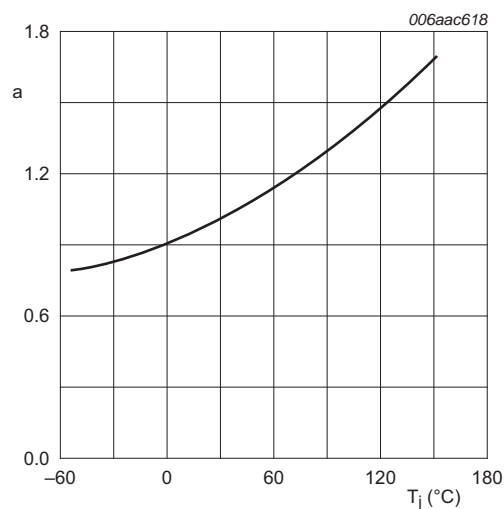
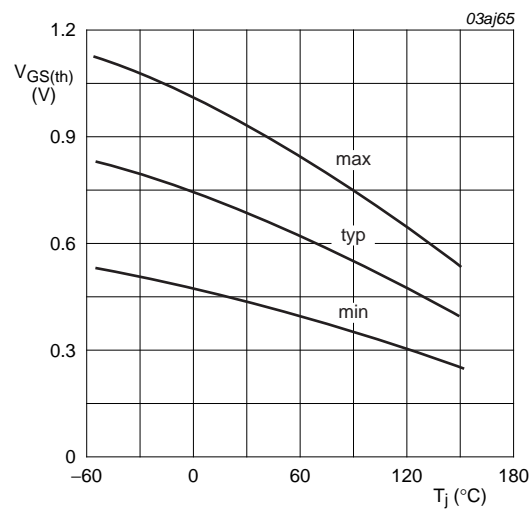


Fig 21. MOSFET: Transfer characteristics: drain current as a function of gate-source voltage; typical values



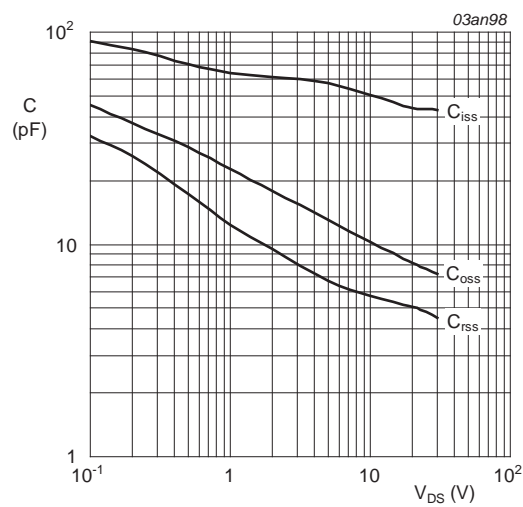
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 22. MOSFET: Normalized drain-source on-state resistance as a function of junction temperature; typical values



$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

Fig 23. MOSFET: Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig 24. MOSFET: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

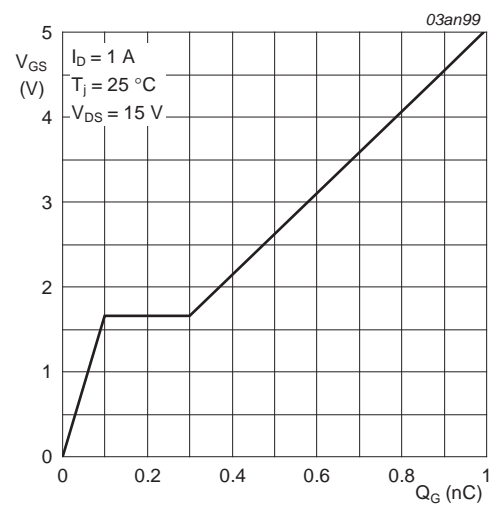


Fig 25. MOSFET: Gate-source voltage as a function of gate charge; typical values

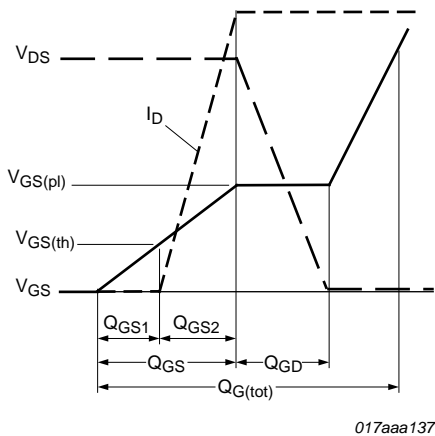


Fig 26. MOSFET: Gate charge waveform definitions

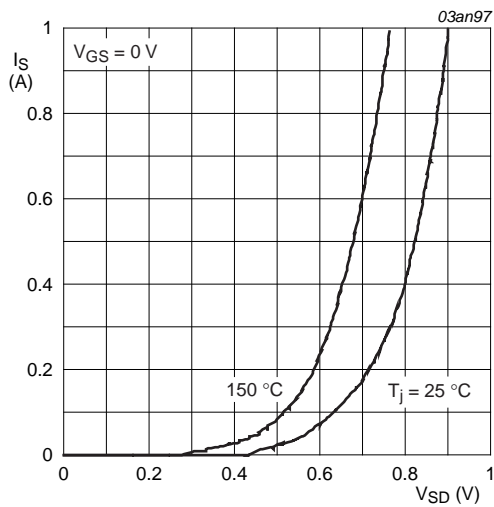


Fig 27. MOSFET: Source current as a function of source-drain voltage; typical values

8. Package outline

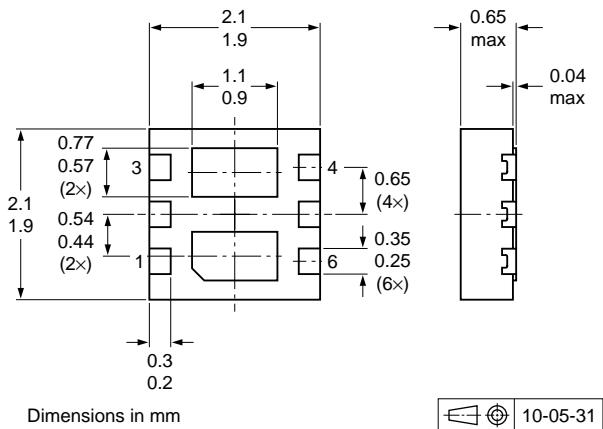


Fig 28. Package outline DFN2020-6 (SOT1118)

9. Packing information

Table 9. Packing methods  
The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

| Type number | Package             | Description                    | Packing quantity |
|-------------|---------------------|--------------------------------|------------------|
|             |                     |                                | 3000             |
| PBSM5240PFH | DFN2020-6 (SOT1118) | 4 mm pitch, 8 mm tape and reel | -115             |

[1] For further information and the availability of packing methods, see [Section 13](#).





## 11. Revision history

Table 10. Revision history

| Document ID     | Release date | Data sheet status  | Change notice | Supersedes |
|-----------------|--------------|--------------------|---------------|------------|
| PBSM5240PFH v.1 | 20120620     | Product data sheet | -             | -          |

## 12. Legal information

### 12.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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