

PBSS5350SS

50 V, 2.7 A PNP/PNP low V_{CEsat} (BISS) transistor

Rev. 01 — 3 April 2007

Product data sheet

1. Product profile

1.1 General description

PNP/PNP double low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a medium power Surface-Mounted Device (SMD) plastic package.

Table 1. Product overview

Type number	Package		NPN/PNP complement	NPN/PNP complement
	NXP	Name		
PBSS5350SS	SOT96-1	SO8	PBSS4350SPN	PBSS4350SS

1.2 Features

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- Dual low power switches (e.g. motors, fans)
- Automotive

1.4 Quick reference data

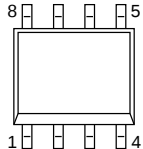
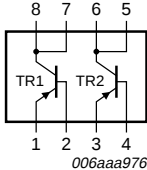
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	-50	V
I_C	collector current		-	-	-2.7	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	-5	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -2$ A; $I_B = -200$ mA	[1] -	95	140	m Ω

[1] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$.

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Symbol
1	emitter TR1		 006aaa976
2	base TR1		
3	emitter TR2		
4	base TR2		
5	collector TR2		
6	collector TR2		
7	collector TR1		
8	collector TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PBSS5350SS	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Marking

Table 5. Marking codes

Type number	Marking code
PBSS5350SS	5350SS

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

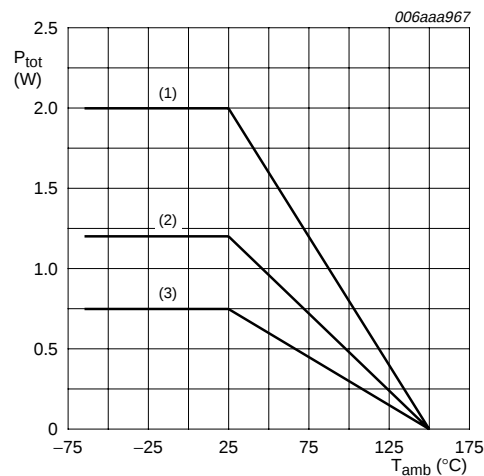
Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor					
V _{CBO}	collector-base voltage	open emitter	-	−50	V
V _{CEO}	collector-emitter voltage	open base	-	−50	V
V _{EBO}	emitter-base voltage	open collector	-	−5	V
I _C	collector current		-	−2.7	A
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms	-	−5	A
I _B	base current		-	−0.5	A
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1] -	0.55	W
			[2] -	0.87	W
			[3] -	1.43	W

Table 6. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^{\circ}\text{C}$	[1] -	0.75	W
			[2] -	1.2	W
			[3] -	2	W
T_j	junction temperature		-	150	$^{\circ}\text{C}$
T_{amb}	ambient temperature		-65	+150	$^{\circ}\text{C}$
T_{stg}	storage temperature		-65	+150	$^{\circ}\text{C}$

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.(1) Ceramic PCB, Al₂O₃, standard footprint(2) FR4 PCB, mounting pad for collector 1 cm²

(3) FR4 PCB, standard footprint

Fig 1. Per device: Power derating curves

6. Thermal characteristics

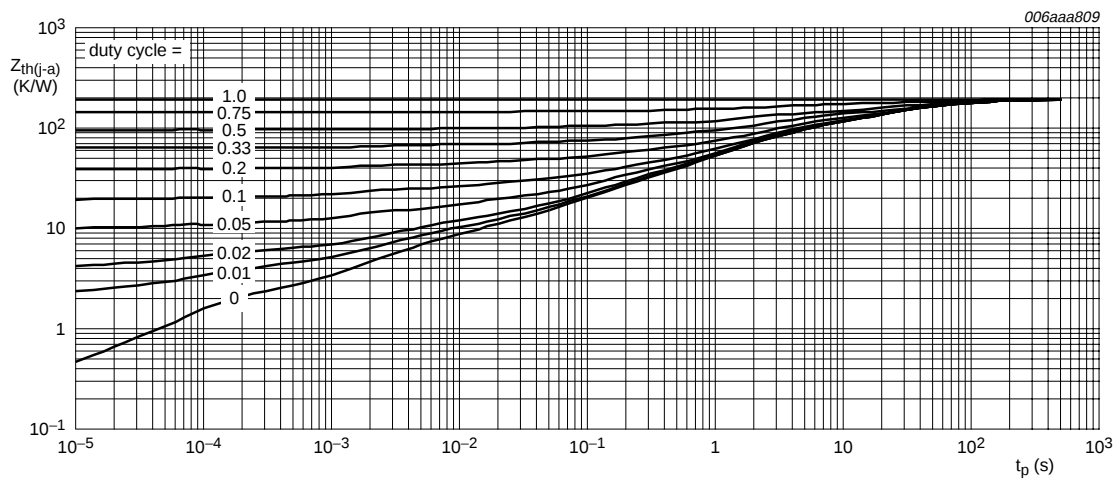
Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] -	-	227	K/W
			[2] -	-	144	K/W
			[3] -	-	87	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	40	K/W
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] -	-	167	K/W
			[2] -	-	104	K/W
			[3] -	-	63	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

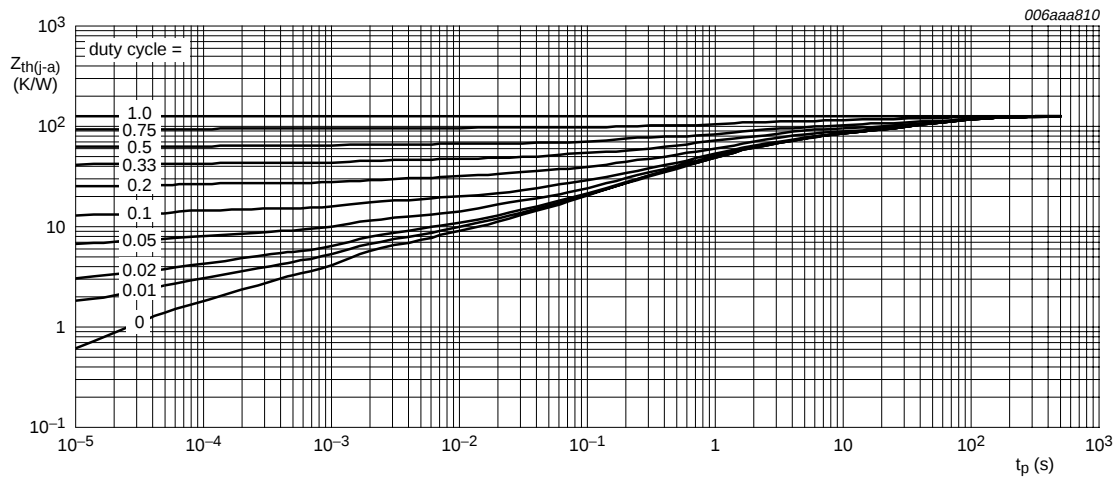
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



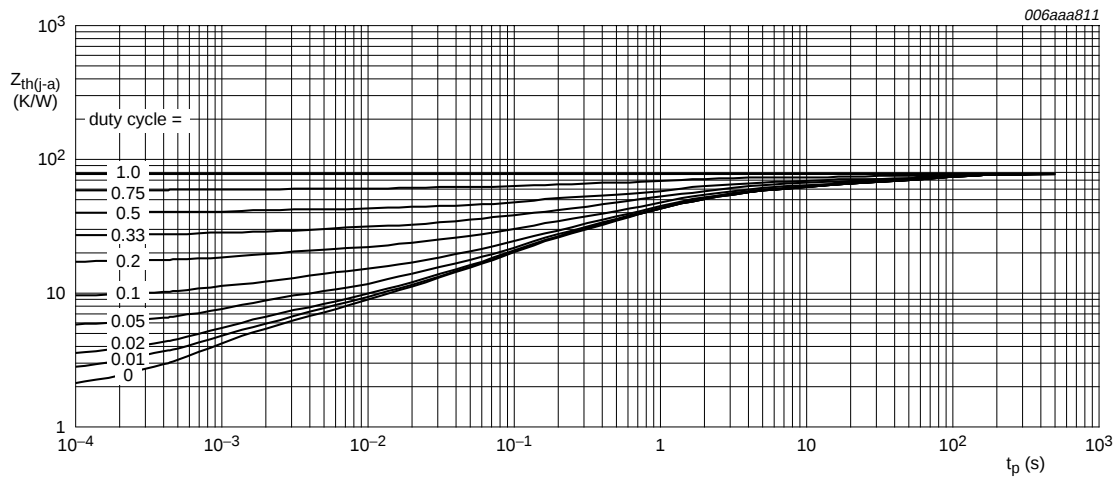
FR4 PCB, standard footprint

Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 1 cm²

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB, Al₂O₃, standard footprint

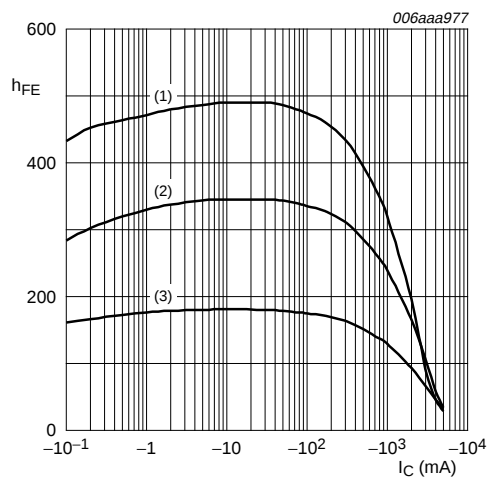
Fig 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 8. Characteristics
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per transistor							
I _{CBO}	collector-base cut-off current	V _{CB} = −50 V; I _E = 0 A	-	-	−100	nA	
		V _{CB} = −50 V; I _E = 0 A; T _j = 150 °C	-	-	−50	μA	
I _{CES}	collector-emitter cut-off current	V _{CE} = −50 V; V _{BE} = 0 V	-	-	−100	nA	
I _{EBO}	emitter-base cut-off current	V _{EB} = −5 V; I _C = 0 A	-	-	−100	nA	
h _{FE}	DC current gain	V _{CE} = −2 V; I _C = −100 mA	200	340	-		
		V _{CE} = −2 V; I _C = −500 mA	[1] 200	290	-		
		V _{CE} = −2 V; I _C = −1 A	[1] 180	250	-		
		V _{CE} = −2 V; I _C = −2 A	[1] 130	180	-		
		V _{CE} = −2 V; I _C = −2.7 A	[1] 95	135	-		
V _{CEsat}	collector-emitter saturation voltage	[1]					
		I _C = −0.5 A; I _B = −50 mA	-	−60	−90	mV	
		I _C = −1 A; I _B = −50 mA	-	−125	−180	mV	
		I _C = −2 A; I _B = −100 mA	-	−225	−320	mV	
		I _C = −2 A; I _B = −200 mA	-	−190	−280	mV	
V _{BEsat}	base-emitter saturation voltage	I _C = −2.7 A; I _B = −270 mA	-	−255	−370	mV	
		[1]					
		I _C = −2 A; I _B = −200 mA	[1]	-	95	140	mΩ
		[1]					
		I _C = −2 A; I _B = −100 mA	-	−0.95	−1.1	V	
V _{BEon}	base-emitter turn-on voltage	I _C = −2.7 A; I _B = −270 mA	-	−1	−1.2	V	
		V _{CE} = −2 V; I _C = −1 A	[1]	-	−0.8	−1.2	V
t _d	delay time	V _{CC} = −10 V; I _C = −2 A;	-	9	-	ns	
t _r	rise time	I _{Bon} = −100 mA;	-	54	-	ns	
t _{on}	turn-on time	I _{Boff} = 100 mA	-	63	-	ns	
t _s	storage time		-	190	-	ns	
t _f	fall time		-	50	-	ns	
t _{off}	turn-off time		-	240	-	ns	
C _C	collector capacitance	V _{CB} = −10 V; I _E = i _e = 0 A; f = 1 MHz	-	25	35	pF	

 [1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.



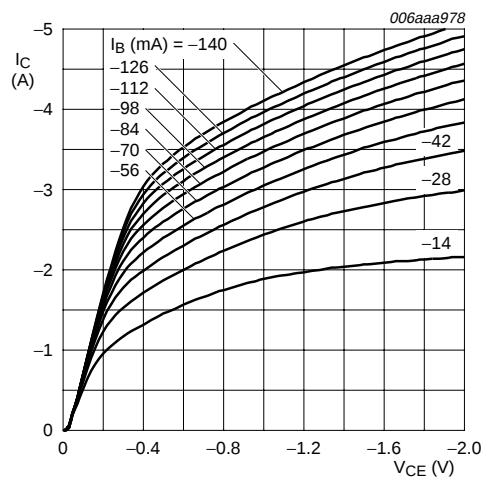
$V_{CE} = -2 \text{ V}$

(1) $T_{amb} = 100 \text{ °C}$

(2) $T_{amb} = 25 \text{ °C}$

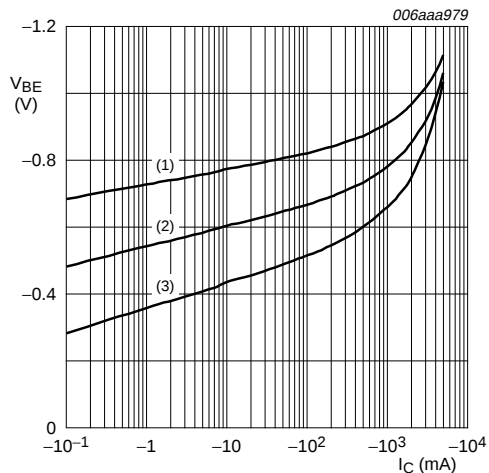
(3) $T_{amb} = -55 \text{ °C}$

Fig 5. DC current gain as a function of collector current; typical values



$T_{amb} = 25 \text{ °C}$

Fig 6. Collector current as a function of collector-emitter voltage; typical values



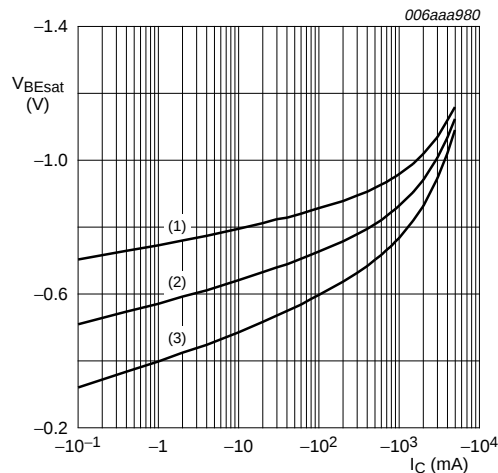
$V_{CE} = -2 \text{ V}$

(1) $T_{amb} = -55 \text{ °C}$

(2) $T_{amb} = 25 \text{ °C}$

(3) $T_{amb} = 100 \text{ °C}$

Fig 7. Base-emitter voltage as a function of collector current; typical values



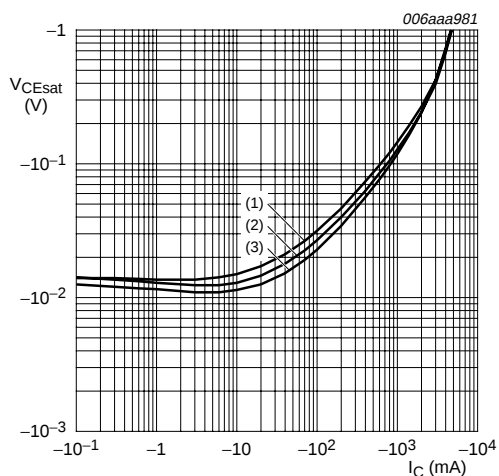
$I_C/I_B = 20$

(1) $T_{amb} = -55 \text{ °C}$

(2) $T_{amb} = 25 \text{ °C}$

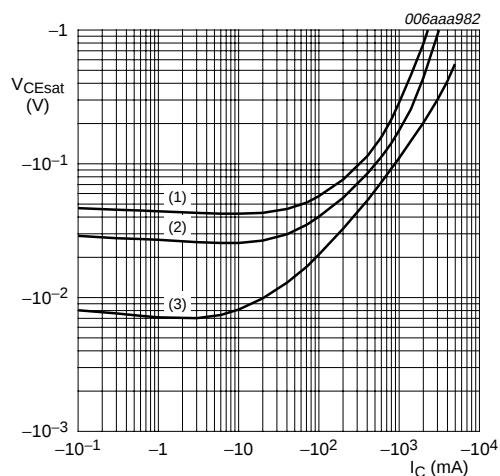
(3) $T_{amb} = 100 \text{ °C}$

Fig 8. Base-emitter saturation voltage as a function of collector current; typical values



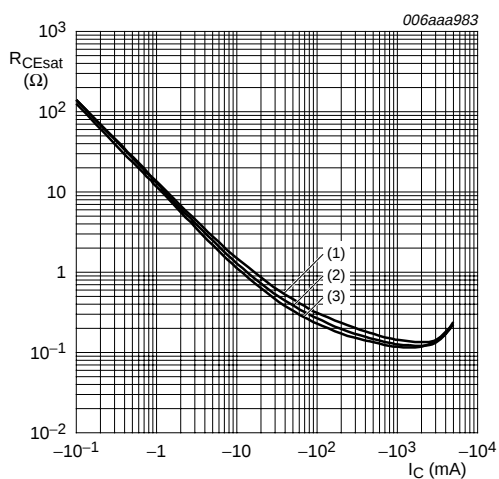
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values



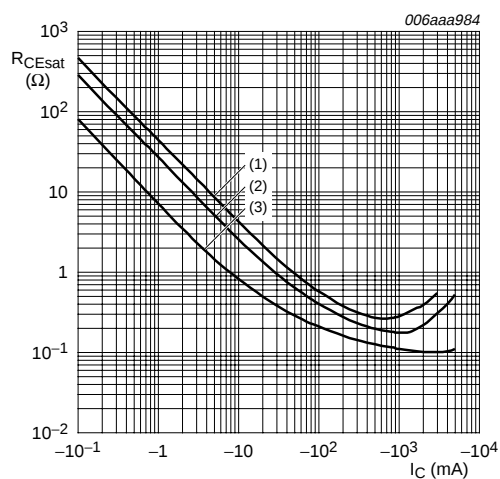
- $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 10$

Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values



- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 11. Collector-emitter saturation resistance as a function of collector current; typical values



- $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 10$

Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values

8. Test information

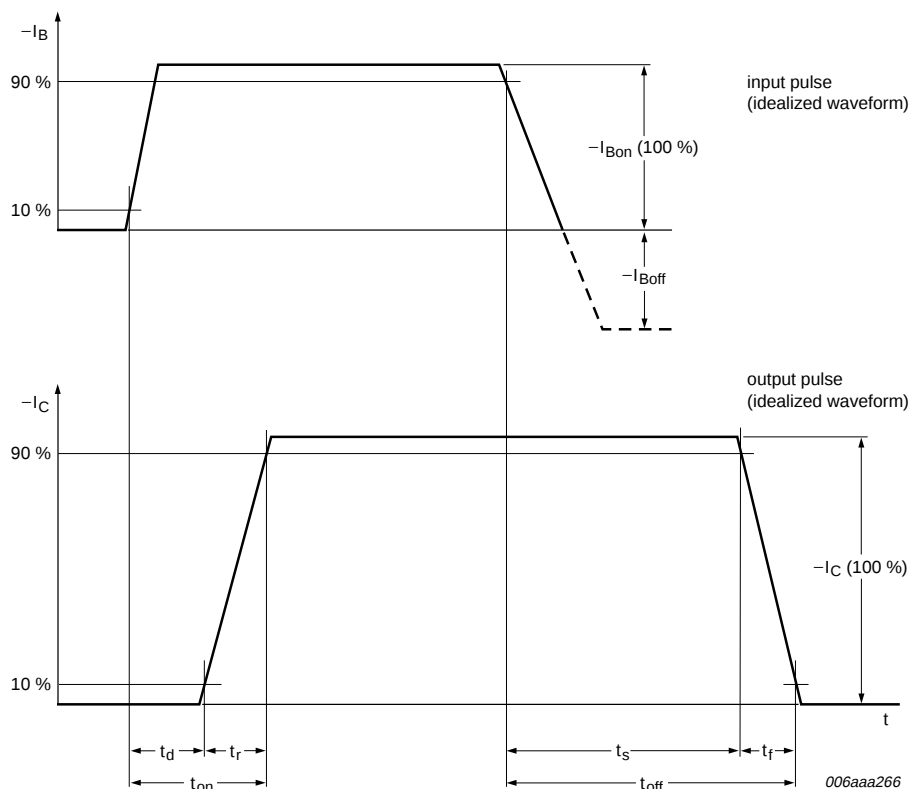
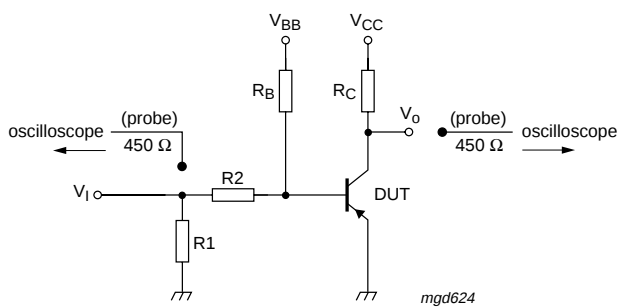


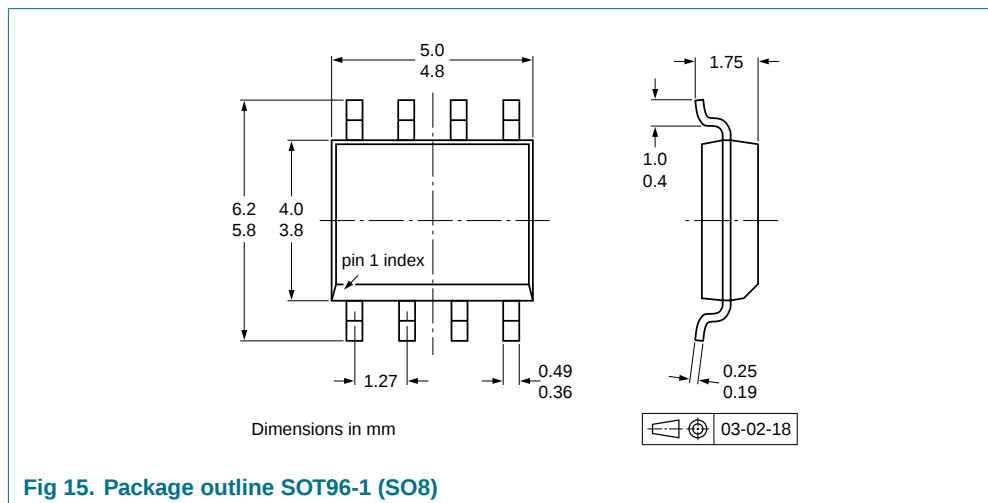
Fig 13. BISS transistor switching time definition



$V_{CC} = -10\text{ V}$; $I_C = -2\text{ A}$; $I_{Bon} = -100\text{ mA}$; $I_{Boff} = 100\text{ mA}$

Fig 14. Test circuit for switching times

9. Package outline



10. Packing information

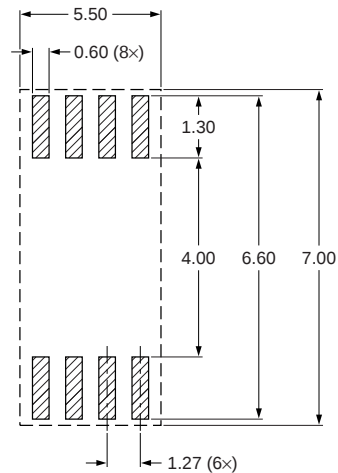
Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity	
			1000	2500
PBSS5350SS	SOT96-1	8 mm pitch, 12 mm tape and reel	-115	-118

[1] For further information and the availability of packing methods, see [Section 14](#).

11. Soldering



▨ solder lands

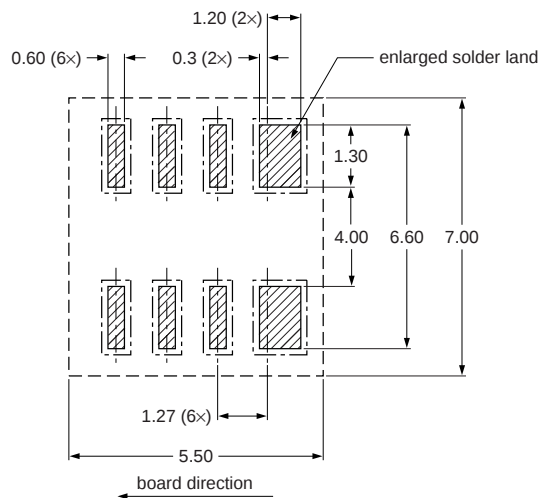
▭ occupied area

placement accuracy ± 0.25

Dimensions in mm

sot096-1_fr

Fig 16. Reflow soldering footprint SOT96-1 (SO8)



▨ solder lands

▭ occupied area

▭ solder resist

placement accuracy ± 0.25

Dimensions in mm

sot096-1_fw

Fig 17. Wave soldering footprint SOT96-1 (SO8)

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS5350SS_1	20070403	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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