CPC5620/CPC5621

LITELINK® III Phone Line Interface IC (DAA)

Features

- Superior voice solution with low noise, excellent part-to-part gain accuracy
- 3 kV_{rms} line isolation
- Transmit power of up to +10 dBm into 600 Ω
- Data access arrangement (DAA) solution for modems at speeds up to V.92
- 3.3 or 5 V power supply operation
- Caller ID signal reception function
- Easy interface with modem ICs and voice CODECs
- Worldwide dial-up telephone network compatibility
- CPC5620 and CPC5621 can be used in circuits that comply with the requirements of TIA/EIA/IS-968 (FCC part 68), UL1950, UL60950, EN/IEC 60950-1 Supplementary Isolation compliant, EN55022B, CISPR22B, EN55024, and TBR-21
- Line-side circuit powered from telephone line
- Compared to other silicon DAA solutions, LITELINK:
  - Uses fewer passive components
  - Takes up less printed-circuit board space
  - Uses less telephone line power
  - Offers simplified operation
  - Is a single-IC solution

Applications

- Computer telephony and gateways, such as VoIP
- PBXs
- Satellite and cable set-top boxes
- V.92 (and other standard) modems
- Fax machines
- Voicemail systems
- Embedded modems for POS terminals, automated banking, remote metering, vending machines, security, and surveillance

Description

LITELINK III is a single-package silicon phone line interface (PLI) DAA used in voice and data communication applications to make connections between low-voltage equipment and high-voltage telephone networks.

LITELINK provides a high-voltage isolation barrier, AC and DC phone line terminations, switch hook, 2-wire to 4-wire hybrid, ring detection, and on-hook signal detection. LITELINK can be used in both differential and single-ended signal applications.

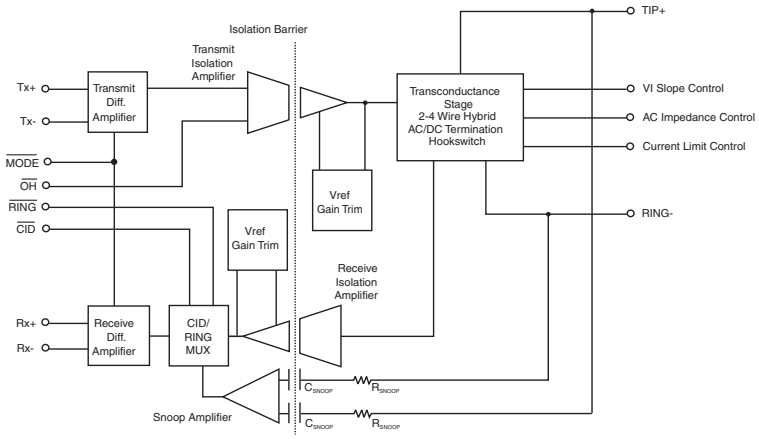
LITELINK uses on-chip optical components and a few inexpensive external components to form a complete voice or high-speed data phone line interface. LITELINK eliminates the need for large isolation transformers or capacitors used in other interface configurations. It includes the required high-voltage isolation barrier in a surface-mount SOIC package.

The CPC5620 (half-wave ringing detect) and CPC5621 (full-wave ringing detect) build upon Clare's LITELINK product line, with improved insertion loss control, improved noise performance, and lower minimum current draw from the phone line. The new mode pin enables worldwide implementation.

Ordering Information

Part Number	Description
CPC5620A	32-pin SOIC, half-wave ring detect, 50/Tube
CPC5620ATR	32-pin SOIC, half-wave ring detect, 1000/Reel
CPC5621A	32-pin SOIC, full-wave ring detect, 50/Tube
CPC5621ATR	32-pin SOIC, full-wave ring detect, 1000/Reel

Figure 1. CPC5620/CPC5621 Block Diagram



1. Electrical Specifications

1.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{DD}	-0.3	6	V
Logic Inputs	-0.3	V_{DD} + 0.3	V
Continuous Tip to Ring Current (R_{ZDC} = 5.2Ω)	-	150	mA
Total Package Power Dissipation	-	1	W
Isolation Voltage	-	3000	V_{rms}
Operating temperature	-40	+85	°C
Storage temperature	-40	+125	°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.2 Performance

Parameter	Minimum	Typical	Maximum	Unit	Conditions
DC Characteristics					
Operating Voltage V_{DD}	3.0	-	5.50	V	Low-voltage side
Operating Current I_{DD}	-	9	13	mA	Low-voltage side
Operating Voltage V_{DDL}	2.8	-	3.2	V	Line side, derived from tip and ring
Operating Current I_{DDL}	-	7	8	mA	Line side, drawn from tip and ring while off-hook
On-hook Characteristics					
Metallic DC Resistance	10	-	-	MΩ	Tip to ring, 100 V_{DC} applied
Longitudinal DC Resistance	10	-	-	MΩ	150 V_{DC} applied from tip and ring to Earth ground
Ringing Signal Detect Level	5	-	-	V_{rms}	68 Hz ring signal applied tip to ring
Ringing Signal Detect Level	28	-	-	V_{rms}	15 Hz ring signal applied tip to ring
Snoop Circuit Frequency Response	166	-	>4000	Hz	-3 dB corner frequency @ 166 Hz, in Clare application circuit
Snoop Circuit CMRR [1]	-	40	-	dB	120 V_{rms} 60 Hz common-mode signal across tip and ring
Ringer Equivalence	-	0.1B	-	REN	
Longitudinal Balance [1]	60	-	-	dB	Per FCC part 68
Off-Hook Characteristics					
AC Impedance	-	600	-	Ω	Tip to ring, using resistive termination application circuit
Longitudinal Balance	40	-	-	dB	Per FCC part 68
Return Loss	-	26	-	dB	Into 600Ω at 1800 Hz
Transmit and Receive Characteristics					
Frequency Response	30	-	4000	Hz	-3 dB corner frequency 30 Hz
Transhybrid Loss	-	36	-	dB	Into 600Ω at 1800 Hz, with C18 in the resistive termination application circuit
Transmit and Receive Insertion Loss	-0.4	0	0.4	dB	30 Hz to 4 kHz, for resistive termination application circuit with $\overline{\text{MODE}}$ de-asserted and for reactive termination application circuit with $\overline{\text{MODE}}$ asserted.
Average In-band Noise	-	-126	-	dBm/Hz	4 kHz flat bandwidth
Harmonic Distortion	-	-80	-	dB	-3 dBm, 600 Hz, 2nd harmonic
Transmit Level	-	-	2.2	V_{P-P}	Single-tone sine wave. Or 0 dBm into 600Ω
Receive Level	-	-	2.2	V_{P-P}	Single-tone sine wave. Or 0 dBm into 600Ω
RX+/RX- Output Drive Current	-	-	0.5	mA	Sink and source
TX+/TX- Input Impedance	60	90	120	kΩ	
Isolation Characteristics					
Isolation Voltage	3000	-	-	V_{rms}	Line side to low-voltage side, one minute duration
Surge Rise Time	2000	-	-	V/μS	No damage via tip and ring
$\overline{\text{MODE}}$, $\overline{\text{OH}}$, and $\overline{\text{CID}}$ Control Logic Inputs					
Input Low Voltage	-	-	0.8	V_{IL}	
Input High Voltage	2.0	-	-	V_{IH}	
High Level Input Current	-	-	-120	μA	$V_{IN} \leq V_{DD}$
Low Level Input Current	-	-	-120	μA	V_{IN} = GND
$\overline{\text{RING}}$ Output Logic Levels					
Output High Voltage	V_{DD} -0.4	-	-	V	I_{OUT} = -400 μA
Output Low Voltage	-	-	0.4	V	I_{OUT} = 1 mA

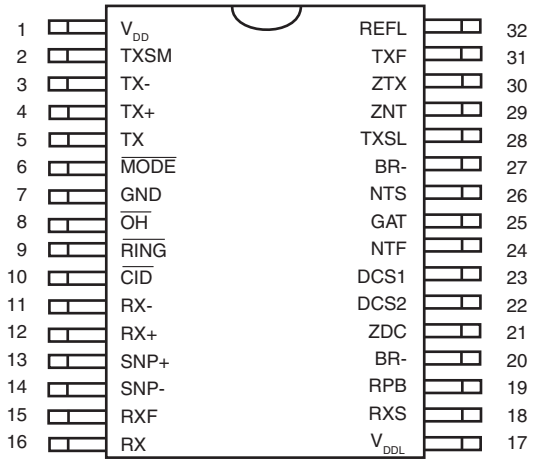
Specifications subject to change without notice. All performance characteristics based on the use of Clare application circuits. Functional operation of the device at conditions beyond those specified here is not implied. All specifications at 25°C and V_{DD} = 5V unless otherwise noted.

1) This parameter is layout and component tolerance dependent.

1.3 Pin Description

Pin	Name	Function
1	VDD	Low-voltage (CPE) side power supply
2	TXSM	Transmit summing junction
3	TX-	Negative differential transmit signal to DAA from low-voltage side
4	TX+	Positive differential transmit signal to DAA from low-voltage side
5	TX	Transmit differential amplifier output
6	$\overline{\text{MODE}}$	When asserted low, changes gain of TX path (-7 dB) and RX path (+7 dB) to accommodate reactive termination networks
7	GND	Low-voltage (CPE) side analog ground
8	$\overline{\text{OH}}$	Assert logic low for off-hook operation
9	$\overline{\text{RING}}$	Ringing Detect Output
10	$\overline{\text{CID}}$	Assert logic low while on hook to allow CID information to be passed to the RX+ and RX- output pins.
11	RX-	Negative differential analog signal received from the telephone line. Must be AC coupled with 0.1 µF.
12	RX+	Positive differential analog signal received from the telephone line. Must be AC coupled with 0.1 µF.
13	SNP+	Positive differential snoop input
14	SNP-	Negative differential snoop input
15	RXF	Receive photodiode amplifier output
16	RX	Receive photodiode summing junction
17	VDDL	Power supply for line side, regulated from tip and ring.
18	RXS	Receive isolation amp summing junction
19	RPB	Receive LED pre-bias current set
20	BR-	Bridge rectifier return
21	ZDC	Electronic inductor DCR/current limit
22	DCS2	DC feedback output
23	DCS1	V to I slope control
24	NTF	Network amplifier feedback
25	GAT	External MOSFET gate control
26	NTS	Receive signal input
27	BR-	Bridge rectifier return
28	TXSL	Transmit photodiode summing junction
29	ZNT	Receiver impedance set
30	ZTX	Transmit transconductance gain set
31	TXF	Transmit photodiode amplifier output
32	REFL	1.25 V_{DC} reference

Figure 2. Pinout



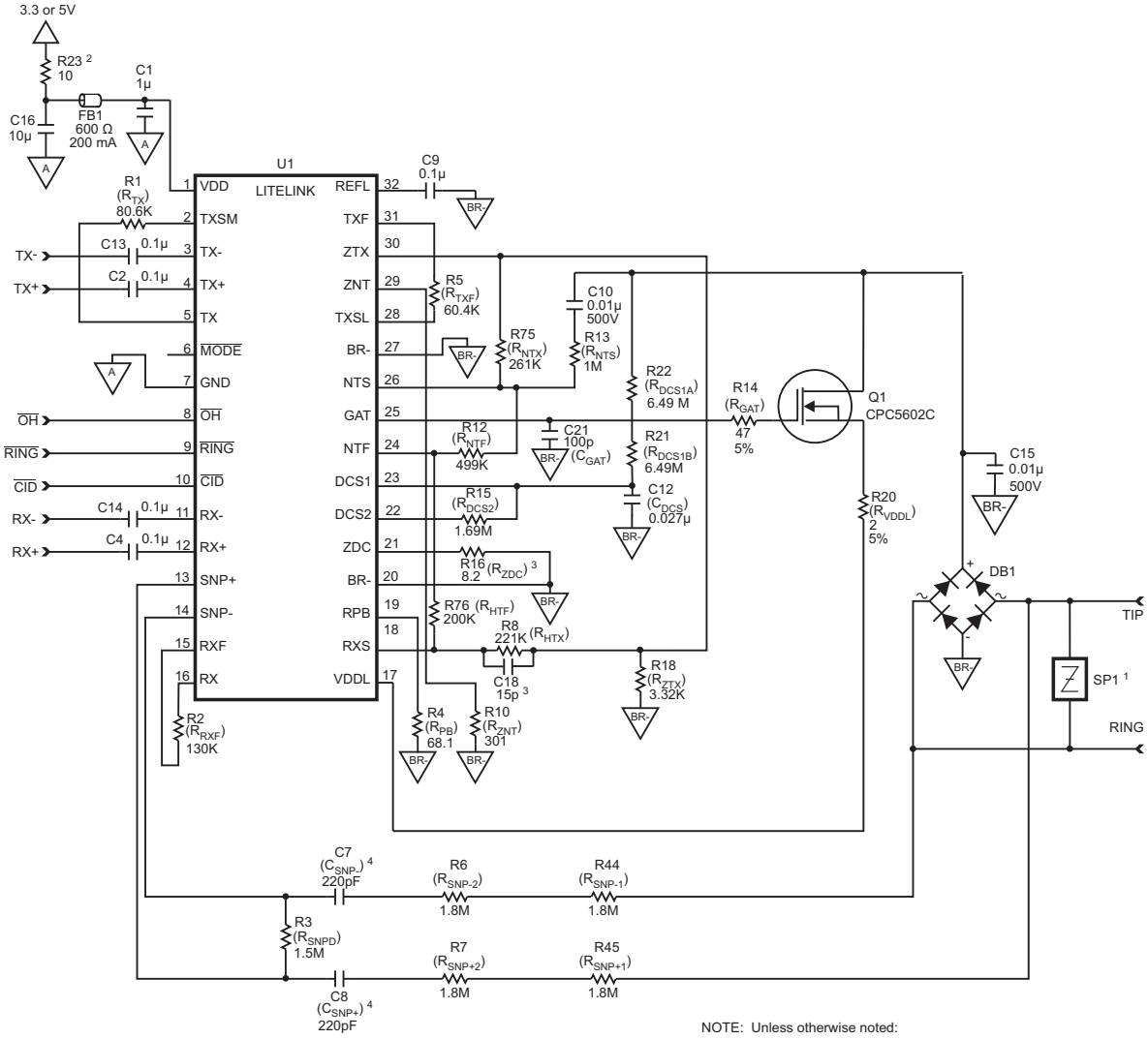
2. Application Circuits

LITELINK can be used with telephone networks worldwide. Some public telephone networks, notably in North America and Japan require resistive line termination. Other telephone networks, as in Europe and elsewhere, require a reactive line termination.

The application circuits below address both line termination models. The reactive termination application circuit (see Figure 4 on page 8) describes the TBR-21 implementation. This circuit can be adapted easily for other reactive termination needs.

2.1 Resistive Termination Application Circuit

Figure 3. Resistive Termination Application Circuit Schematic



[1]This design was tested and found to comply with FCC Part 68 with this Sidactor. Other compliance requirements may require a different part.

*[2]Higher-noise power supplies may require substitution of a 220 µH inductor, Toko 380HB-2215 or similar. See the Power Quality section of Clare application note AN-146, **Guidelines for Effective LITELINK Designs** for more information.*

[3]Optional for enhanced transhybrid loss.

[4]Use voltage ratings based on the isolation requirements of your application.

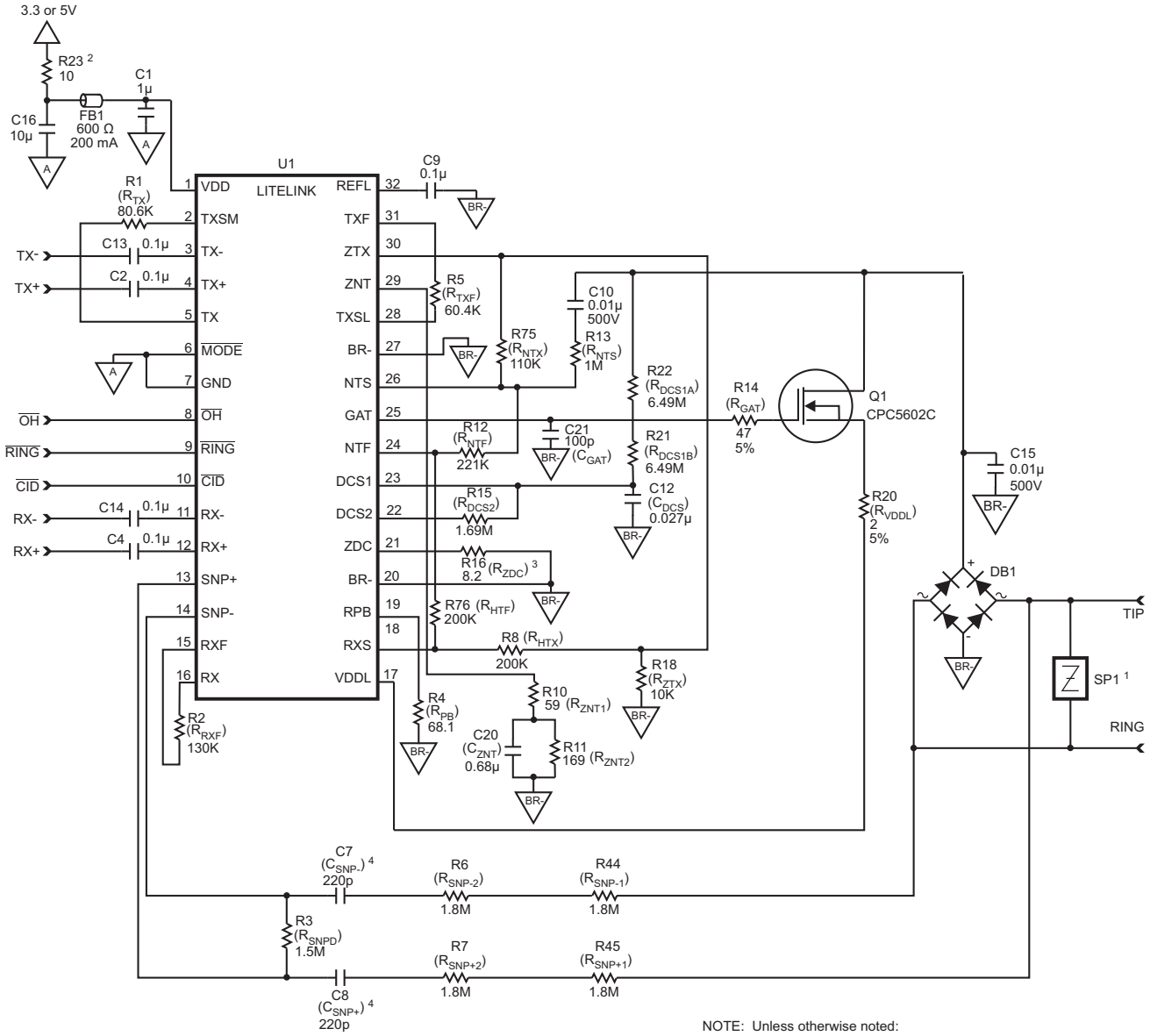
2.1.1 Resistive Termination Application Circuit Part List

Quantity	Reference Designator	Description	Supplier(s)
1	C1	1 µF, 16 V, ±10%	AVX, Murata, Novacap, Panasonic, SMEC, Tecate, etc.
5	C2, C4, C9, C13, C14	0.1 µF, 16 V, ±10%	
2	C7, C8 [1]	220 pF, ±5%	
2	C10, C15	0.01 µF, 500 V, ±10%	
1	C12	0.027 µF, 16 V, ±10%	
1	C16	10 µF, 16 V, ±10%	
1	C18 (optional)	15 pF, 16 V, ±10%	
1	C21	100 pF, 16 V, 10%	
1	R1	80.6 kΩ, 1/16 W, ±1%	Panasonic, Electro Films, FMI, Vishay, etc.
1	R2	130 kΩ, 1/16 W, ±1%	
1	R3	1.5 MΩ, 1/16 W, ±1%	
1	R4	68.1 Ω, 1/16 W, ±1%	
1	R5	60.4 kΩ, 1/16 W, ±1%	
4	R6, R7, R44, R45 [2]	1.8 MΩ, 1/10 W, ±1%	
1	R8	221 kΩ, 1/16 W, ±1%	
1	R10	301 Ω, 1/16 W, ±1%	
1	R12	499 kΩ, 1/16 W, ±1%	
1	R13	1 MΩ, 1/16 W, ±1%	
1	R14	47 Ω, 1/16 W, ±5%	
1	R15	1.69 MΩ, 1/16 W, ±1%	
1	R16	8.2 Ω, 1/8 W, ±1%	
1	R18	3.32 kΩ, 1/16 W, ±1%	
1	R20	2 Ω, 1/16 W, ±5%	
1	R21, R22	6.49 MΩ, 1/16 W, ±1%	
1	R23	10 Ω, 1/16 W, ±5%, or 220 µH inductor	
1	R75	261 kΩ, 1/16 W, ±1%	
1	R76	200 kΩ, 1/16 W, ±1%	
1	FB1	600 Ω, 200 mA ferrite bead	Murata BLM11A601S or similar
1	DB1	S1ZB60 bridge rectifier	Shindengen, Diodes, Inc.
1	SP1	350 V	Bourns (TISP4350H3) or Teccor (P3100SC)
1	Q1	CPC5602 FET	Clare
1	U1	CPC5620/CPC5621 LITELINK	

[1]Use voltage ratings based on the isolation requirements of your application. Typical applications will require 2kV to safely hold off the isolation voltage.

[2]Use components that allow enough space to account for the possibility of high-voltage arcing.

Figure 4. Reactive Termination Application Circuit Schematic



NOTE: Unless otherwise noted:
Resistor values are in Ohms
All resistors are 1%.
Capacitor values are in Farads.

[1]This design was tested and found to comply with FCC Part 68 with this Sidactor. Other compliance requirements may require a different part.

*[2]Higher-noise power supplies may require substitution of a 220 µH inductor, Toko 380HB-2215 or similar. See the Power Quality section of Clare application note AN-146, **Guidelines for Effective LITELINK Designs** for more information.*

*[3]R_{ZDC} sets the loop-current limit, see **"Setting a Current Limit" on page 13**. Also see Clare's application note AN-146 for heat sinking recommendations for the CPC5602C FET.*

[4]Use voltage ratings based on the isolation requirements of your application.

2.1.2 Reactive Termination Application Circuit Part List

Quantity	Reference Designator	Description	Supplier
1	C1	1 µF, 16 V, ±10%	AVX, Murata, Novacap, Panasonic, SMEC, Tecate, etc.
5	C2, C4, C9, C13, C14	0.1 µF, 16 V, ±10%	
2	C7, C8 [1]	220 pF, ±5%	
2	C10, C15	0.01 µF, 500 V, ±10%	
1	C12	0.027 µF, 16 V, ±10%	
1	C16	10 µF, 16 V, ±10%	
1	C20	0.68 µF, 16 V, ±10%	
1	C21	100 pF, 16 V, 10%	
1	R1	80.6 kΩ, 1/16 W, ±1%	Panasonic, Electro Films, FMI, Vishay, etc.
1	R2	130 kΩ, 1/16 W, ±1%	
1	R3	1.5 MΩ, 1/16 W, ±1%	
1	R4	68.1 Ω, 1/16 W, ±1%	
1	R5	60.4 kΩ, 1/16 W, ±1%	
4	R6, R7, R44, R45 [2]	1.8 MΩ, 1/10 W, ±1%	
1	R8	200 kΩ, 1/16 W, ±1%	
1	R10	59 Ω, 1/16 W, ±1%	
1	R11	169 Ω, 1/16 W, ±1%	
1	R12	221 kΩ, 1/16 W, ±1%	
1	R13	1 MΩ, 1/16 W, ±1%	
1	R14	47 Ω, 1/16 W, ±5%	
1	R15	1.69 MΩ, 1/16 W, ±1%	
1	R16	8.2 Ω, 1/8 W, ±1%	
1	R18	10 kΩ, 1/16 W, ±1%	
1	R20	2 Ω, 1/16 W, ±5%	
1	R21, R22	6.49 MΩ, 1/16 W, ±1%	
1	R23	10 Ω, 1/16 W, ±5%, or 220 µH inductor	
1	R75	110 kΩ, 1/16 W, ±1%	
1	R76	200 kΩ, 1/16 W, ±1%	
1	FB1	600 Ω, 200 mA ferrite bead	Murata BLM11A601S or similar
1	DB1	S1ZB60 bridge rectifier	Shindengen, Diodes, Inc.
1	SP1	350 V	Bourns (TISP4350H3) or Teccor (P3100SC)
1	Q1	CPC5602 FET	Clare
1	U1	CPC5620/CPC5621 LITELINK	

[1]Use voltage ratings based on the isolation requirements of your application. Typical applications will require 2kV to safely hold off the isolation voltage.

[2]Use components that allow enough space to account for the possibility of high-voltage arcing.

3. Using LITELINK

As a full-featured telephone line interface, LITELINK performs the following functions:

- DC termination and V/I slope control
- AC impedance control
- 2-wire to 4-wire conversion (hybrid)
- Current limiting
- Ringing signal reception
- Caller ID signaling reception
- Switch hook

LITELINK can accommodate specific application features without sacrificing basic functionality and performance. Application features include, but are not limited to:

- High transmit power operation
- Pulse dialing
- Ground start
- Loop start
- Parallel telephone off-hook detection (line intrusion)
- Battery reversal detection
- Line presence detection
- World-wide programmable operation

This section of the data sheet describes LITELINK operation in standard configuration for usual operation. Clare offers additional application information on-line (see Section 5 on page 13). These include information on the following topics:

- Circuit isolation considerations
- Optimizing LITELINK performance
- Data Access Arrangement architecture
- LITELINK circuit descriptions
- Surge protection
- EMI considerations

Other specific application materials are also referenced in this section as appropriate.

3.1 Switch Hook Control (On-hook and Off-hook States)

LITELINK operates in one of two conditions, on-hook and off-hook. In the on-hook condition the telephone line is available for calls. In the off-hook condition the telephone line is engaged. The $\overline{OH}$ control input is used to place LITELINK in one of these two states.

With $\overline{OH}$ high, LITELINK is on-hook and ready to make or receive a call. While on-hook, the $\overline{CID}$ control is used to select between passing the caller-ID tones from Tip and Ring to the RX+ and RX- outputs and the ringing detect function. Setting $\overline{CID}$ to a logic low enables the CID path while placing $\overline{CID}$ to a logic high configures the LITELINK to detect ringing.

Asserting $\overline{OH}$ low causes LITELINK to answer or originate a call by entering the off-hook state. In the off-hook state, loop current flows through LITELINK.

3.2 On-hook Operation: $\overline{OH}$=1

The LITELINK application circuit leakage current is less than 10 μA with 100 V across ring and tip, equivalent to greater than 10 MΩ on-hook resistance.

3.2.1 Ringing Signal Reception via the Snoop Circuit

In the on-hook state (OH and CID not asserted), an internal multiplexer turns on the snoop circuit. This circuit monitors the telephone line for two conditions; an incoming ring signal, and caller ID data bursts.

Refer to the application schematic diagram (see Figure 3. on page 6). C7 (CSNP-) and C8 (CSNP+) provide a high-voltage isolation barrier between the telephone line and SNP- and SNP+ on the LITELINK while coupling AC signals to the snoop amplifier. The snoop circuit “snoops” the telephone line continuously while drawing no current. In the LITELINK, ringing signals are compared to a threshold. The comparator output forms the RING signal output from LITELINK. This signal must be qualified by the host system as a valid ringing signal. A low level on RING indicates that the LITELINK ring signal threshold has been exceeded.

For the CPC5620 (with the half-wave ring detector), the frequency of the RING output follows the frequency of the ringing signal from the central office (CO), typically 20 Hz. The RING output of the CPC5621 (with the full-wave ring detector) is twice the ringing signal frequency.

Hysteresis is employed in the LITELINK ring detector circuit to provide noise immunity. The set-up of the ring detector comparator causes RING output pulses to remain low for most of the ringing signal half-cycle. The RING output returns high for the entire negative half-cycle of the ringing signal for the CPC5620. For the CPC5621, the RING output returns high for a short period near the zero-crossing of the ringing signal before returning low during the positive half-cycle. For both the CPC5620 and CPC5621, the RING output remains high between ringing signal bursts.

The ringing detection threshold depends on the values of R3 (R_{SNPD}), R6 & R44 (R_{SNP-}), R7 & R45 (R_{SNP+}), C7 (C_{SNP-}), and C8 (C_{SNP+}). The value of these components shown in the application circuits are recommended for typical operation. The ringing detection threshold can be changed according to the following formula:

$$V_{RINGPK} = \left(\frac{750mV}{R_{SNPD}}\right)\sqrt{\left[(R_{SNP_{TOTAL}} + R_{SNPD})^2 + \frac{1}{(\pi f_{RING} C_{SNP})^2}\right]}$$

Where:

- R_{SNPD} = R3 in the application circuits shown in this data sheet.
- $RSNP_{TOTAL}$ = the total of R6, R7, R44, and R45 in the application circuits shown in this data sheet.
- C_{SNP} = C7 = C8 in the application circuits shown in this data sheet.
- And f_{RING} is the frequency of the ringing signal.

Clare Application Note AN-117 **Customize Caller ID Gain and Ring Detect Voltage Threshold** is a spreadsheet for trying different component values in this circuit. Changing the ringing detection threshold will also change the caller ID gain and the timing of the polarity reversal detection pulse, if used.

3.2.2 Polarity Reversal Detection with CPC5621 in On-hook State

The full-wave ringing detector in the CPC5621 makes it possible to detect on-hook tip and ring polarity reversal using the $\overline{RING}$ output. When the polarity of tip and ring reverses, a pulse on $\overline{RING}$ indicates the event. Your system logic must be able to discriminate this single pulse of approximately 1 msec (using the recommended snoop circuit external components) from a valid ringing signal.

3.2.3 On-hook Caller ID Signal Reception

On-hook caller ID (CID) signals are processed by LITELINK by coupling the CID data burst through the snoop circuit to the LITELINK RX outputs under control of the $\overline{CID}$ pin. In North America, CID data signals are typically sent between the first and second ringing signal.

In North American applications, follow these steps to receive on-hook caller ID data via the LITELINK RX outputs:

1. Detect the first ringing signal outputs on $\overline{RING}$.
2. Assert $\overline{CID}$ low.
3. Process the CID data from the RX outputs.
4. De-assert $\overline{CID}$ (high or floating).

Note: Taking LITELINK off-hook (via the $\overline{OH}$ pin) disconnects the snoop path from both the receive outputs and the $\overline{RING}$ output, regardless of the state of the $\overline{CID}$ pin.

CID gain from tip and ring to RX+ and RX- is determined by:

$$GAIN_{CID}(dB) = 20\log\left[\frac{6R_{SNPD}}{\sqrt{\left[(R_{SNP_{TOTAL}} + R_{SNPD})^2 + \frac{1}{(\pi f C_{SNP})^2}\right]}}\right]$$

Where:

- R_{SNPD} = R3 in the application circuits in this data sheet
- $RSNP_{TOTAL}$ = the total of R6, R7, R44, and R45 in the application circuits in this data sheet
- C_{SNP} = C7 = C8 in the application circuits in this data sheet
- and where f is the frequency of the CID signal

The recommended components in the application circuit yield a gain 0.27 dB at 2000 Hz. Clare Application Note AN-117 **Customize Caller ID Gain and Ring Detect Voltage Threshold** is a spreadsheet for trying different component values in this circuit. Changing the CID gain will also change the ring detection threshold and the timing of the polarity reversal detection pulse, if used.

For single-ended receive applications where only one RX output is used, the snoop circuit gain can be adjusted back to 0 dB by changing the value of the snoop series resistors R6, R7, R44 and R45 from 1.8MΩ to 715kΩ. This change results in negligible modification to the ringing detect threshold.

3.3 Off-Hook Operation: $\overline{OH}$=0

3.3.1 Receive Signal Path

Signals to and from the telephone network appear on the tip and ring connections of the application circuit. Receive signals are extracted from transmit signals by the LITELINK two-wire to four-wire hybrid. Next, the receive signal is converted to infrared light by the receive photodiode amplifier and receive path LED. The intensity of the light is modulated by the receive

signal and coupled across the electrical isolation barrier by a reflective dome.

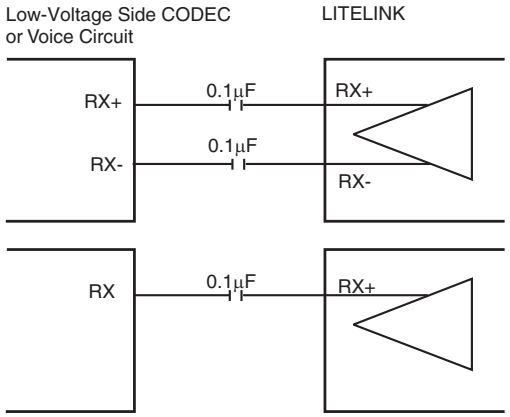
On the equipment's low voltage side of the barrier, the receive signal is converted by a photodiode into a photocurrent. The photocurrent, a linear representation of the receive signal, is amplified and converted to a differential voltage output on RX+ and RX-.

Variations in gain are controlled to within ±0.4 dB by factory gain trim, which sets the output to unity gain.

To accommodate single-supply operation, LITELINK includes a small DC bias on the RX outputs of 1.0V_{DC}. Most applications should AC couple the RX outputs as shown in Figure 5.

LITELINK may be used for differential or single-ended output as shown in Figure 5. Single-ended use will produce 6 dB less signal output amplitude. Do not exceed 0 dBm into 600 Ω (2.2 V_{P-P}) signal input with the standard application circuit. See application note AN-157, **Increased LITELINK III Transmit Power** for more information.

Figure 5. Differential and Single-ended Receive Path Connections to LITELINK



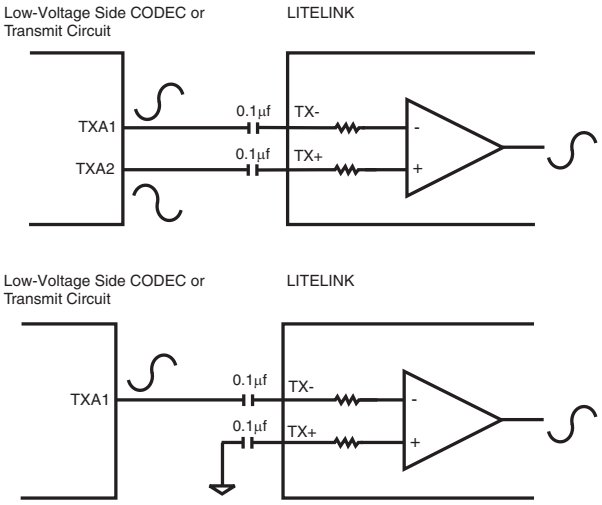
3.3.2 Transmit Signal Path

Connect transmit signals from the low-voltage side equipment to the TX+ and TX- pins of LITELINK. Do not exceed a signal level of 0 dBm in 600 Ω (or 2.2 V_{P-P}). Differential transmit signals are converted to single-ended signals in LITELINK. The signal is coupled to the transmit photodiode amplifier in a similar manner to the receive path. See application note AN-157, **Increased LITELINK III Transmit Power** for more information.

The output of the photodiode amplifier is coupled to a voltage-to-current converter via a transconductance stage where the transmit signal modulates the telephone line loop current. As in the receive path, gain is set to unity at the factory, limiting insertion loss variation to ±0.4 dB.

Differential and single-ended transmit signals into LITELINK should not exceed a signal level of 0 dBm referenced to 600 Ω (or 2.2 V_{P-P}). For output power levels above 0dBm consult the application note AN-157, **Increased LITELINK III Transmit Power** for more information.

Figure 6. Differential and Single-ended Transmit Path Connections to LITELINK



3.4 Start-up Requirements

$\overline{OH}$ must be de-asserted (set logic high) once after power-up for at least 50ms to transfer internal gain trim values within LITELINK. This would be normal operation in most applications. Failure to comply with this requirement will result in transmission gain errors and possibly distortion.

3.5 DC Characteristics

The CPC5620 and CPC5621 are designed for worldwide application, including use under the requirements of TBR-21. The ZDC, DCS1, and DCS2 pins control the VI slope characteristics of LITELINK. Selecting appropriate resistor values for R_{ZDC} (R16) and R_{DCS} (R15) in the provided application circuits assure compliance with DC requirements.

3.5.1 Setting a Current Limit

LITELINK includes a telephone line current limit feature that is selectable by choosing the desired value for R_{ZDC} (R16) using the following formula:

$$I_{CL}Amps = \frac{1V}{R_{ZDC}} + 0.008A$$

Clare recommends using 8.2 Ω for R_{ZDC} for most applications, limiting telephone line current to 130 mA.

Whether using the recommended value above or when setting R_{ZDC} higher for a lower loop current limit refer to the guidelines for FET thermal management provided in AN-146, **Guidelines for Effective LITELINK Designs**.

3.6 AC Characteristics

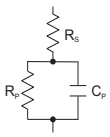
3.6.1 Resistive Termination Applications

North American and Japanese telephone line AC termination requirements are met with a resistive 600 Ω AC termination. Receive termination is applied to the LITELINK ZNT pin (pin 29) as a 301 Ω resistor, R_{ZNT} (R10).

3.6.2 Reactive Termination Applications

Many countries use a single-pole complex impedance to model the telephone network transmission line characteristic impedance as shown in the table below.

Line Impedance Model

		Australia	China	TBR 21
	R_S	220 Ω	200 Ω	270 Ω
	R_P	820 Ω	680 Ω	750 Ω
	C_P	120 nF	100 nF	150 nF

Proper gain and termination impedance circuits for a complex impedance requires the use of complex network on ZNT as shown in the **"Reactive Termination Application Circuit Schematic" on page 8**.

3.6.3 Mode Pin Usage

Assert the $\overline{\text{MODE}}$ pin low to introduce a 7 dB pad into the transmit path and add 7 dB of gain to the receive path. These changes compensate for the gain changes made to the transmit and receive paths in reactive termination implementations.

Insertion loss with $\overline{\text{MODE}}$ de-asserted and the resistive termination application circuit is 0 dB. Insertion loss with the reactive termination application circuit and $\overline{\text{MODE}}$ asserted is also 0 dB.

4. Regulatory Information

LITELINK III can be used to build products that comply with the requirements of TIA/EIA/IS-968 (formerly FCC part 68), FCC part 15B, TBR-21, EN60950, UL1950, EN55022B, IEC950/IEC60950, CISPR22B, EN55024, and many other standards. LITELINK provides supplementary isolation. Metallic surge requirements are met through the inclusion of a Sidactor in the application circuit. Longitudinal surge protection is provided by LITELINK's optical barrier technology and the use of high-voltage components in the application circuit as needed.

The information provided in this document is intended to inform the equipment designer but it is not sufficient to assure proper system design or regulatory compliance. Since it is the equipment manufacturer's responsibility to have their equipment properly designed to conform to all relevant regulations, designers using LITELINK are advised to carefully verify that their end-product design complies with all applicable safety, EMC, and other relevant standards and regulations. Semiconductor components are not rated to withstand electrical overstress or electro-static discharges resulting from inadequate protection measures at the board or system level.

5. LITELINK Design Resources

The Clare, Inc. web site has a wealth of information useful for designing with LITELINK, including application notes and reference designs that already meet all applicable regulatory requirements. See the following links:

LITELINK datasheets and reference designs

Application note AN-117 **Customize Caller ID Gain and Ring Detect Voltage Threshold**

Application note AN-146, **Guidelines for Effective LITELINK Designs**

Application note AN-152 **LITELINK II to LITELINK III Design Conversion**

Application note AN-155 **Understanding LITELINK Display Feature Signal Routing and Applications**

6. LITELINK Performance

The following graphs show LITELINK performance using the North American application circuit shown in this data sheet.

Figure 7. Receive Frequency Response at RX

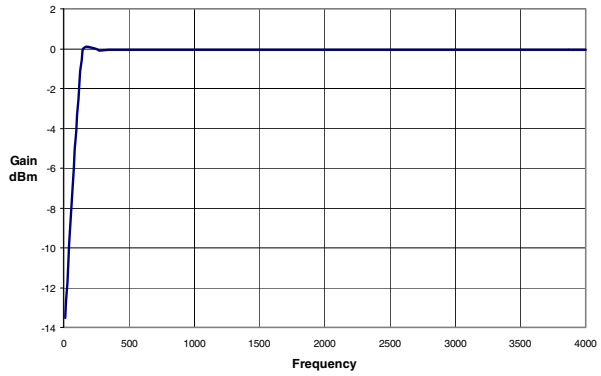


Figure 8. Transmit Frequency Response at TX

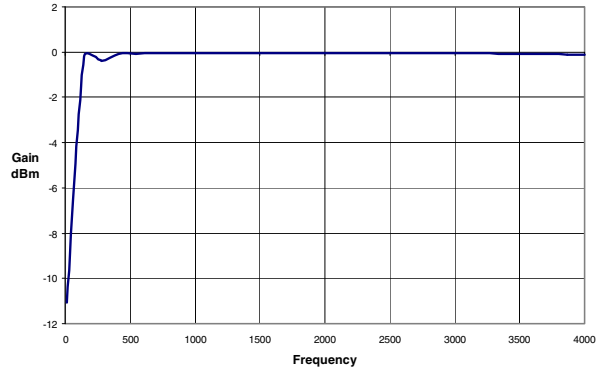


Figure 9. Receive THD on RX

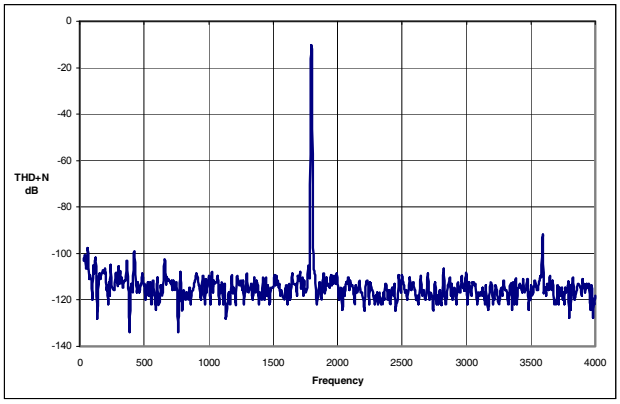


Figure 10.Transmit THD on Tip and Ring

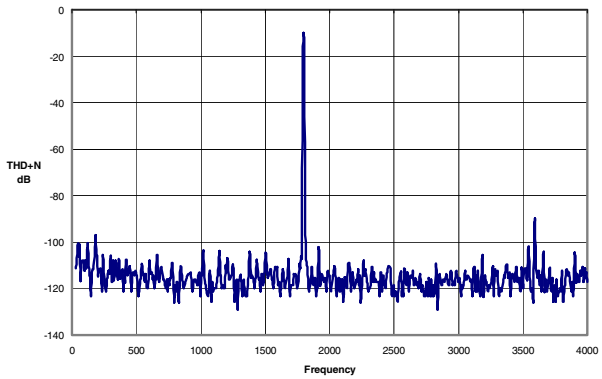


Figure 11.Transhybrid Loss

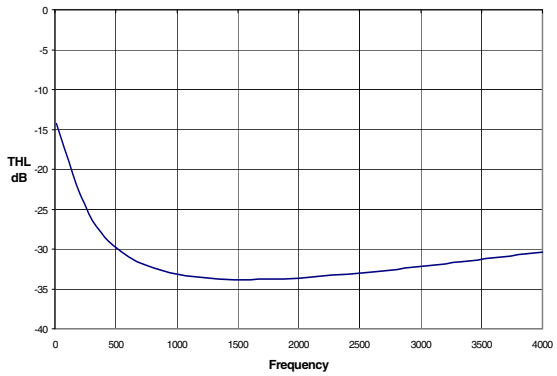


Figure 12.Return Loss

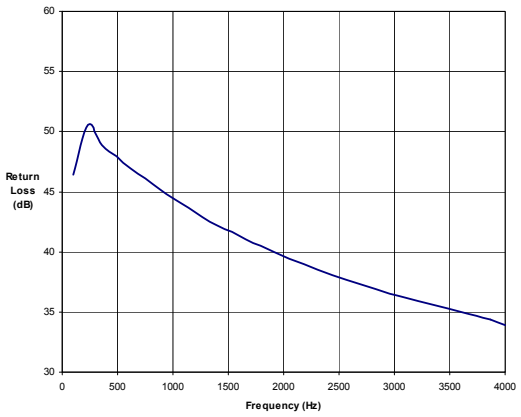


Figure 13.Snoop Circuit Frequency Response

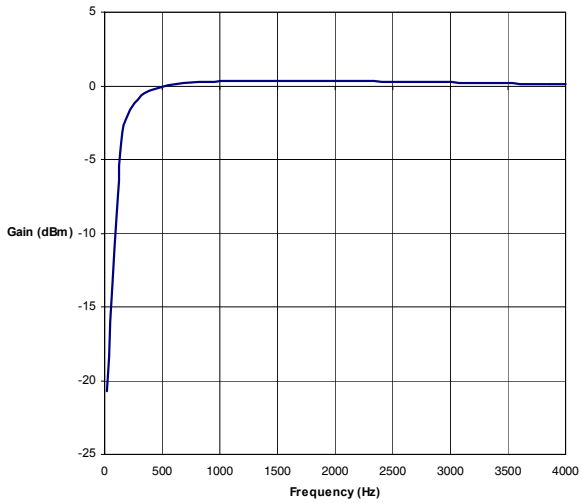


Figure 14.Snoop Circuit THD + N

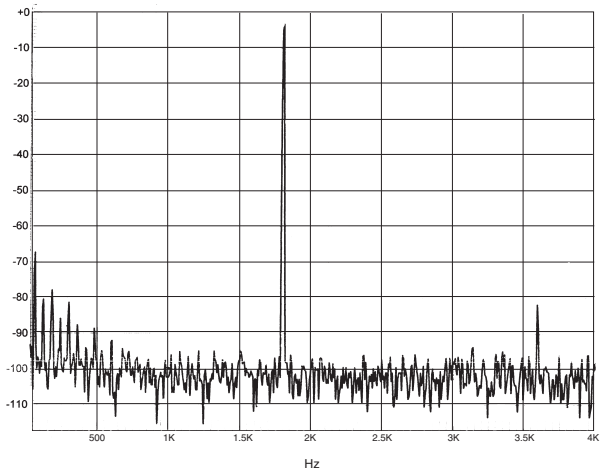
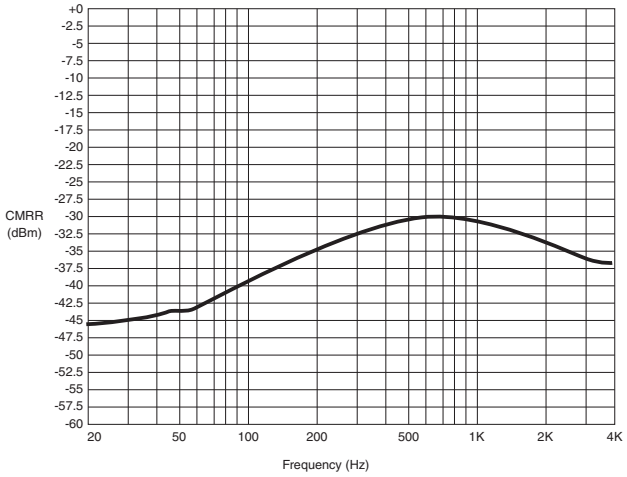


Figure 15.Snoop Circuit Common Mode Rejection



7. Manufacturing Information

7.1 Mechanical Dimensions

Figure 16. Dimensions

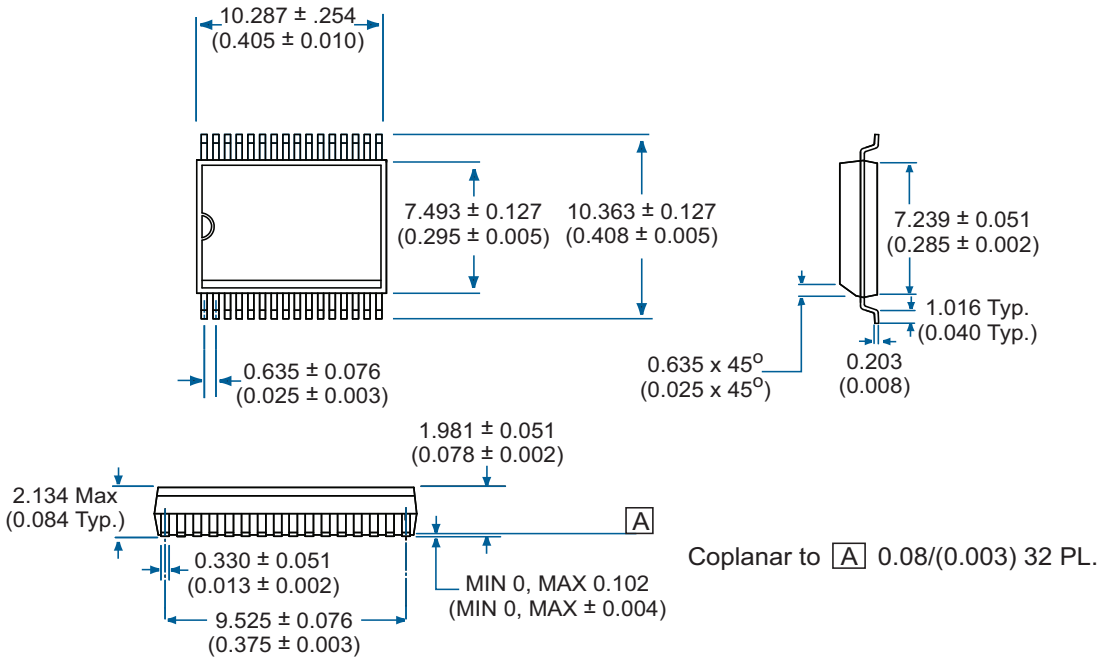
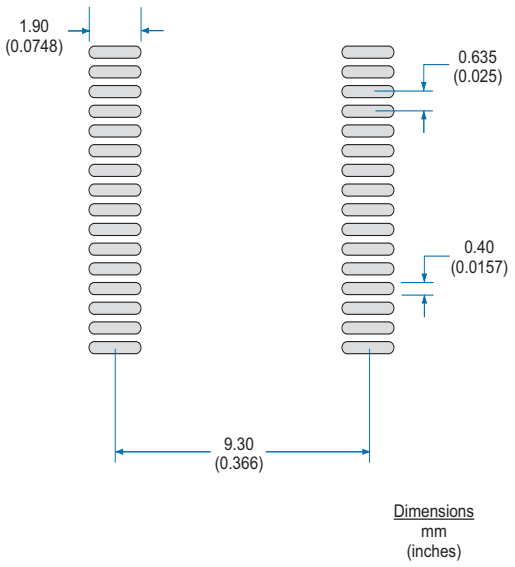


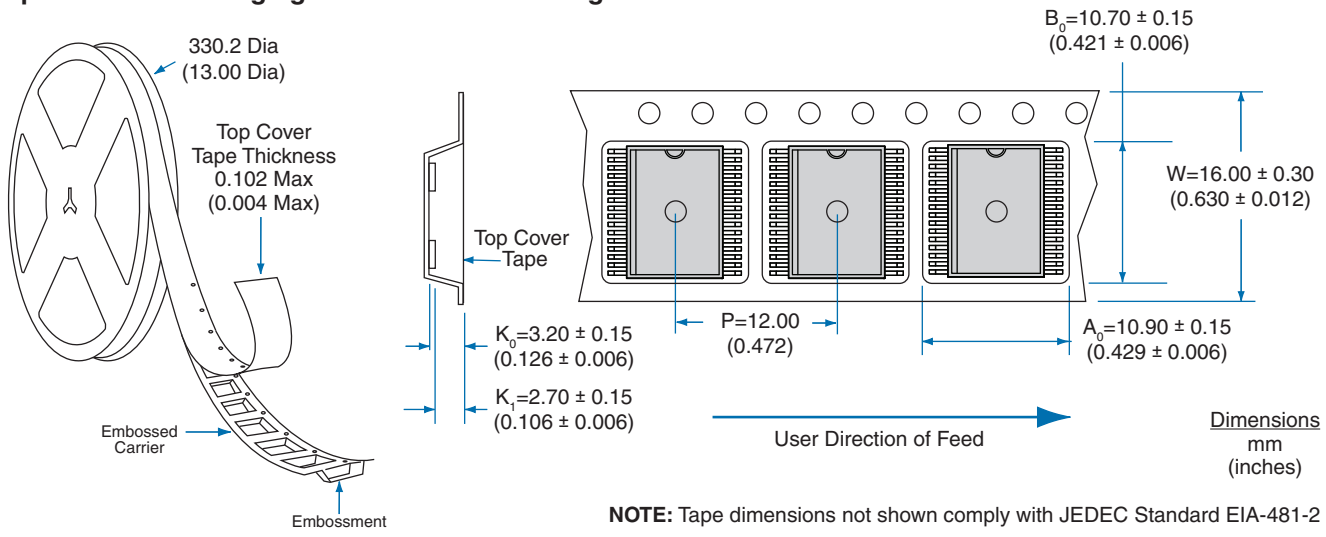
Figure 17. Recommended Printed Circuit Board Layout



7.2 Tape and Reel Packaging

Figure 18. Tape and Reel Dimensions

Tape and Reel Packaging for 32-Pin SOIC Package



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

7.3 Soldering

7.3.1 Moisture Reflow Sensitivity

Clare has characterized the moisture reflow sensitivity of this package, and has determined that this component must be handled in accordance with IPC/JEDEC standard J-STD-033 moisture sensitivity level (MSL), level 3 classification.

7.3.2 Reflow Profile

For proper assembly, the component must be processed in accordance with the current revision of IPC/JEDEC standard J-STD-020. Failure to follow the recommended guidelines may cause permanent damage to the device resulting in impaired performance and/or a reduced lifetime expectancy.

7.4 Washing

Clare does not recommend ultrasonic cleaning or the use of chlorinated solvents.

For additional information please visit www.clare.com

Specification: DS-CPC5620/CPC5621 - R04