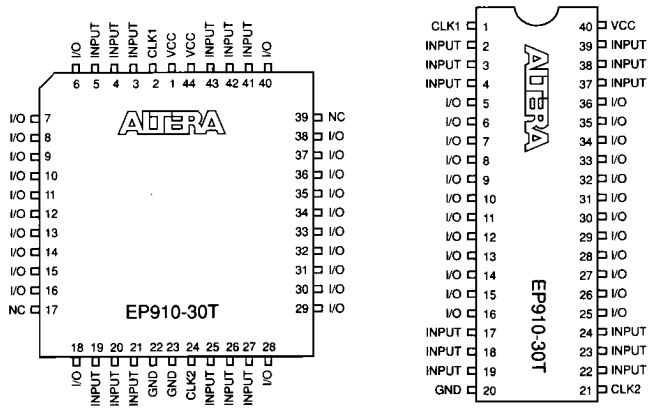
Features

- High-performance, 24-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} = 30 ns
  - Counter frequencies up to 33 MHz
  - Pipelined data rates up to 41 MHz
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- Pin-, function-, and programming file-compatible with Altera's EP910 and EP910A EPLDs
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Available in low-cost, one-time-programmable (OTP) plastic packages (See Figure 26):
  - 44-pin J-lead chip carrier (PLCC)
  - 40-pin dual in-line package (PDIP)

Figure 26. EP910T Package Pin-Out Diagrams

Package outlines not drawn to scale.



44-Pin J-Lead 40-Pin DIP

General Description

Altera's EP910T EPLD is a low-cost, high-performance version of the EP910 device. The EP910T operates in a turbo mode that is optimized for high-speed applications. The Turbo Bit in the device, which is preset at the factory, is permanently turned on. For information on EP910T architecture, refer to Figure 22 earlier in this data sheet.

Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		–250	250	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1200	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time	*Note (2)*		100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10		10	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load, *Note (5)*		80	115	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Note (5)*		80	115	mA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (4)*

			EP910-30T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		30	ns
t_{PD2}	I/O input to non-registered output			33	ns
t_{PZX}	Input to output enable			30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (7)*		30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		33	ns
t_{IO}	I/O input pad and buffer delay			3	ns

Global Clock Mode			EP910-30T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	41.7		MHz
t_{SU}	Input setup time		24		ns
t_H	Input hold time		0		ns
t_{CH}	Clock high time		12		ns
t_{CL}	Clock low time		12		ns
t_{CO1}	Clock to output delay			18	ns
t_{CNT}	Minimum clock period			30	ns
f_{CNT}	Internal maximum frequency	*Note (5)*	33.3		MHz

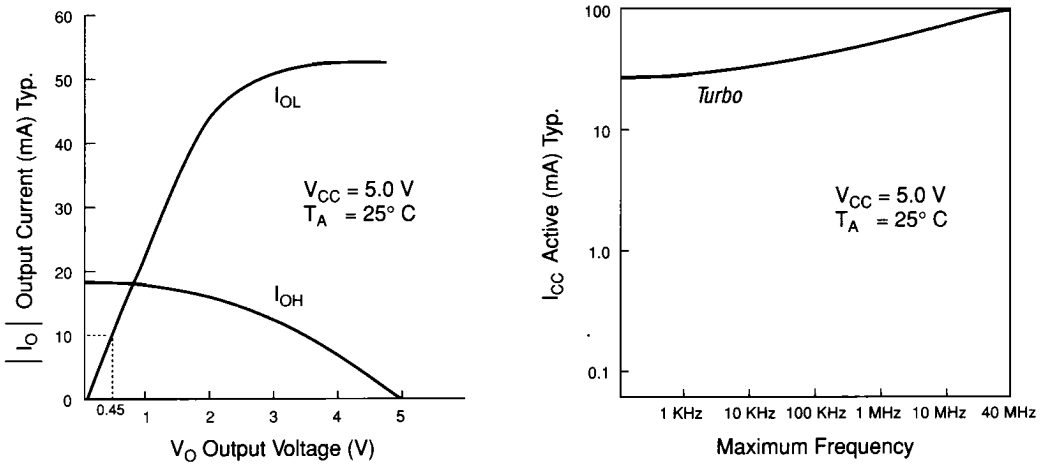
Array Clock Mode			EP910-30T		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (8)*	33.3		MHz
t_{ASU}	Input setup time		10		ns
t_{AH}	Input hold time		15		ns
t_{ACH}	Clock high time		15		ns
t_{ACL}	Clock low time		15		ns
t_{ACO1}	Clock to output delay			33	ns
t_{ACNT}	Minimum clock period			30	ns
f_{ACNT}	Internal maximum frequency	*Note (5)*	33.3		MHz

Notes to tables:

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) For all Clocks: t_R and t_F = 100 ns.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
(5) Measured with a device programmed as a 24-bit counter. I_{CC} measured at 0° C.
(6) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. Pin 21 (high-voltage pin during programming) has a maximum capacitance of 60 pF.
(7) Sample-tested only for an output change of 500 mV.
(8) The f_{MAX} values represent the highest frequency for pipelined data.

Figure 27 shows the maximum output drive characteristics of EP910T I/O pins and typical supply (I_{CC}) current versus frequency for the EP910T EPLD.

Figure 27. EP910T Maximum Output Drive Characteristics & I_{CC} vs. Frequency



Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EP910-30T
Industrial Temp.	(–40° C to 85° C)	Consult factory
Military Temp.	(–55° C to 125° C)	Consult factory