

# AN11219

## Programming the PCA200x family of watch ICs

Rev. 1 — 4 September 2012

Application note

### Document information

Info	Content
<b>Keywords</b>	PCA2000, PCA2001, PCA2002, PCA2003, Calibration
<b>Abstract</b>	The PCA200x are CMOS integrated circuits for battery operated wrist watches with a 32 kHz quartz crystal as the timing element and a bipolar 1 Hz stepping motor. The quartz crystal oscillator and the frequency divider are optimized for minimum power consumption. A timing accuracy of 1 ppm is achieved with a programmable, digital frequency adjustment. This document describes how the calibration can be performed.



## Revision history

Rev	Date	Description
v.1	20120904	Initial version

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## 1. Introduction

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The PCA200x are CMOS integrated circuits for battery operated wrist watches with a 32 kHz quartz crystal as the timing element and a bipolar 1 Hz stepping motor. The quartz crystal oscillator and the frequency divider are optimized for minimum power consumption. A timing accuracy of 1 ppm is achieved with a programmable, digital frequency adjustment.

To obtain the minimum overall power consumption for the watch, an automatic motor pulse adaptation function is provided. The circuit supplies only the minimum drive current, which is necessary to ensure a correct motor step. Changing the drive current of the motor is achieved by chopping the motor pulse with a variable duty cycle. The pulse width and the range of the variable duty cycle can be programmed to suit different types of motors.

A pin RESET is provided which can be used for stopping the motor, for accurate time setting, and for accelerated testing of the watch.

The PCA2000 has a battery End Of Life (EOL) warning function. If the battery voltage drops below the EOL threshold voltage (which can be programmed for silver oxide or lithium batteries), the motor steps change from one pulse per second to a burst of four pulses every 4 seconds. The EOL function is not present in PCA2001, PCA2002 and PCA2003.

## 2. Functional description

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### 2.1 Motor pulse

The motor driver delivers pulses with an alternating polarity. The output waveform across the motor terminals is illustrated in [Figure 1](#). Between the motor pulses, both terminals are connected to  $V_{DD}$  which means that the motor is short-circuit.

The following parameters can be programmed in a One Time Programmable (OTP) memory:

- Output periods of 1 s, 5 s, 10 s, 20 s, and 30 s
- Pulse width ( $t_p$ ) between 0.98 ms and 7.8 ms in steps of 0.98 ms
- Full or chopped (75 %) output pulse
- Pulse stretching: An enlargement pulse added to the primary motor pulse. This enlargement pulse has a duty cycle of 25 % and a width which is twice the programmed motor pulse width. The repetition period for the chopping pattern is 0.98 ms. [Figure 2](#) shows an example for a 3.9 ms pulse.

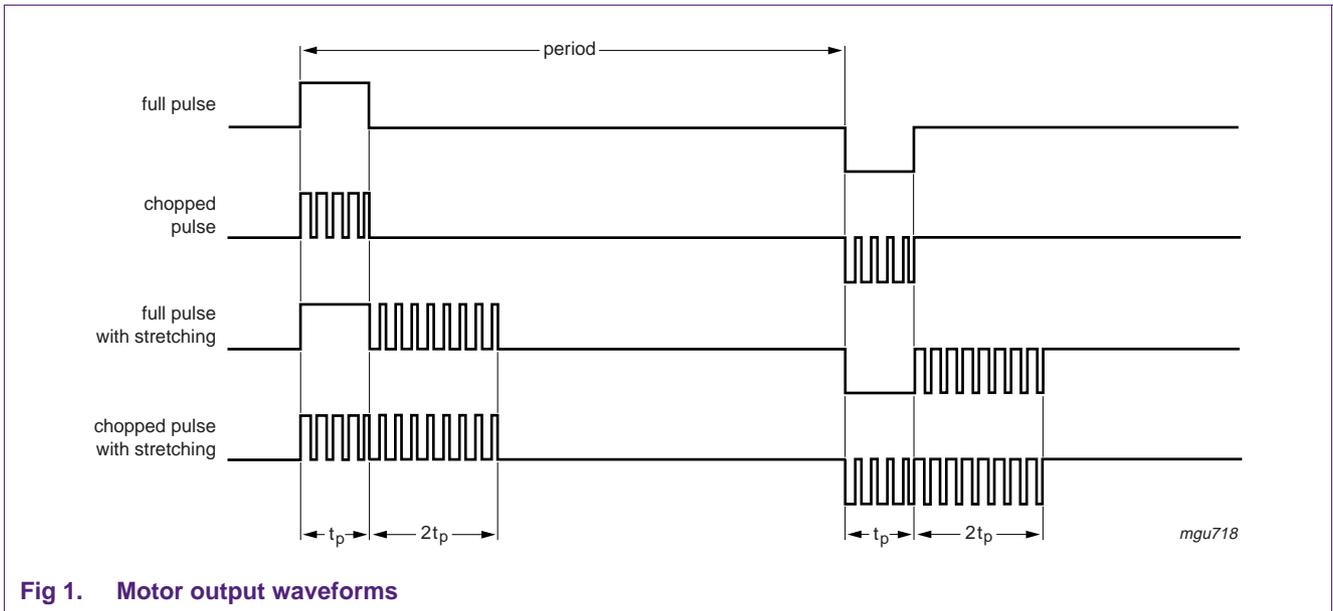


Fig 1. Motor output waveforms

Figure 2 shows an example for a 3.9 ms pulse.

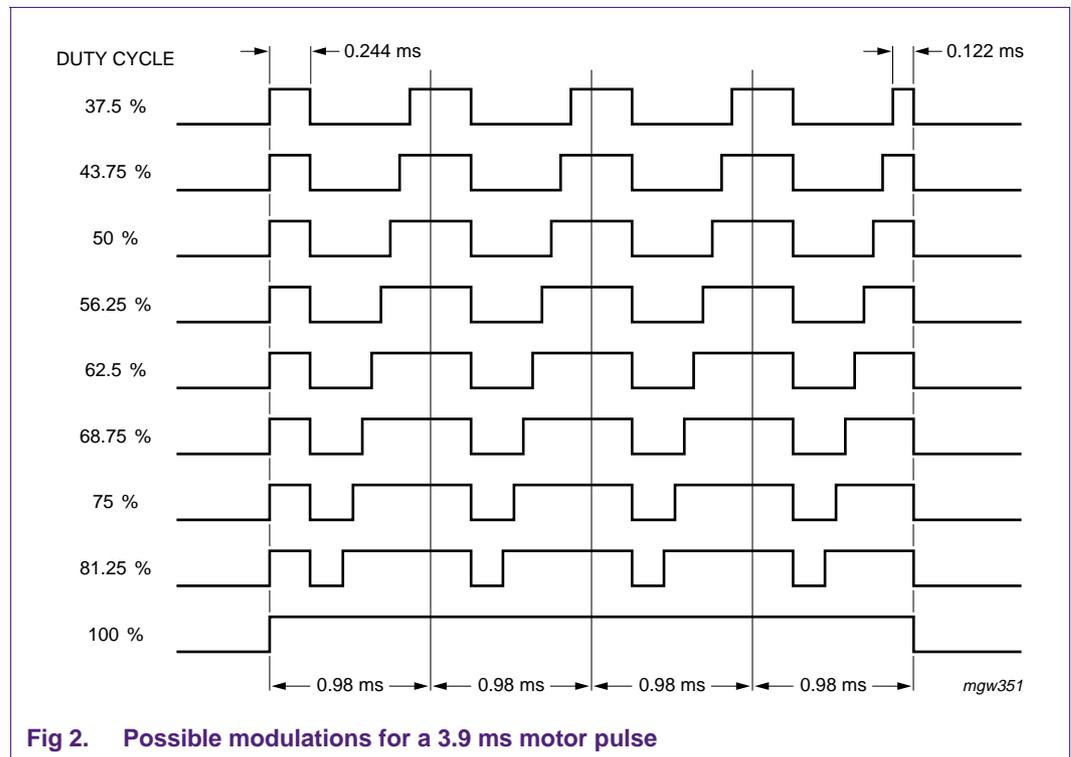


Fig 2. Possible modulations for a 3.9 ms motor pulse

## 2.2 Time calibration

The quartz oscillator frequency would be exactly 32.768 kHz if the oscillator load capacitance would fit exactly the requirements of the crystal. The quartz oscillator frequency is internally divided by 1024 and is nominally

$f_{nom} = 32.768 \text{ kHz} / 1024 = 32 \text{ Hz}$ . This frequency can be measured at pin RESET as a square wave signal ( $f_o$ ).

The quartz crystal oscillator has an integrated capacitance of 5.2 pF, which is lower than the specified load capacitance ( $C_L$ ) of 8.2 pF for the quartz crystal. Therefore, the oscillator frequency is typically 60 ppm higher than 32.768 kHz (corresponding to about 3 minutes too fast per month). This positive frequency offset is compensated by removing the appropriate number of 8192 Hz pulses in the divider chain (maximum 127 pulses), every 1 or 2 minutes. The time correction is given in [Table 1](#).

**Table 1. Time calibration**

Calibration period	Correction per step (n = 1)		Correction per step (n = 127)	
	ppm	seconds per day	ppm	seconds per day
1 minute	2.03	0.176	258	22.3
2 minutes	1.017	0.088	129	11.15

After measuring the effective oscillator frequency, the number of correction pulses must be calculated and stored together with the calibration period in the OTP memory (see [Section 3 on page 12](#)).

Before programming the calibration word A (state 3) which contains the number of 8192 Hz pulses to be removed and the calibration period, first the motor pulse parameters must be programmed using word B (state 4).

Since the programming is done using an OTP, a register bit can be changed from 0 to 1, but once programmed to 1 it can't be set back to 0.

An automatic test sequence might have two phases:

- Program the IC in accordance with the mechanism used, followed by calibration
- Verify that the IC has been correctly programmed (optional for large series production)

## 2.3 Reset

At pin RESET an output signal with the frequency  $f_o$  is provided. Connecting pin RESET to  $V_{DD}$  stops the motor drive and opens the motor switches. After releasing pin RESET, the first motor pulse is generated exactly one period later with the opposite polarity to the last pulse before stopping. The debounce time for the reset function is between 31 ms and 62 ms.

Connecting pin RESET to  $V_{SS}$  activates the test mode. In this mode the motor output frequency is 32 Hz, which can be used to test the mechanical function of the watch.

## 2.4 Programming possibilities

### 2.4.1 PCA2000 and PCA2001

The programming data is organized in an array of four 8-bit words (see [Table 2](#)):

**Word A** — for the time calibration,

**Words B and C** — for setting of the motor pulses and

**Word D** — for the type recognition.

**Table 2. PCA2000 and PCA2001 register overview**

Word	Bit							
	1	2	3	4	5	6	7	8
A	number of 8192 Hz pulses to be removed							calibration period
B	lowest stage: duty cycle		number of driving stages		highest stage: duty cycle	pulse stretching	factory test bits	
C	pulse width			maximum time delay between positive and negative detection pulses			EOL voltage	factory test bit
D	type				factory test bits			

**Table 3. PCA2000 and PCA2001 description of word A bits**

Bit	Value	Description
<b>Inhibition time</b>		
1 to 7	-	adjust the number of the 8192 Hz pulses to be removed; bit 1 is the MSB and bit 7 is the LSB
<b>Calibration period</b>		
8	0	1 minute
	1	2 minutes

**Table 4. PCA2000 and PCA2001 description of word B bits**

Bit	Value	Description
<b>Duty cycle lowest driving stage</b>		
1 to 2	00	37.5 %
	01	43.75 %
	10	50 %
	11	56.25 %
<b>Number of driving stages</b>		
3 to 4	00	3
	01	4
	10	5
	11	<a href="#">6<sup>[1]</sup></a>
<b>Duty cycle highest driving stage</b>		
5	0	75 % <sup>[2]</sup>
	1	100 %
<b>Pulse stretching</b>		

Table 4. PCA2000 and PCA2001 description of word B bits ...continued

Bit	Value	Description
6	0	no pulse stretching
	1	pulse of $2 \times t_p$ and duty cycle of 25 % are added
<b>Factory test bits</b>		
7 to 8	-	-

[1] Including the highest driving stage, which one has no motor step detection.

[2] If the maximum duty cycle of 75 % is selected, not all programming combinations are possible since the second highest level must be smaller than the highest driving level.

Table 5. PCA2000 and PCA2001 description of word C bits

Bit	Value	Description
<b>Pulse width <math>t_p</math></b>		
1 to 3	000	0.98 ms
	001	1.95 ms
	010	2.93 ms
	011	3.91 ms
	100	4.88 ms
	101	5.86 ms
	110	6.84 ms
	111	7.81 ms
<b>Time delay <math>t_{d(max)}</math> [1]</b>		
4 to 6	000	3.91 ms
	001	4.88 ms
	010	5.86 ms
	011	6.84 ms
	100	7.81 ms
	101	8.79 ms
	110	9.77 ms
	111	10.74 ms
<b>EOL voltage of the battery</b>		
7	0	1.38 V (silver-oxide)
	1	2.5 V (lithium)
<b>Factory test bit</b>		
8	-	-

[1] Between positive and negative detection pulses.

### 2.4.2 PCA2002

The programming data is organized in an array of four 8-bit words (see [Table 6](#)).

**Word A** — for the time calibration,

**Word B** — for setting of the motor pulses,

**Word C** — is not used with PCA2002 and

**Word D** — for the type recognition.

**Table 6. PCA2002 register overview**

Word	Bit							
	1	2	3	4	5	6	7	8
A	number of 8192 Hz pulses to be removed							calibration period
B	pulse width			output period			duty cycle	pulse stretching
C	-	-	-	-	-	-	-	-
D	type				factory test bit	-	-	-

There are four words, only words A and B can be programmed. The meaning of the individual bits is given in [Table 7](#) and [Table 8](#).

Table 7. PCA2002 description of word A bits

Bit	Value	Description
<b>Inhibit time</b>		
1 to 7	-	adjust the number of the 8192 Hz pulses to be removed; bit 1 is the MSB and bit 7 is the LSB
<b>Calibration period</b>		
8	0	1 minute
	1	2 minutes

Table 8. PCA2002 description of word B bits

Bit	Value	Description
<b>Pulse width <math>t_p</math> (ms)</b>		
1 to 3	000	0.98 ms
	001	1.95 ms
	010	2.93 ms
	011	3.91 ms
	100	4.88 ms
	101	5.86 ms
	110	6.84 ms
	111	7.81 ms
<b>Output period (s)</b>		
4 to 6	000	1
	001	5
	010	10
	011	20
	100	30
<b>Duty cycle of motor pulse</b>		
7	0	75 %
	1	100 %
<b>Pulse stretching</b>		
8	0	no pulse stretching
	1	a pulse width of $2 \times t_p$ and a duty factor of 25 % are added

### 2.4.3 PCA2003

The programming data is organized in an array of four 8-bit words (see [Table 9](#)):

**Word A** — for the time calibration,

**Words B and C** — for setting of the motor pulses and

**Word D** — for the type recognition.

Table 9. PCA2003 register overview

Word	Bit							
	1	2	3	4	5	6	7	8
A	number of 8192 Hz pulses to be removed							calibration period
B	lowest stage: duty cycle		number of driving stages		highest stage: duty cycle	pulse stretching	output period	
C	pulse width			maximum time delay between positive and negative detection pulses			output period	factory test bit
D	type				factory test bits			

Table 10. PCA2003 description of word A bits

Bit	Value	Description
<b>Inhibition time</b>		
1 to 7	-	adjust the number of the 8192 Hz pulses to be removed; bit 1 is the MSB and bit 7 is the LSB
<b>Calibration period</b>		
8	0	1 minute
	1	2 minutes

Table 11. PCA2003 description of word B bits

Bit	Value	Description
<b>Duty cycle lowest driving stage</b>		
1 to 2	00	37.5 %
	01	43.75 %
	10	50 %
	11	56.25 %
<b>Number of driving stages</b>		
3 to 4	00	3
	01	4
	10	5
	11	6 <sup>[1]</sup>
<b>Duty cycle highest driving stage</b>		
5	0	75 % <sup>[2]</sup>
	1	100 %
<b>Pulse stretching</b>		
6	0	no pulse stretching
	1	pulse of $2 \times t_p$ and duty cycle of 25 % are added
<b>Output period</b>		
7 to 8	00	1 s
	01	5 s
	10	10 s
	11	20 s

- [1] Including the highest driving stage, which one has no motor step detection.
- [2] If the maximum duty cycle of 75 % is selected, not all programming combinations are possible since the second highest level must be smaller than the highest driving level.

Table 12. PCA2003 description of word C bits

Bit	Value	Description
<b>Pulse width <math>t_p</math></b>		
1 to 3	000	0.98 ms
	001	1.95 ms
	010	2.93 ms
	011	3.91 ms
	100	4.88 ms
	101	5.86 ms
	110	6.84 ms
	111	7.81 ms
<b>Time delay <math>t_{d(max)}</math> <a href="#">[1]</a></b>		
4 to 6	000	3.91 ms
	001	4.88 ms
	010	5.86 ms
	011	6.84 ms
	100	7.81 ms
	101	8.79 ms
	110	9.77 ms
	111	10.74 ms
<b>Output period</b>		
7	0	bit 7 and 8 of word B active
	1	30 s, bit 7 and 8 of word B inactive
<b>Factory test bit</b>		
8	-	-

- [1] Between positive and negative detection pulses.

## 2.5 Type recognition

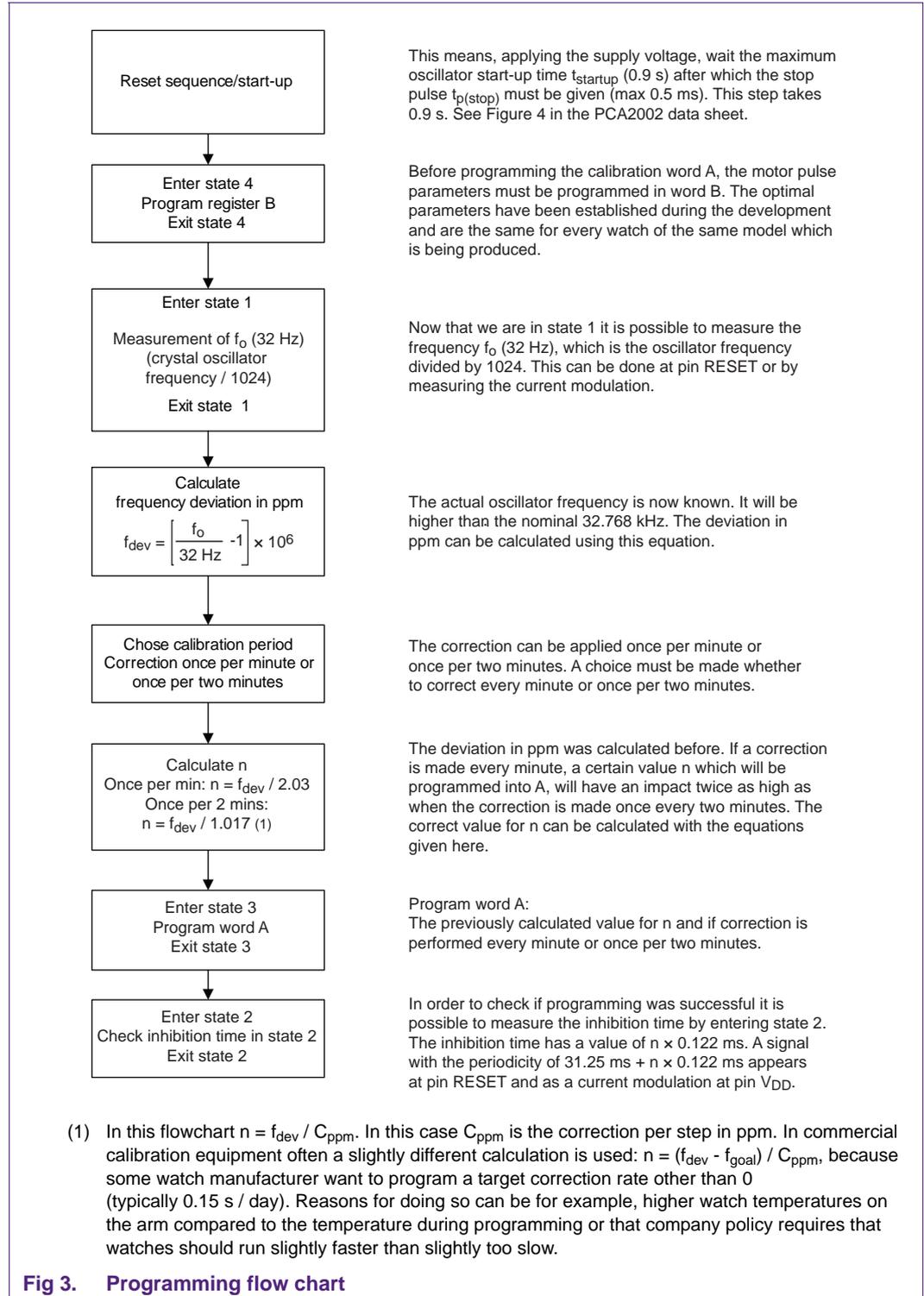
Byte D is read only and is to determine which type of the PCA200x family is used in a particular application.

Table 13. Description of word D bits

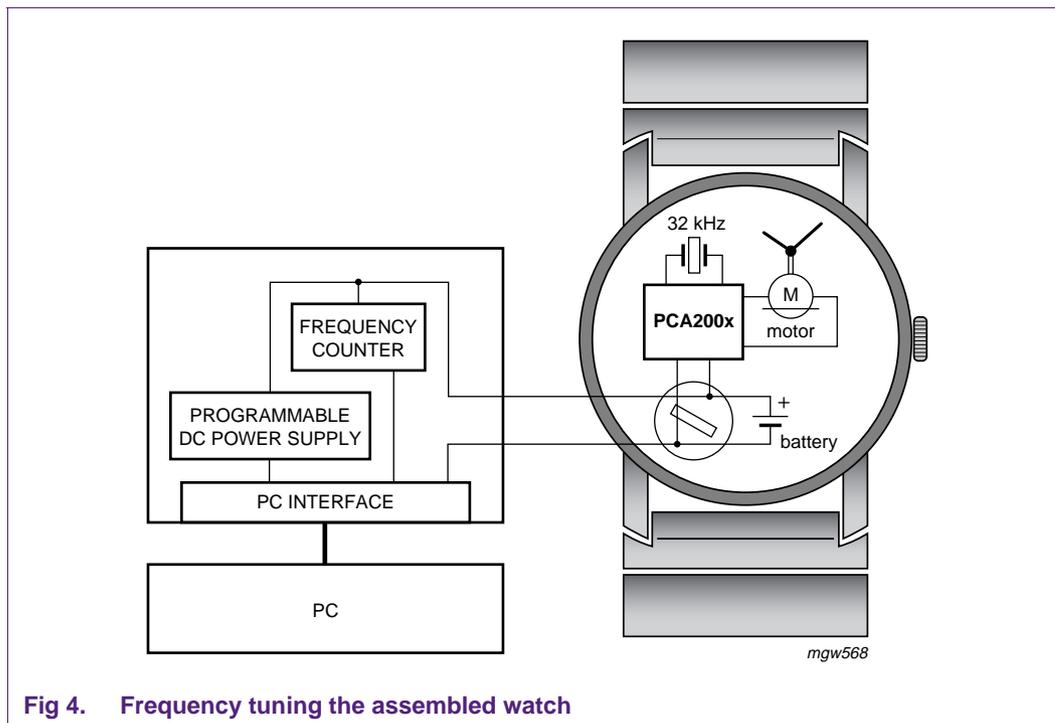
Bit	Value	Description
<b>Type recognition</b>		
1 to 4	0000	PCA2002
	1000	PCA2000
	0100	PCA2001
	1100	PCA2003

### 3. Programming procedure

The flow chart in [Figure 3](#) indicates the programming procedure of the PCA2002. Details are given in the description on the following pages.



For a watch, it is essential that the timing calibration can be made after the watch has been fully assembled. In this situation, the supply pins are often the only terminals which are still accessible. [Figure 4](#) shows the set-up for programming<sup>1</sup> the assembled watch.



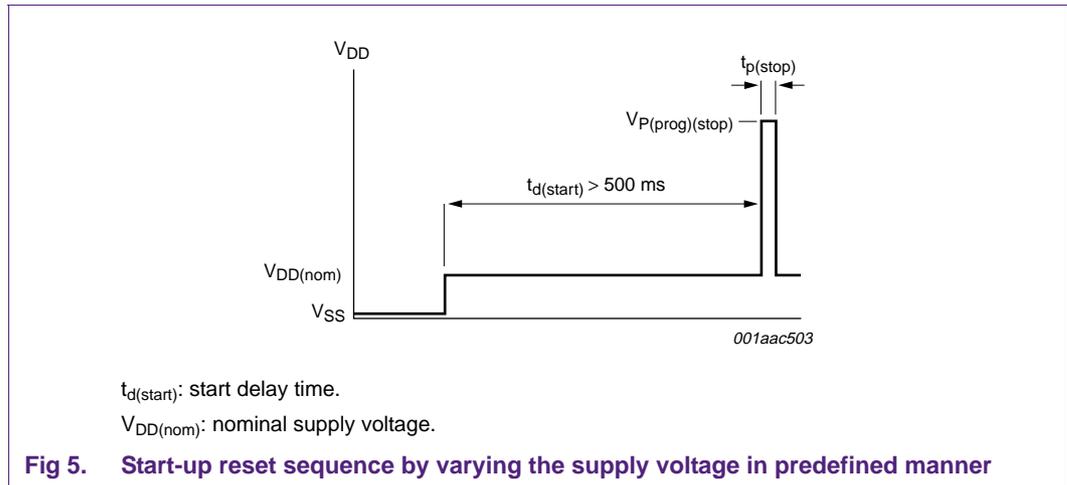
**Fig 4. Frequency tuning the assembled watch**

Executing a power-on-reset, writing to the OTP cells and performing the related functional checks is achieved in the PCA200x by modulating the supply voltage. The necessary control circuit consists basically of a voltage level detector, an instruction counter which determines the function to be performed and an 8-bit shift register, which allows programming the OTP cells of an 8-bit word in one step and which acts also as a data pointer for checking the OTP content.

In order to ensure that the oscillator starts up correctly after powering up the watch, a reset sequence must be executed. The reset sequence is given in [Figure 5](#).

**Important:** The programming procedure requires a stable oscillator, which means that a waiting time, determined by the start-up time of the oscillator, is necessary after power-up of the circuit. The maximum oscillator start-up time of the oscillator is 0.9 s. In [Figure 5](#) " $t_{d(start)} > 500 \text{ ms}$ " is indicated. In most cases this is enough but it may be necessary to reserve up to 900 ms for the oscillator start-up. This reset sequence is only required after power-up and not in between the various programming stages. That means that it is required just once during a normal programming procedure.

1. As far as NXP CWG knows, the two Swiss companies, Witschi and Femto, offer commercial programmers.



The control circuit consists of an instruction counter which determines the function to be performed and an 8-bit shift register, which allows programming the OTP cells of an 8-bit word in one step and which acts also as a data pointer for checking the OTP content. There are six different states. In a normal programming procedure, these states are not accessed in sequence from 1 to 6. The different states are:

- State 1** — measurement of  $f_0$  (32Hz), the oscillator frequency divided by 1024
- State 2** — measurement of the inhibition time
- State 3** — write/check word A
- State 4** — write/check word B
- State 5** — check word C (for PCA2002 don't care since no meaning)
- State 6** — check word D (type recognition)

Every instruction state is switched on with a programming start pulse,  $V_{P(prog)(start)}$  with duration  $t_{p(start)}$ . This is the only way to enter the programming mode. For details about voltage levels and duration of the various pulses, please refer to the data sheets. After this large pulse, an initial waiting time  $t_0$  is required. The programming instructions are then entered by modulating the supply voltage with small pulses (amplitude  $V_{P(mod)}$  and pulse width  $t_{mod}$ ). The first small pulse defines the start time, the following pulses perform three different functions depending on the time delay ( $t_d$ ) from the preceding pulse (see [Figure 6](#), [Figure 7](#), [Figure 8](#) and [Figure 9](#)):

- $t_d = t_1$  (0.7 ms) — increments the instruction counter
- $t_d = t_2$  (1.7 ms) — clocks the shift register with data = logic 0
- $t_d = t_3$  (2.7 ms) — clocks the shift register with data = logic 1

After the  $V_{P(prog)(start)}$  pulse, the instruction counter is in state 1 and the data shift register is cleared.

As mentioned above there is only one method to enter the programming mode, but there are two different methods to leave the programming mode:

1. The instruction stated ends with a second pulse to  $V_{P(prog)(stop)}$  or with the pulse to  $V_{store}$ .

2. If no pulse to  $V_{P(prog)(stop)}$  or  $V_{store}$  is given, the instruction states are terminated automatically two seconds after the last supply modulation pulse.

Examples are given below.

### 3.1 Enter state 4, program register B and exit state 4

Before programming the calibration word A, the motor pulse parameters must be programmed in word B. This means that state 4 is needed. The optimal parameters depend on the mechanism that is being used and during development of the watch the best settings for the mechanism must be established. These are then the same for every watch of the same model that is being produced.

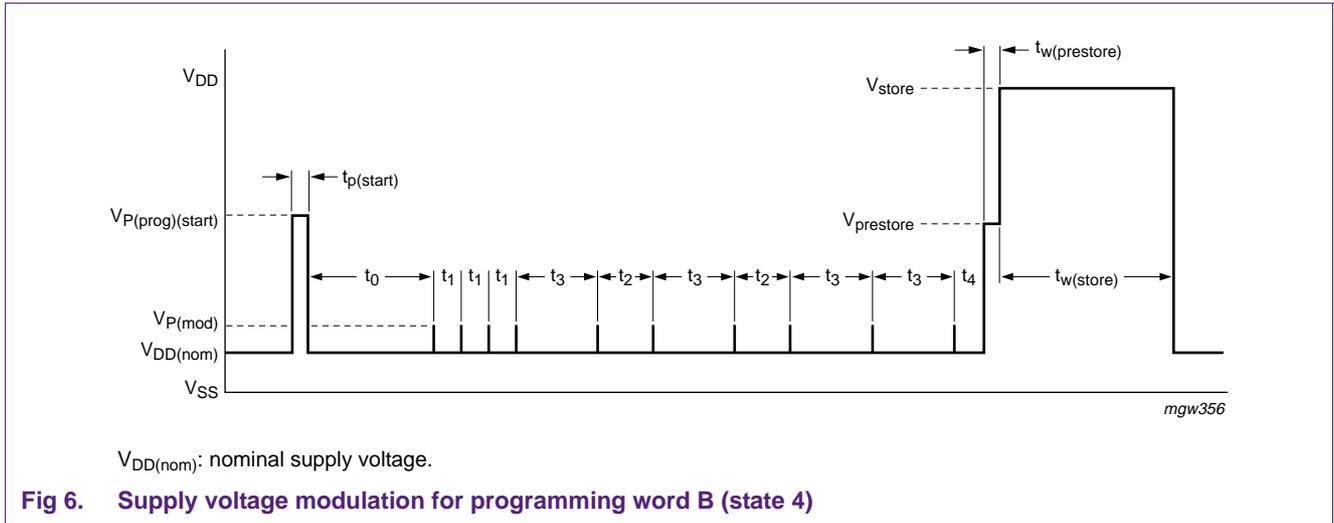
In general, in order to program a memory word (here memory word B), the following steps need to be performed:

1. Start with a  $V_{P(prog)(start)}$  pulse, wait for the time period  $t_0$  and then set the instruction counter to the word to be written ( $t_d = t_1$ ). After  $t_0$  the first small pulse puts the IC in state 1. Every consecutive waiting time  $t_d = t_1$  followed by a small pulse increases the state;
2. Enter the data to be stored into the shift register ( $t_d = t_2$  or  $t_3$ ), LSB first (bit 8) and MSB last (bit 1);
3. Applying the two-stage programming pulse  $V_{prestore}$  followed by  $V_{store}$  stores the word. The delay between the last data bit and the pre-store pulse  $V_{prestore}$  is  $t_d = t_4$ . Store the word by raising the supply voltage to  $V_{store}$ ; the delay between the last data bit and the store pulse is  $t_d$ .

The example below in [Figure 6](#) shows programming of  $B = 110101$  (the sequence is LSB first and MSB last)<sup>2</sup>. It performs the following functions:

- Start;
- Setting the instruction counter to state 4 (word B);
- Entering data word 110101 into the shift register (sequence: LSB first, MSB last);
- Writing the OTP cells for word B.

2. This example is only valid for PCA2000 and PCA2001; for PCA2002 the sequence would be 11001001, programming a pulse width of 6.8 ms, an output period of 10 s, a duty cycle of 75 % and a pulse stretching of 1.



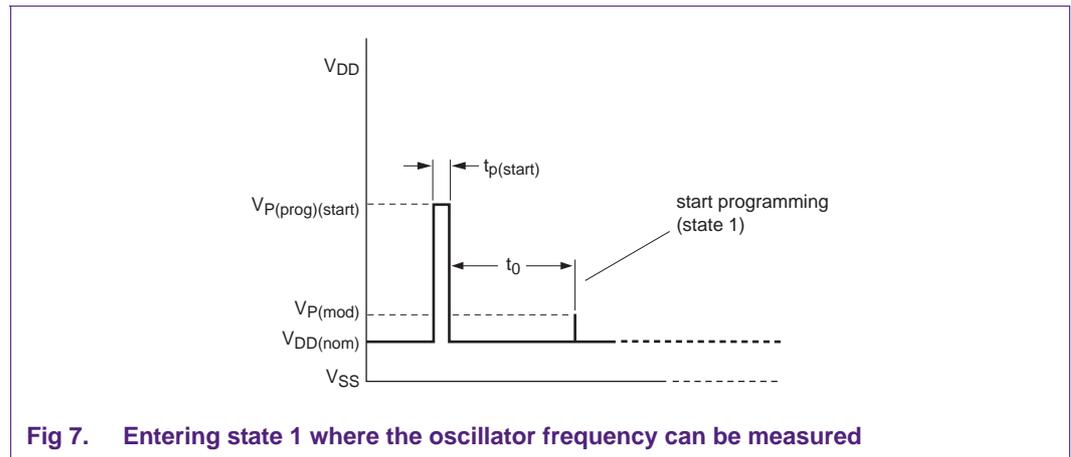
### 3.2 Enter state 1, measure the oscillator frequency and leave state 1

Now that the motor pulse parameters have been programmed, it is possible to calibrate the watch. This is done by first measuring the actual oscillator frequency. From there the required number of inhibition pulses can be calculated. In short, enter state 1, measure the frequency  $f_o$  (which is the oscillator frequency divided by 1024) and leave state 1. State 1 starts with a pulse to  $V_P$  and ends with a second pulse to  $V_P$  as indicated below.

In order to enter state 1 the following step needs to be performed:

1. Start with a  $V_{P(prog)(start)}$  pulse, wait for the time period  $t_0$  and then give a small pulse.

This is indicated in [Figure 7](#).



The frequency  $f_o$  can either be monitored directly at pin RESET or as a modulation of the supply current (a modulating resistor of 30 kΩ is connected between  $V_{DD}$  and  $V_{SS}$  when the signal at pin RESET is HIGH, increasing the supply current accordingly).

Leave state 1 by giving a pulse to  $V_{P(prog)(stop)}$ . If no such pulse is given, state 1 is left automatically two seconds after the last supply modulation pulse.

### 3.3 Calculate the frequency deviation of the oscillator in ppm, and the value of n

The actual oscillator frequency is now known. It was purposely set higher than 32.768 kHz. The frequency adjustment is made by introducing longer seconds at certain intervals (pulses from the quartz are inhibited at those intervals). During the inhibition sequence one 32 Hz-period at the pin RESET is increased by  $n \times 0.122$  ms. Here  $n$  is the number that is programmed in the OTP. The programmed inhibition time can later easily be measured in state 2, see [Section 3.5](#).

The frequency deviation in ppm can be calculated as follows:

$$f_{dev} = \left( \frac{f_o}{32 \text{ Hz}} - 1 \right) \times 10^6 \quad (1)$$

The correction can be applied once per minute or once per two minutes (calibration period). This is a choice that has to be made.

If a correction is made ever minute a certain value  $n$  which will be programmed into word A will have an impact twice as high as when the correction is made only once every two minutes. The correct value for  $n$  (the number of 8192 Hz pulses to be inhibited) can be calculated with the following formulas (see also [Table 1](#)):

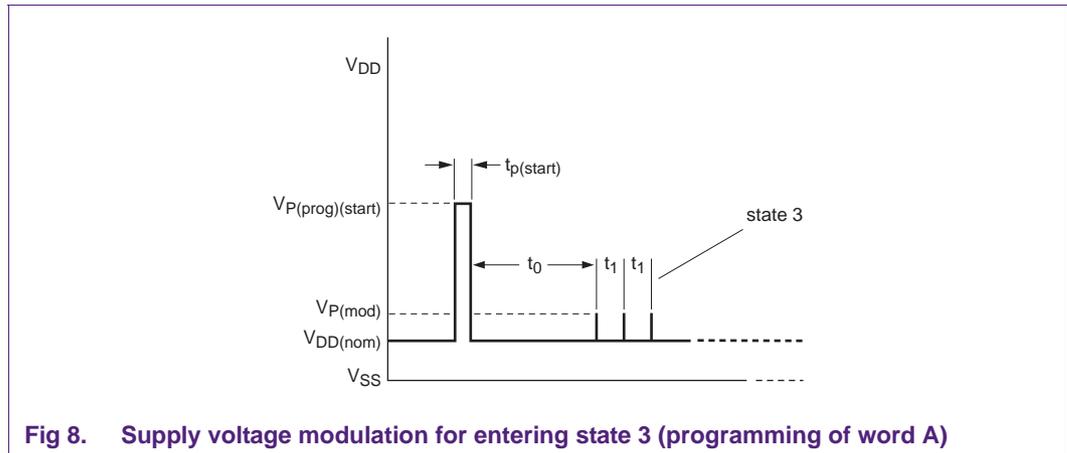
- Correction once per minute:  $n = f_{dev}/2.03$
- Correction once per two minutes:  $n = f_{dev}/1.017$

The calculated value  $n$  must be programmed into register A, together with the calibration period in the next step.

### 3.4 Enter state 3, program word A and leave state 3

In general, in order to program a memory word (here memory word A), the following steps need to be performed:

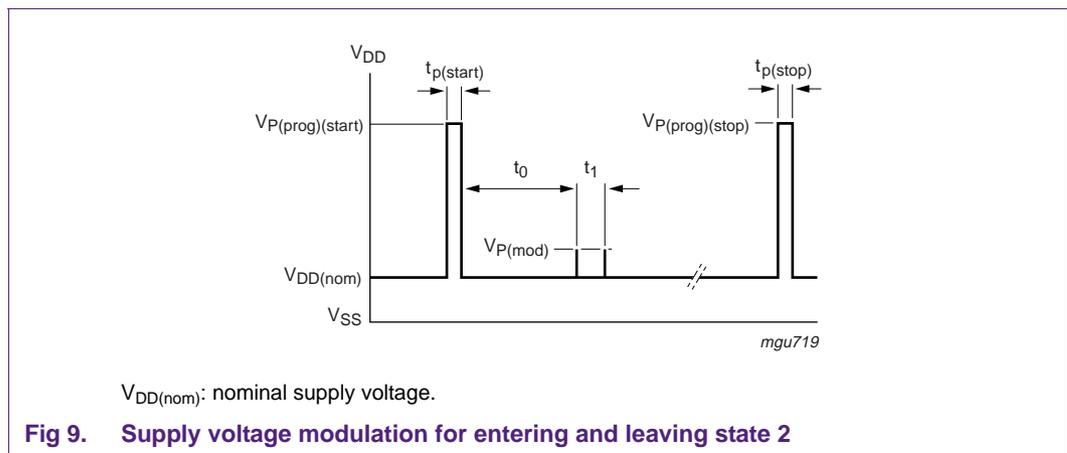
1. Start with a  $V_{P(prog)(start)}$  pulse, wait for the time period  $t_0$  and then set the instruction counter to the word to be written ( $t_d = t_1$ ). After  $t_0$  the first small pulse puts the IC in state 1. Every consecutive waiting time  $t_d = t_1$  followed by a small pulse increases the state;
2. Enter the data to be stored into the shift register ( $t_d = t_2$  or  $t_3$ ), LSB first (bit 8) and MSB last (bit 1);
3. Applying the two-stage programming pulse  $V_{prestore}$  followed by  $V_{store}$  stores the word. The delay between the last data bit and the pre-store pulse  $V_{prestore}$  is  $t_d = t_4$ . Store the word by raising the supply voltage to  $V_{store}$ ; the delay between the last data bit and the store pulse is  $t_d$ .



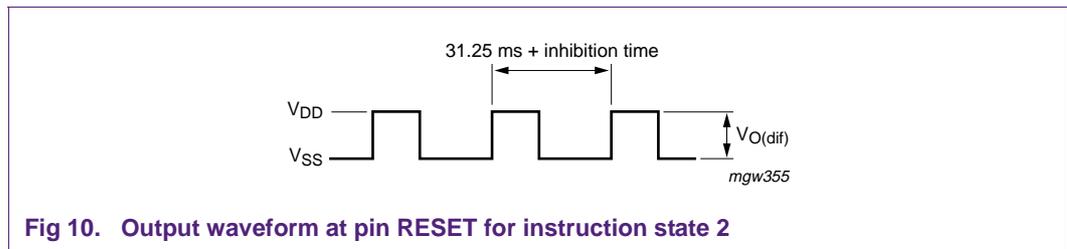
After state 3 has been entered the programming of the word and leaving state 3 is as indicated in the example of [Figure 8](#).

### 3.5 Check the inhibition time in State 2

In order to check whether programming was successful it is possible to measure the inhibition time. Also the inhibition time can either be monitored directly at pin RESET or as a modulation of the supply current (a modulating resistor of 30 kΩ is connected between V<sub>DD</sub> and V<sub>SS</sub> when the signal at pin RESET is HIGH, increasing the supply current accordingly). The inhibition time is measured in state 2. The inhibition time has a value of  $n \times 0.122$  ms (reciprocal of 8192 Hz). A signal with the periodicity of 31.25 ms +  $n \times 0.122$  ms appears at pin RESET and as a current modulation at pin V<sub>DD</sub>, see [Figure 9](#) and [Figure 10](#). The 31.25 ms is the reciprocal of 32 Hz.



[Figure 9](#) above indicates how to enter and leave state 2. [Figure 10](#) below indicates the output waveforms that appear at pin RESET in state 2.



## 4. References

- [1] **AN10439** — Wafer Level Chip Size Package
- [2] **AN10706** — Handling bare die
- [3] **PCA2000; PCA2001** — 32 kHz watch circuit with programmable adaptive motor pulse; product data sheet
- [4] **PCA2002** — 32 kHz watch circuit with programmable output period and pulse width; product data sheet
- [5] **PCA2003** — 32 kHz watch circuit with programmable adaptive motor pulse and pulse period; product data sheet

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Date of release: 4 September 2012

Document identifier: AN11219