PCA9502

8-bit I/O expander with I²C-bus/SPI interface

Rev. 03 — 13 October 2006 Product data sheet

1. General description

The PCA9502 is an 8-bit I/O expander with I²C-bus/SPI host interface. The device comes in a very small HVQFN24 package, which makes it ideally suitable for hand-held, battery operated applications.

The device also supports software reset, which allows the host to reset the device at any time, independent of the hardware reset signal.

2. Features

2.1 General features

- Selectable I²C-bus or SPI interface
- 3.3 V or 2.5 V operation
- Industrial temperature range: –40 °C to +85 °C
- Eight programmable I/O pins
- Software reset
- Industrial and commercial temperature ranges
- Available in HVQFN24 package
- 16 hardware-selectable slave addresses

2.2 I²C-bus features

- Noise filter on SCL/SDA inputs
- 400 kbit/s (maximum)
- Compliant with I²C-bus Fast-mode
- Slave mode only

2.3 SPI features

- 15 Mbit/s maximum speed
- Slave mode only
- SPI Mode 0

3. Applications

- Factory automation and process control
- Portable and battery operated devices
- Cellular data devices

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA9502BS	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-3

5. Block diagram

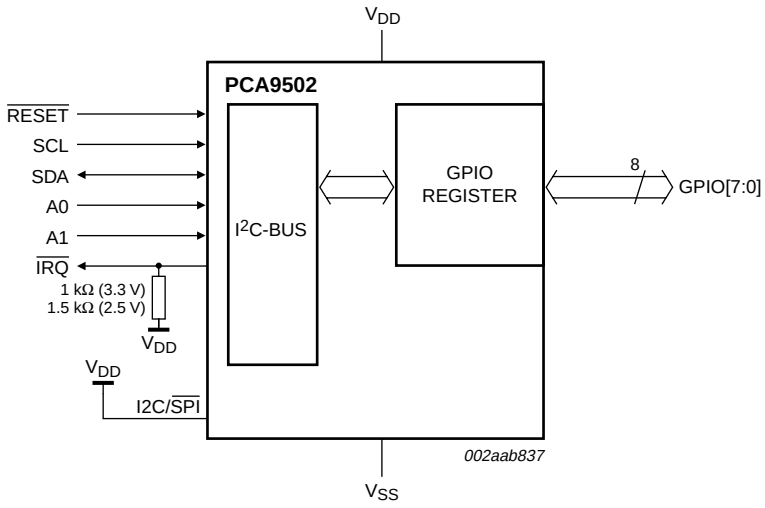


Fig 1. Block diagram of PCA9502 I²C-bus interface

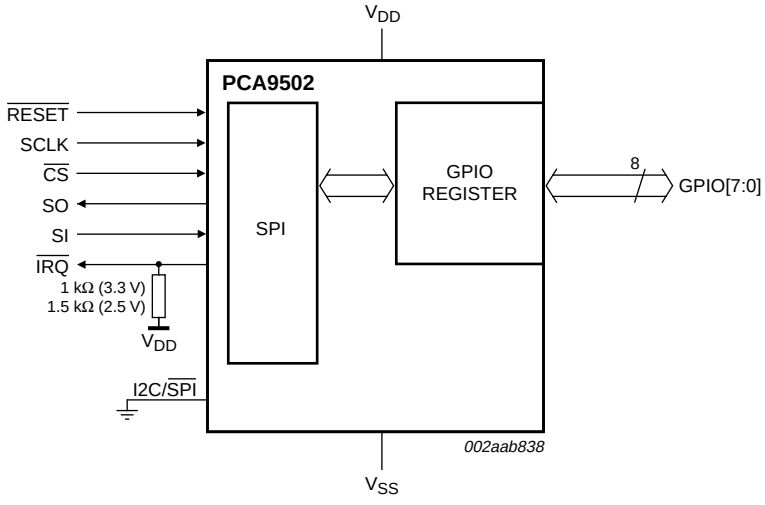
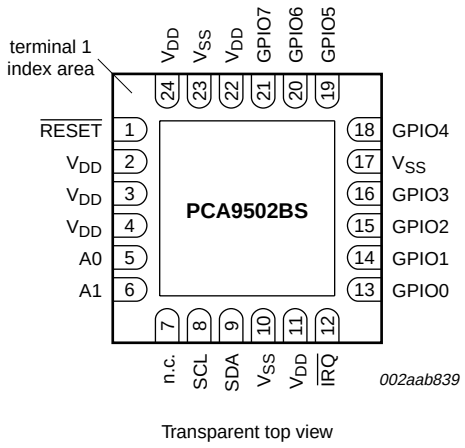


Fig 2. Block diagram of PCA9502 SPI interface

6. Pinning information

6.1 Pinning



a. I²C-bus interface

b. SPI interface

Fig 3. Pin configuration for HVQFN24

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
$\overline{RESET}$	1	I	device hardware reset (active LOW)[1]
V_{DD}	2, 3, 11, 22, 24	-	power supply
I2C/$\overline{SPI}$	4	I	I²C-bus or SPI interface select. I²C-bus interface is selected if this pin is at logic HIGH. SPI interface is selected if this pin is at logic LOW.
$\overline{CS}$/A0	5	I	SPI chip select or I²C-bus device address select A0. If SPI configuration is selected by I2C/$\overline{SPI}$ pin, this pin is the SPI chip select pin (Schmitt trigger, active LOW). If I²C-bus configuration is selected by I2C/$\overline{SPI}$ pin, this pin along with A1 pin allows user to change the device's base address.
SI/A1	6	I	SPI data input pin or I²C-bus device address select A1. If SPI configuration is selected by I2C/$\overline{SPI}$ pin, this is the SPI data input pin. If I²C-bus configuration is selected by I2C/$\overline{SPI}$ pin, this pin along with A0 pin allows user to change the device's base address. To select the device address, please refer to Table 11.
SO	7	O	SPI data output pin. If SPI configuration is selected by I2C/$\overline{SPI}$ pin, this is a 3-stateable output pin. If I²C-bus configuration is selected by I2C/$\overline{SPI}$ pin, this pin function is undefined and must be left as n.c. (not connected).
SCL/SCLK	8	I	I²C-bus or SPI input clock.
SDA	9	I/O	I²C-bus data input/output, open-drain if I²C-bus configuration is selected by I2C/$\overline{SPI}$ pin. If SPI configuration is selected then this pin is an undefined pin and must be connected to V_{SS}.

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
$\overline{IRQ}$	12	O	Interrupt (open-drain, active LOW). Interrupt is enabled when interrupt sources are enabled in the I/O Interrupt Enable register (IOIntEna). The interrupt condition is the change of state of the input pins. An external resistor (1 kΩ for 3.3 V, 1.5 kΩ for 2.5 V) must be connected between this pin and V_{DD}.
GPIO0	13	I/O	programmable I/O pin
GPIO1	14	I/O	programmable I/O pin
GPIO2	15	I/O	programmable I/O pin
GPIO3	16	I/O	programmable I/O pin
GPIO4	18	I/O	programmable I/O pin
GPIO5	19	I/O	programmable I/O pin
GPIO6	20	I/O	programmable I/O pin
GPIO7	21	I/O	programmable I/O pin
V_{SS}	10, 17, 23	-	ground
V_{SS}	center pad	-	The center pad on the back side of the HVQFN24 package is metallic and should be connected to ground on the printed-circuit board.

[1] See Section 7.1 “Hardware reset, Power-On Reset (POR) and software reset”

7. Functional description

The device interfaces to a host through either I²C-bus or SPI interface (selectable through I2C/$\overline{SPI}$ pin), and provides the host with eight programmable GPIO pins.

7.1 Hardware reset, Power-On Reset (POR) and software reset

These three reset methods are identical and will reset the internal registers as indicated in Table 3.

Table 3 summarizes the state of registers after reset.

Table 3. Registers after reset

Register	Reset state
I/O direction	all bits cleared
I/O interrupt enable	all bits cleared
I/O control	all bits cleared

Table 4 summarizes the state of hardware pins after reset.

Table 4. Signals after reset

Signal	Reset state
I/Os	inputs
$\overline{IRQ}$	HIGH by external pull-up

7.2 Interrupts

The PCA9502 has interrupt generation capability. The interrupt enable register (IOIntEna) enables interrupts due to I/O pin change of state, and the $\overline{IRQ}$ signal in response to an interrupt generation.

8. Register descriptions

The programming combinations for register selection are shown in Table 5.

Table 5. Register map - read/write properties

Register name	Read mode	Write mode
IODir	I/O pin direction	I/O pin direction
IOState	I/O pin states	n/a
IOIntEna	I/O interrupt enable register	I/O interrupt enable register
IOControl	I/O pins control	I/O pins control

Table 6. PCA9502 internal registers

Register address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
General Register Set										
0x0A[1]	IODir	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x0B[1]	IOState	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x0C[1]	IOIntEna	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0x0D[1]	reserved [2]	reserved [2]	reserved [2]	reserved [2]	reserved [2]	reserved [2]	reserved [2]	reserved [2]	reserved [2]	
0x0E[1]	IOControl	reserved [2]	reserved [2]	reserved [2]	reserved [2]	SReset	reserved [2]	reserved [2]	IOLatch	R/W

[1] Other addresses 0x00 through 0x09, 0x0F are reserved and should not be accessed (read or write).

[2] These bits are reserved and should be set to 0.

8.1 Programmable I/O pins Direction register (IODir)

This register is used to program the I/O pins direction. Bit 0 to bit 7 control GPIO0 to GPIO7.

Table 7. IODir register (address 0x0A) bit description

Bit	Symbol	Description
7:0	IODir	set GPIO pins 7:0 to input or output 0 = input 1 = output

Remark: If there is a pending input (GPIO) interrupt and IODir is written, this pending interrupt will be cleared, that is, the interrupt signal will be negated.

8.2 Programmable I/O pins State register (IOState)

When ‘read’, this register returns the actual state of all I/O pins. When ‘write’, each register bit will be transferred to the corresponding IO pin programmed as output.

Table 8. IOState register (address 0x0B) bit description

Bit	Symbol	Description
7:0	IOState	Write this register: set the logic level on the output pins 0 = set output pin to zero 1 = set output pin to one Read this register: return states of all pins

8.3 I/O Interrupt Enable register (IOIntEna)

This register enables the interrupt due to a change in the I/O configured as inputs.

Table 9. IOIntEna register (address 0x0C) bit description

Bit	Symbol	Description
7:0	IOIntEna	input interrupt enable 0 = a change in the input pin will not generate an interrupt 1 = a change in the input will generate an interrupt

8.4 I/O Control register (IOControl)

Table 10. IOControl register (address 0x0E) bit description

Bit	Symbol	Description
7:4	-	reserved for future use
3	SReset	software reset A write to this bit will reset the device. Once the device is reset this bit is automatically set to 0.
2:1	-	reserved for future use
0	IOLatch	enable/disable inputs latching 0 = input values are not latched. A change in any input generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input register is read, then the interrupt is cleared. 1 = input values are latched. A change in the input generates an interrupt and the input logic value is loaded in the bit of the corresponding input state register (IOState). A read of the IOState register clears the interrupt. If the input pin goes back to its initial logic state before the interrupt register is read, then the interrupt is not cleared and the corresponding bit of the IOState register keeps the logic value that initiates the interrupt. Example: If GPIO4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the IOState register will capture this change and an interrupt is generated (if enabled). When the read is performed on the IOState register, the interrupt is de-asserted, assuming there were no additional input(s) that changed, and bit 4 of the IOState register will read ‘1’. The next read of the IOState register should now read ‘0’.

9. I²C-bus operation

The two lines of the I²C-bus are a serial data line (SDA) and a serial clock line (SCL). Both lines are connected to a positive supply via a pull-up resistor, and remain HIGH when the bus is not busy. Each device is recognized by a unique address whether it is a microcomputer, LCD driver, memory or keyboard interface and can operate as either a transmitter or receiver, depending on the function of the device. A device generating a message or data is a transmitter, and a device receiving the message or data is a receiver. Obviously, a passive function like an LCD driver could only be a receiver, while a microcontroller or a memory can both transmit and receive data.

9.1 Data transfers

One data bit is transferred during each clock pulse (see Figure 4). The data on the SDA line must remain stable during the HIGH period of the clock pulse in order to be valid. Changes in the data line at this time will be interpreted as control signals. A HIGH-to-LOW transition of the data line (SDA) while the clock signal (SCL) is HIGH indicates a START condition, and a LOW-to-HIGH transition of the SDA while SCL is HIGH defines a STOP condition (see Figure 5). The bus is considered to be busy after the START condition and free again at a certain time interval after the STOP condition. The START and STOP conditions are always generated by the master.

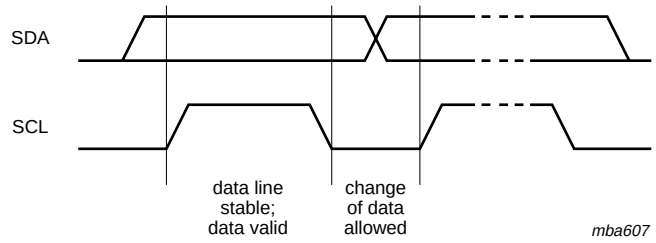


Fig 4. Bit transfer on the I²C-bus

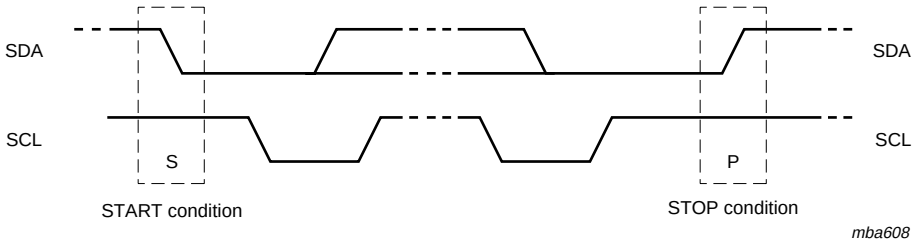


Fig 5. START and STOP conditions

The number of data bytes transferred between the START and STOP condition from transmitter to receiver is not limited. Each byte, which must be eight bits long, is transferred serially with the most significant bit first, and is followed by an acknowledge bit. (see Figure 6). The clock pulse related to the acknowledge bit is generated by the master. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, while the transmitting device releases this pulse (see Figure 7).

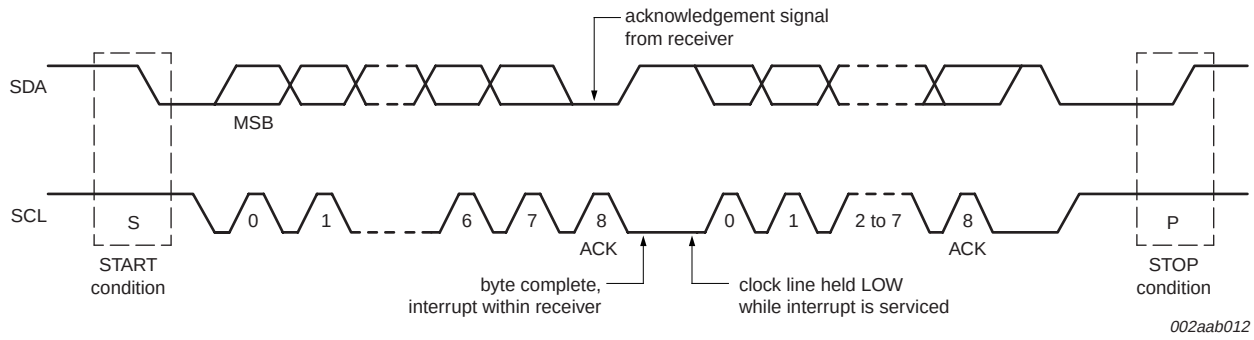


Fig 6. Data transfer on the I²C-bus

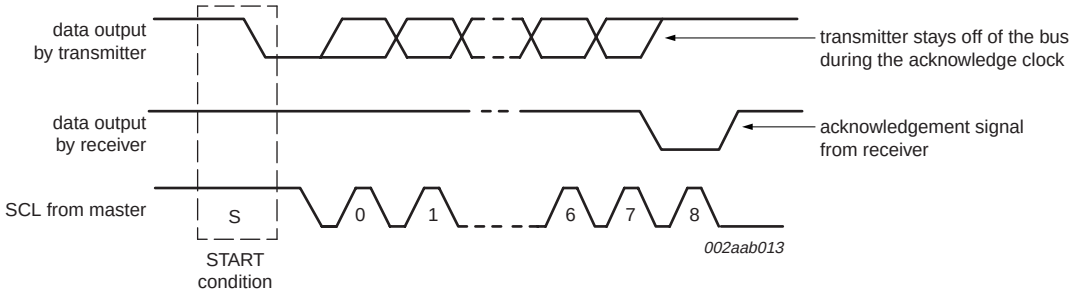


Fig 7. Acknowledge on the I²C-bus

A slave receiver must generate an acknowledge after the reception of each byte, and a master must generate one after the reception of each byte clocked out of the slave transmitter.

There is an exception to the ‘acknowledge after every byte’ rule. It occurs when a master is a receiver: it must signal an end of data to the transmitter by **not** signalling an acknowledge on the last byte that has been clocked out of the slave. The acknowledge related clock, generated by the master should still take place, but the SDA line will not be pulled down. In order to indicate that this is an active and intentional lack of acknowledgement, we shall term this special condition as a ‘negative acknowledge’.

9.2 Addressing and transfer formats

Each device on the bus has its own unique address. Before any data is transmitted on the bus, the master transmits on the bus the address of the slave to be accessed for this transaction. A well-behaved slave with a matching address, if it exists on the network, should of course acknowledge the master's addressing. The addressing is done by the first byte transmitted by the master after the START condition.

An address on the network is seven bits long, appearing as the most significant bits of the address byte. The last bit is a direction (R/$\overline{W}$) bit. A ‘0’ indicates that the master is transmitting (write) and a ‘1’ indicates that the master requests data (read). A complete data transfer, comprised of an address byte indicating a ‘write’ and two data bytes is shown in Figure 8.

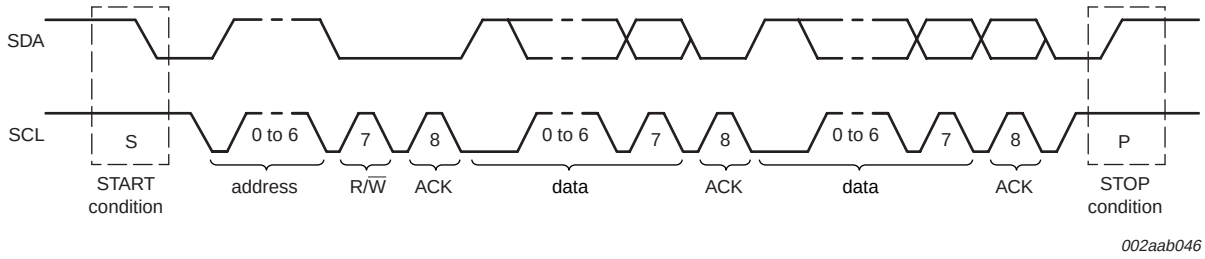


Fig 8. A complete data transfer

When an address is sent, each device in the system compares the first seven bits after the START with its own address. If there is a match, the device will consider itself addressed by the master, and will send an acknowledge. The device could also determine if in this transaction it is assigned the role of a slave receiver or slave transmitter, depending on the R/$\overline{W}$ bit.

Each node of the I²C-bus network has a unique seven-bit address. The address of a microcontroller is of course fully programmable, while peripheral devices usually have fixed and programmable address portions.

When the master is communicating with one device only, data transfers follow the format of Figure 8, where the R/$\overline{W}$ bit could indicate either direction. After completing the transfer and issuing a STOP condition, if a master would like to address some other device on the network, it could start another transaction by issuing a new START.

Another way for a master to communicate with several different devices would be by using a ‘repeated START’. After the last byte of the transaction was transferred, including its acknowledge (or negative acknowledge), the master issues another START, followed by address byte and data, without effecting a STOP. The master may communicate with a number of different devices, combining ‘reads’ and ‘writes’. After the last transfer takes place, the master issues a STOP and releases the bus. Possible data formats are demonstrated in Figure 9. Note that the repeated START allows for both change of a slave and a change of direction, without releasing the bus. We shall see later on that the change of direction feature can come in handy even when dealing with a single device.

In a single master system, the repeated START mechanism may be more efficient than terminating each transfer with a STOP and starting again. In a multimaster environment, the determination of which format is more efficient could be more complicated, as when a master is using repeated STARTs it occupies the bus for a long time and thus preventing other devices from initiating transfers.

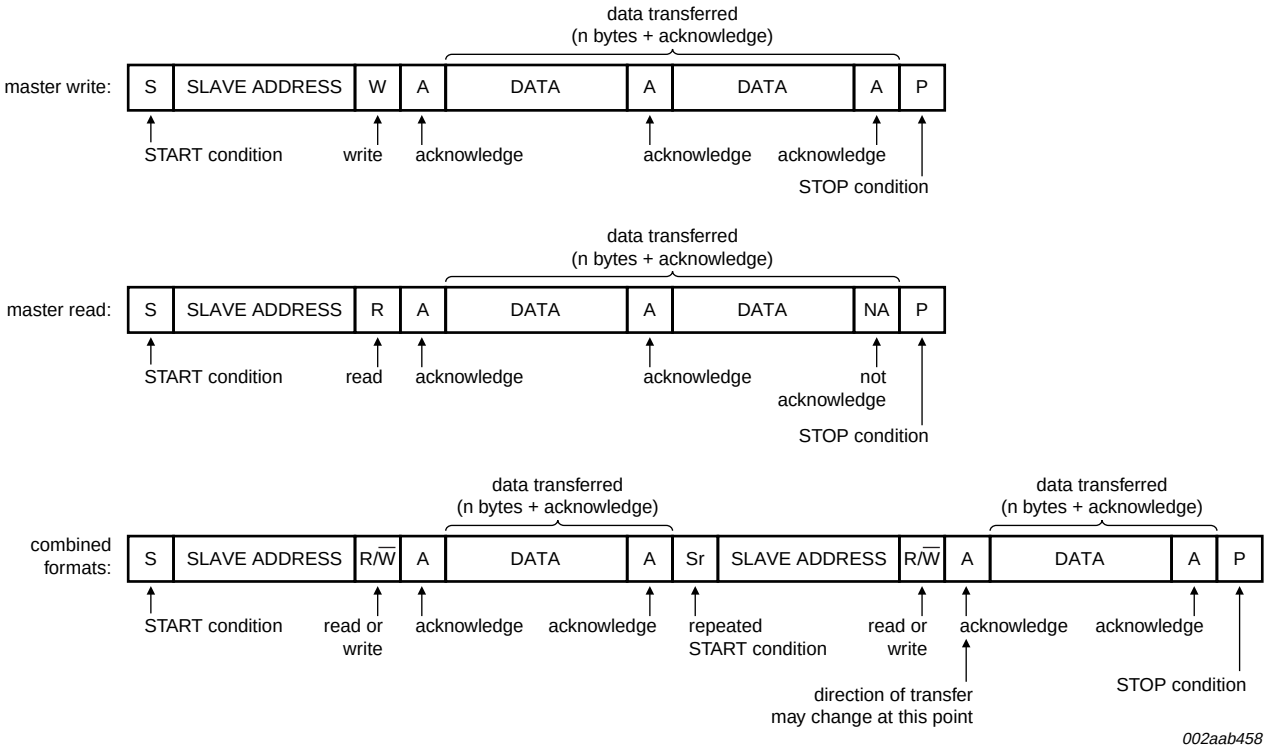


Fig 9. I²C-bus data formats

9.3 Addressing

Before any data is transmitted or received, the master must send the address of the receiver via the SDA line. The first byte after the START condition carries the address of the slave device and the read/write bit. Table 11 shows how the PCA9502's address can be selected by using A1 and A0 pins. For example, if these 2 pins are connected to V_{DD}, then the PCA9502's address is set to 0x90, and the master communicates with it through this address.

Table 11. PCA9502 address map

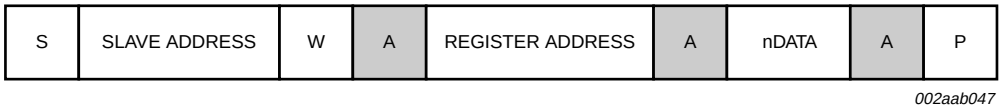
A1	A0	PCA9502 I²C-bus addresses (hex)[1]
V_{DD}	V_{DD}	0x90 (1001 000X)
V_{DD}	V_{SS}	0x92 (1001 001X)
V_{DD}	SCL	0x94 (1001 010X)
V_{DD}	SDA	0x96 (1001 011X)
V_{SS}	V_{DD}	0x98 (1001 100X)
V_{SS}	V_{SS}	0x9A (1001 101X)
V_{SS}	SCL	0x9C (1001 110X)
V_{SS}	SDA	0x9E (1001 111X)
SCL	V_{DD}	0xA0 (1010 000X)
SCL	V_{SS}	0xA2 (1010 001X)
SCL	SCL	0xA4 (1010 010X)
SCL	SDA	0xA6 (1010 011X)
SDA	V_{DD}	0xA8 (1010 100X)
SDA	V_{SS}	0xAA (1010 101X)
SDA	SCL	0xAC (1010 110X)
SDA	SDA	0xAE (1010 111X)

[1] X = logic 0 for write cycle; X = logic 1 for read cycle.

9.4 Use of sub-addresses

When a master communicates with the PCA9502 it must send a sub-address in the byte following the slave address byte. This sub-address is the internal address of the word the master wants to access for a single byte transfer, or the beginning of a sequence of locations for a multi-byte transfer. A sub-address is an 8-bit byte. Unlike the device address, it does not contain a direction (R/$\overline{W}$) bit, and like any byte transferred on the bus it must be followed by an acknowledge.

A register write cycle is shown in Figure 10. The START is followed by a slave address byte with the direction bit set to 'write', a sub-address byte, a number of data bytes, and a STOP signal. The sub-address indicates which register the master wants to access. and the data bytes which follow will be written one after the other to the sub-address location.

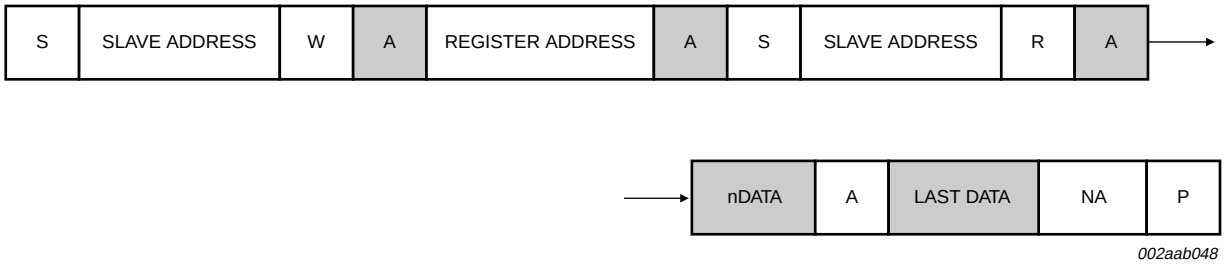


White block: host to PCA9502

Grey block: PCA9502 to host

Fig 10. Master writes to slave

The register read cycle (see Figure 11) commences in a similar manner, with the master sending a slave address with the direction bit set to 'write' with a following sub-address. Then, in order to reverse the direction of the transfer, the master issues a repeated START followed again by the device address, but this time with the direction bit set to 'read'. The data bytes starting at the internal sub-address will be clocked out of the device, each followed by a master-generated acknowledge. The last byte of the read cycle will be followed by a negative acknowledge, signalling the end of transfer. The cycle is terminated by a STOP signal.



White block: host to PCA9502

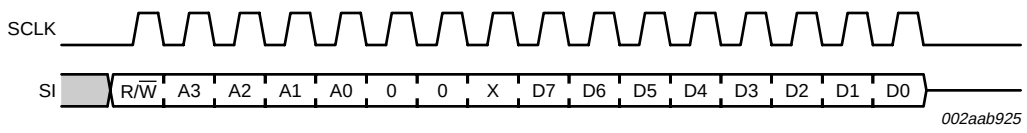
Grey block: PCA9502 to host

Fig 11. Master read from Slave

Table 12. Register address byte (I²C-bus)

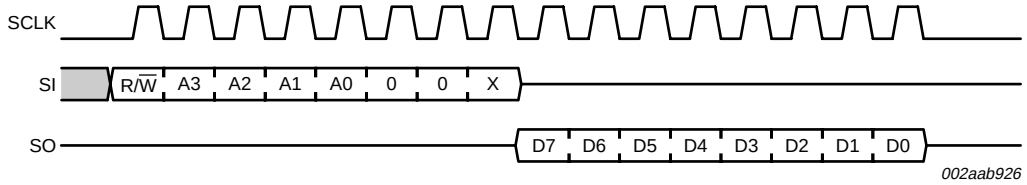
Bit	Name	Function
7	-	not used
6:3	A[3:0]	internal register select
2:1	-	not used, set to 0
0	-	not used

10. SPI operation



R/W = 0; A[3:0] = register address

a. Register write



R/W = 1; A[3:0] = register address

b. Register read

Fig 12. SPI operation

Table 13. Register address byte (SPI)

Bit	Name	Function
7	R/W	1: read from PCA9502 0: write to PCA9502
6:3	A[3:0]	internal register select
2:1	-	not used, set to 0
0	-	not used

11. Limiting values

Table 14. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.3	+4.6	V
V_I	input voltage	any input	–0.3	+5.5[1]	V
I_I	input current	any input	–10	+10	mA
I_O	output current	any output	–10	+10	mA
P_{tot}	total power dissipation		-	300	mW
P/out	power dissipation per output		-	50	mW
T_{amb}	ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C

[1] 5.5 V steady state voltage tolerance on inputs and outputs is valid only when the supply voltage is present. 4.6 V steady state voltage tolerance on inputs and outputs when no supply voltage is present.

12. Static characteristics

Table 15. Static characteristics

V_{DD} = (2.5 V ± 0.2 V) or (3.3 V ± 0.3 V); T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD} = 2.5 V		V_{DD} = 3.3 V		Unit
			Min	Max	Min	Max	
Supplies							
V_{DD}	supply voltage		2.3	2.7	3.0	3.6	V
I_{DD}	supply current	operating; no load	-	750	-	750	µA
		static; no load	-	600	-	600	µA
Inputs I2C/$\overline{SPI}$							
V_{IH}	HIGH-level input voltage		1.6	5.5[1]	2.0	5.5[1]	V
V_{IL}	LOW-level input voltage		-	0.6	-	0.8	V
I_L	leakage current	input; V_I = 0 V or 5.5 V[1]	-	1	-	1	µA
C_i	input capacitance		-	3	-	3	pF
Output SO							
V_{OH}	HIGH-level output voltage	I_{OH} = −400 µA	1.85	-	-	-	V
		I_{OH} = −4 mA	-	-	2.4	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	-	0.4	-	-	V
		I_{OL} = 4 mA	-	-	-	0.4	V
C_o	output capacitance		-	4	-	4	pF
Inputs/outputs GPIO0 to GPIO7							
V_{IH}	HIGH-level input voltage		1.6	5.5[1]	2.0	5.5[1]	V
V_{IL}	LOW-level input voltage		-	0.6	-	0.8	V
V_{OH}	HIGH-level output voltage	I_{OH} = −400 µA	1.85	-	-	-	V
		I_{OH} = −4 mA	-	-	2.4	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	-	0.4	-	-	V
		I_{OL} = 4 mA	-	-	-	0.4	V
I_L	leakage current	input; V_I = 0 V or 5.5 V[1]	-	1	-	1	µA
C_o	output capacitance		-	4	-	4	pF
Output $\overline{IRQ}$							
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	-	0.4	-	-	V
		I_{OL} = 4 mA	-	-	-	0.4	V
C_o	output capacitance		-	4	-	4	pF
I²C-bus input/output SDA							
V_{IH}	HIGH-level input voltage		1.6	5.5[1]	2.0	5.5[1]	V
V_{IL}	LOW-level input voltage		-	0.6	-	0.8	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	-	0.4	-	-	V
		I_{OL} = 4 mA	-	-	-	0.4	V
I_L	leakage current	input; V_I = 0 V or 5.5 V[1]	-	10	-	10	µA
C_o	output capacitance		-	7	-	7	pF

Table 15. Static characteristics *...continued*

V_{DD} = (2.5 V ± 0.2 V) or (3.3 V ± 0.3 V); T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD} = 2.5 V		V_{DD} = 3.3 V		Unit
			Min	Max	Min	Max	
I²C-bus inputs SCL, $\overline{CS}$/A0, SI/A1							
V_{IH}	HIGH-level input voltage		1.6	5.5[1]	2.0	5.5[1]	V
V_{IL}	LOW-level input voltage		-	0.6	-	0.8	V
I_L	leakage current	input; V_I = 0 V or 5.5 V[1]	-	10	-	10	µA
C_i	input capacitance		-	7	-	7	pF

[1] 5.5 V steady state voltage tolerance on inputs and outputs is valid only when the supply voltage is present. 3.8 V steady state voltage tolerance on inputs and outputs when no supply voltage is present.

13. Dynamic characteristics

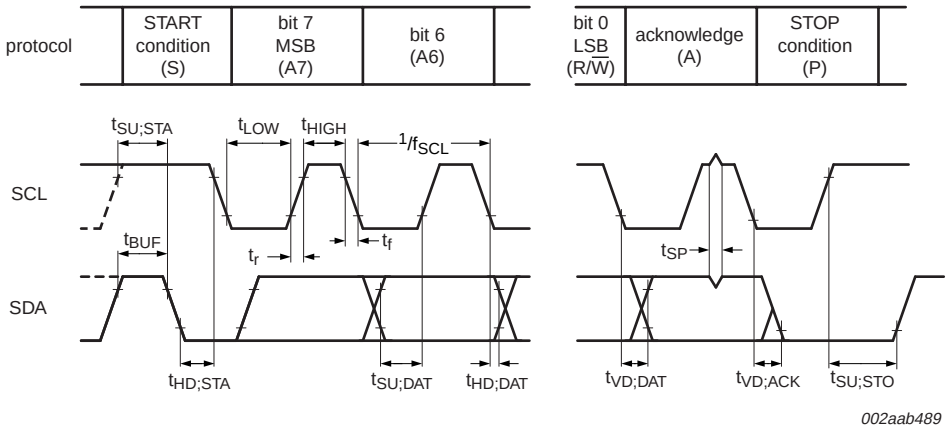
Table 16. I²C-bus timing specifications

All the timing limits are valid within the operating supply voltage, ambient temperature range and output load; V_{DD} = (2.5 V ± 0.2 V) or (3.3 V ± 0.3 V); T_{amb} = −40 °C to +85 °C; refer to V_{IL} and V_{IH} with an input voltage of V_{SS} to V_{DD}. All output load = 25 pF, except SDA output load = 400 pF.[1]

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		[2]	0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.7	-	0.6	-	µs
$t_{HD;DAT}$	data hold time			0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time			-	0.6	-	0.6	µs
$t_{VD;DAT}$	data valid time	SCL LOW to data out valid		-	0.6	-	0.6	ns
$t_{SU;DAT}$	data set-up time			250	-	150	-	ns
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals			-	300	-	300	ns
t_r	rise time of both SDA and SCL signals			-	1000	-	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns
t_{d1}	I²C-bus GPIO output valid time			0.5	-	0.5	-	µs
t_{d4}	I2C input pin interrupt valid time			0.2	-	0.2	-	µs
t_{d5}	I2C input pin interrupt clear time			0.2	-	0.2	-	µs

[1] A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

[2] Minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if SDA is held LOW for a minimum of 25 ms.



Rise and fall times refer to V_{IL} and V_{IH}.

Fig 13. I²C-bus timing diagram

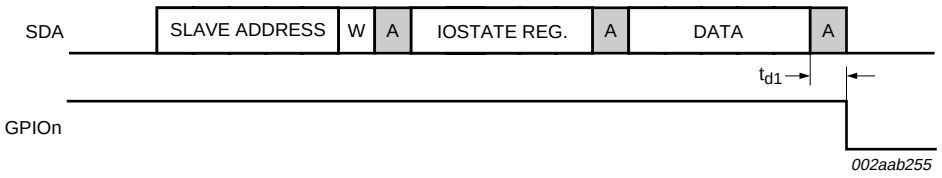


Fig 14. Write to output

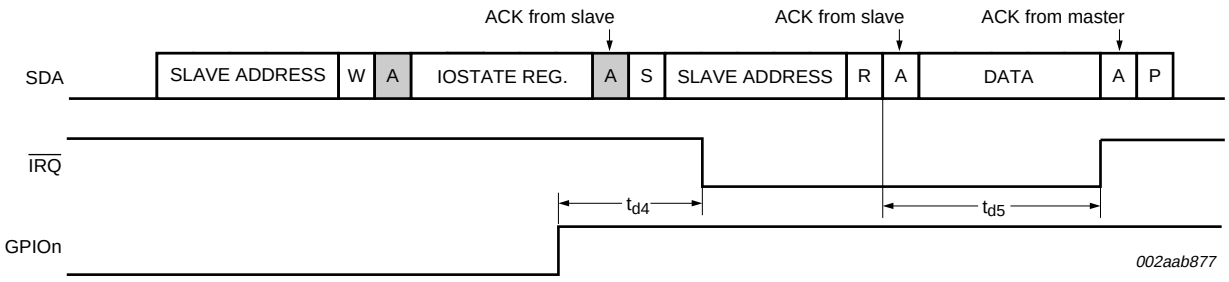


Fig 15. GPIO pin interrupt

Table 17. SPI-bus timing specifications

All the timing limits are valid within the operating supply voltage, ambient temperature range and output load; V_{DD} = (2.5 V ± 0.2 V) or (3.3 V ± 0.3 V); T_{amb} = −40 °C to +85 °C; and refer to V_{IL} and V_{IH} with an input voltage of V_{SS} to V_{DD}. All output load = 25 pF, unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD} = 2.5 V		V_{DD} = 3.3 V		Unit
			Min	Max	Min	Max	
$t_{d(CS\_NH-SOZ)}$	$\overline{CS}$ HIGH to SO 3-state delay time	C_L = 100 pF	-	100	-	100	ns
$t_{su(CS\_N-SCLK)}$	$\overline{CS}$ to SCLK setup time		100	-	100	-	ns
$t_{h(CS\_N-SCLK)}$	$\overline{CS}$ to SCLK hold time		20	-	20	-	ns
$t_{d(SCLK-SO)}$	SCLK fall to SO valid delay time	C_L = 100 pF	-	25	-	20	ns
$t_{su(SI-SCLK)}$	SI to SCLK setup time		10	-	20	-	ns
$t_{h(SI-SCLK)}$	SI to SCLK hold time		10	-	10	-	ns
T_{SCLK}	SCLK period	t_{SCLKL} + t_{SCLKL}	83	-	67	-	ns
t_{SCLKH}	SCLK HIGH time		30	-	25	-	ns
t_{SCLKL}	SCLK LOW time		30	-	25	-	ns
$t_{w(CS\_NH)}$	$\overline{CS}$ HIGH pulse width		200	-	200	-	ns
t_{d9}	SPI output data valid time		200	-	200	-	ns
t_{d13}	$\overline{SPI}$ interrupt clear time		200	-	200	-	ns

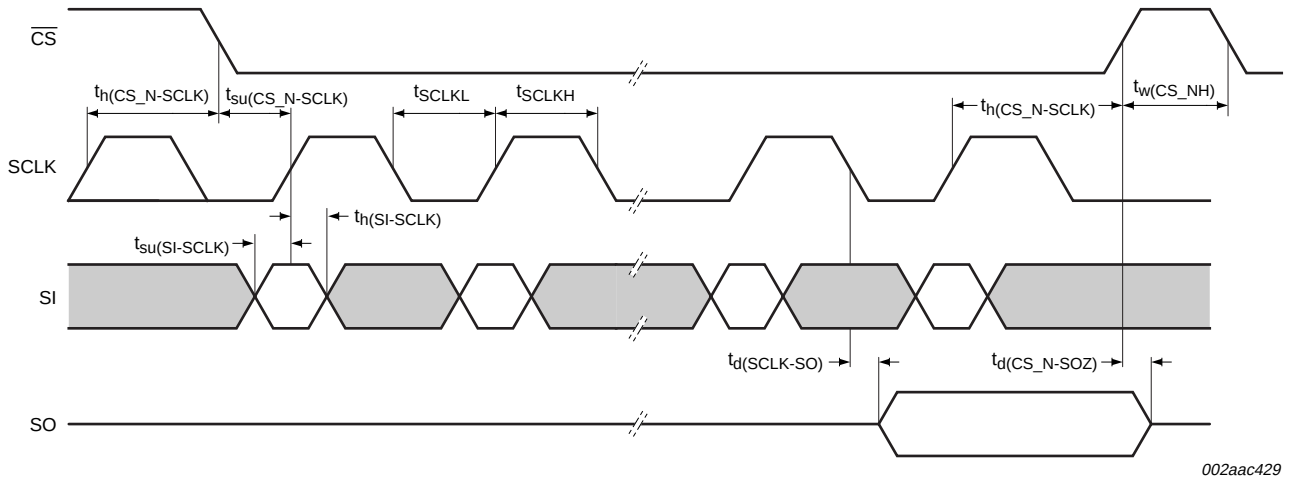
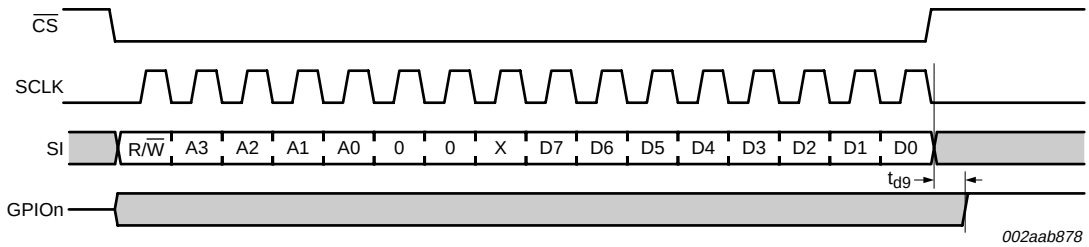
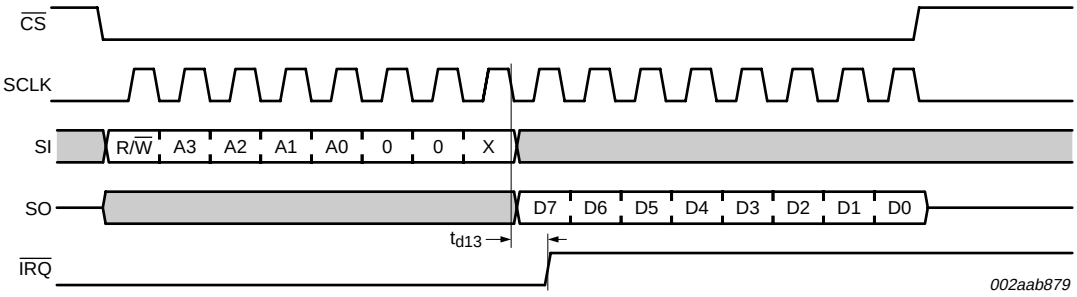


Fig 16. Detailed SPI-bus timing



R/$\overline{W}$ = 0; A[3:0] = IOState (0x0B)

Fig 17. SPI write IOState to GPIO switch

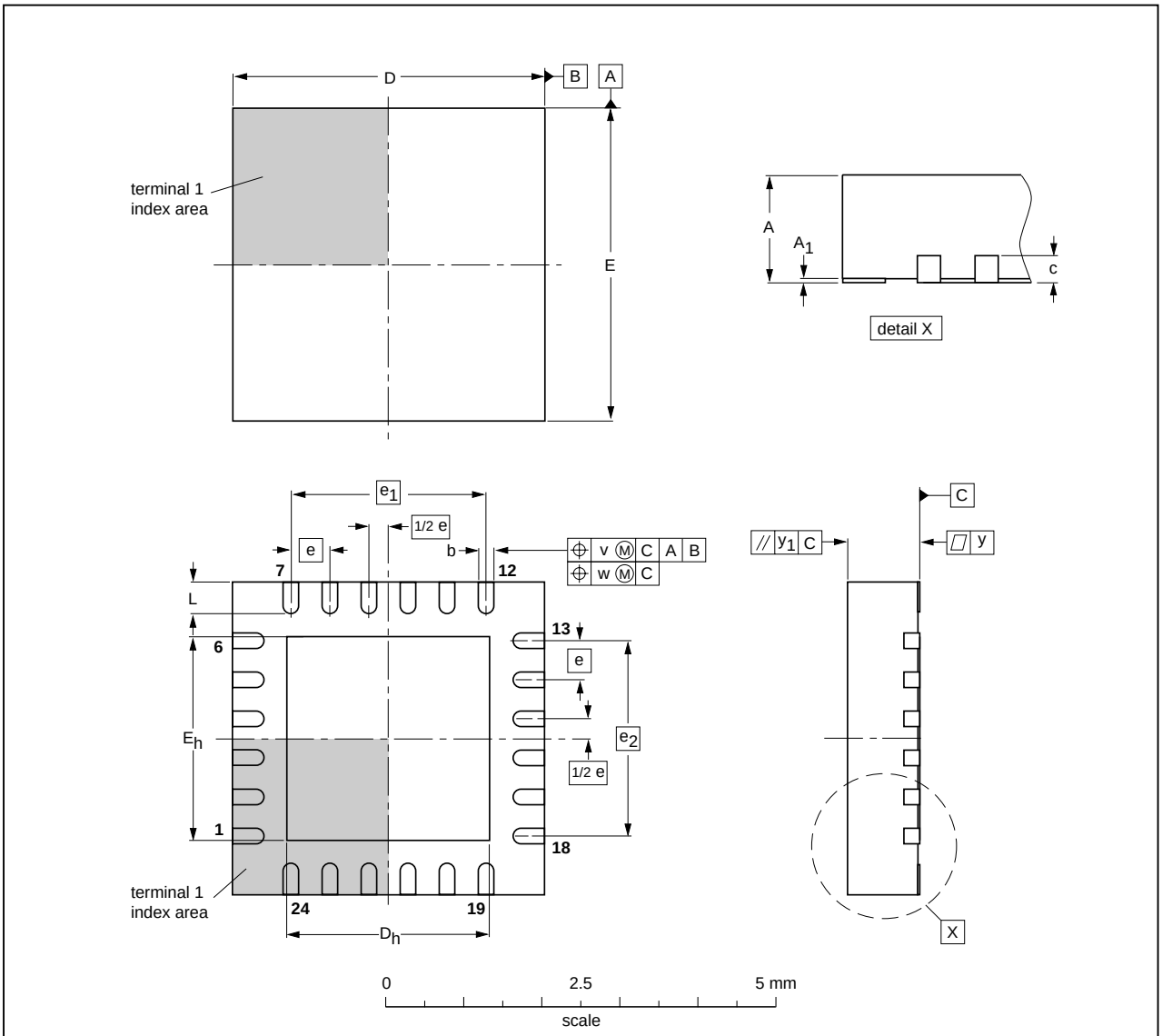


R/W = 1; A[3:0] = IOState (0x0B)

Fig 18. Read IOState to clear GPIO INT

14. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.75 2.45	4.1 3.9	2.75 2.45	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-3	- - -	MO-220	- - -			~~04-11-19~~ 05-03-10

Fig 19. Package outline SOT616-3 (HVQFN24)

15. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

16. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 20) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 18 and 19

Table 18. SnPb eutectic process (from J-STD-020C)

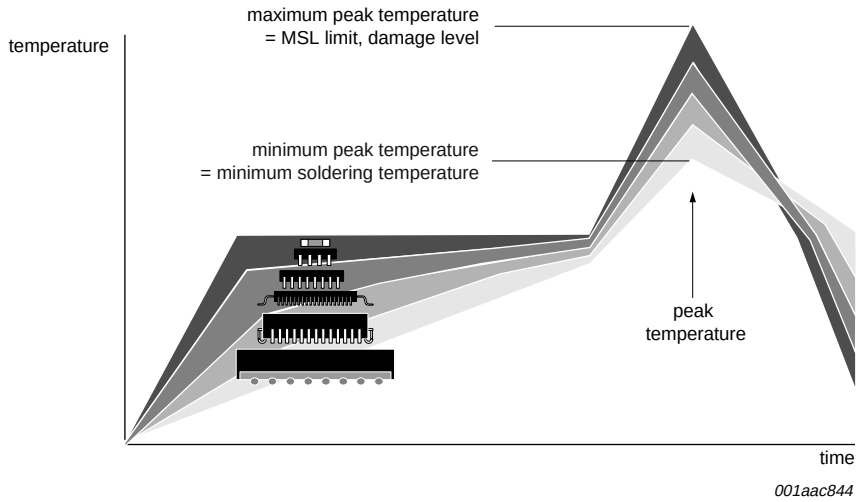
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 19. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 20.



MSL: Moisture Sensitivity Level

Fig 20. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 20. Abbreviations

Acronym	Description
GPIO	General Purpose Input/Output
I²C-bus	Inter Integrated Circuit bus
I/O	Input/Output
LCD	Liquid Crystal Display
POR	Power-On Reset
SPI	Serial Peripheral Interface

18. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9502_3	20061013	Product data sheet	-	PCA9502_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 15 “Static characteristics”, sub-section “Supplies”: – I_{DD}, supply current, operating; no load: changed maximum limit from 6.0 mA to 750 μA for both 2.5 V and 3.3 V supply voltage ranges – I_{DD}, supply current: added “static; no load” Conditions (max 600 μA)			
PCA9502_2	20060803	Product data sheet	-	PCA9502_1
PCA9502_1	20060707	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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