Designing a PD69208 48-port PoE System 802.3af/802.3at Compliant

Application Note

Introduction

This application note provides detailed information and circuitry design guidelines for the implementation of a 48-port Power over Ethernet (PoE) system, based on Microsemi's™ PoE manager and PD69200 PoE Controller.

PoE manager can be:

8-channel: PD69208- old version,

PD69208M- support up to 60W,

PD69208T4-(4 pair).

And 4-channel: PD69204,PD69204T4-(4 pair).

A layout guideline for PoE system based on PD69208/4 is also included in this document.

This document enables designers to integrate PoE capabilities, as specified in IEEE802.3af, IEEE802.3at and PoH standards, into an Ethernet switch.

PD69208/4 PoE manager implements real time functions as specified in the standards, including detection, classification, port-status monitoring, and system level activities such as power management and MIB (Management Information Base) support for system management. The PoE manager is designed to detect and disable disconnected PDs (Powered Devices), using DC disconnection methods, as specified in the standards.

The PD69208/4 provides PD real time protection through the following mechanisms: overload, under load, over voltage and short-circuit.

PD69208/4 share the same design, package and features. The only different between PD69208 and PD69204 is the number of ports.

An evaluation board (P/N PD-IM-7648) can be ordered.

Applicable Documents

- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- PD69208 and PD69200 datasheet, catalogue number DS_PD69208
- DS_PD69208T4_PD69200
- DS_PD69204T4_PD69200
- DS_PD69208M_PD69200
- IEEE 802.3BT draft 2.0
- Serial Communication Protocol user guide , catalogue number PD69200_UG_COMM_PROT
- PD69200_TN_218 PoE LED Stream Interface
- TN_205 6Kv surge protection.
- TN_134 Emergency Power Management.

Features

- IEEE 802.3af-2003 standard compliant
- IEEE802.3at-2009 standard compliant
- Power over HDBasT standard compliant (60W/95W)
- Configurable AT/AF modes
- Configurable standard/reduced cap detection mode
- Supports pre-standard PD detection
- Supports Cisco devices detection
- Single DC voltage input (44 – 57V_{DC})
- Two & three event classification
- Voltage monitoring/protection
- Low power dissipation
- Internal sense resistor (0.1Ω)
- Internal MOSFET with Low R_{DS_ON} (~0.24Ω)
- Internal power on reset
- Only one external front end component per port
- Includes Reset input from hosting system
- Four direct address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- On-chip thermal protection
- Built in 3.3V_{DC} and 5V_{DC} regulators

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- Emergency power management supporting sixteen configurable power banks
- Can be cascaded to up to 12 PoE devices (48 logical ports in 4 pairs configuration).
- Supports 4 pair connection (PD69208T4)
- Wide temperature range: -40° to +85°C MSL3,RoHS compliant
- Support I2C and UART communication & software update.

Integration

The system described is destined for a 48-port switch feeding power over two pair for each port. Any combination between PD69208 and PD69204 can be implemented with up to 12 chips. Same design can be applied to 1 to 12 PoE managers controlling eight ports each (from 8 ports to 96 ports in multiples of 8) or with PD69204 in multiples of 4 ports.

PoE system board can be easily integrated on top of a switch, providing the capability to add any PoE application while using different daughter applications (refer to Figure 1).

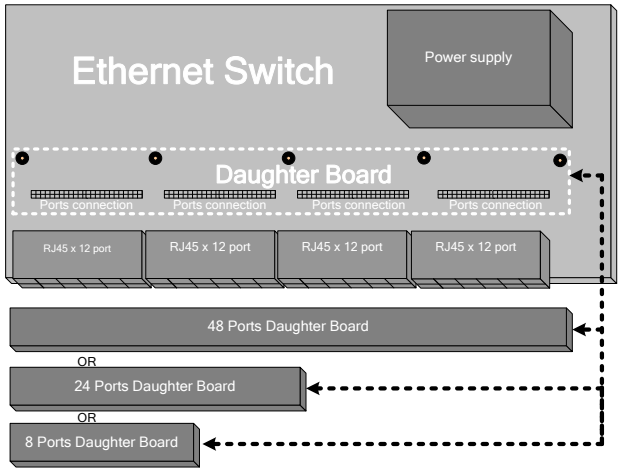

Figure 1: PoE Daughter Board Integration

Overall Description

A typical application includes the following blocks (Figure 2):

- PoE circuit for 48 ports based on six PD69208.
- Controller circuit, used to initialize, control and monitor each of the PD69208 via an internal ESPI isolated bus. The PoE Controller communicates with the Host CPU via a non-isolated UART or an I^2C interface.
- Isolation Circuit for ESPI bus.

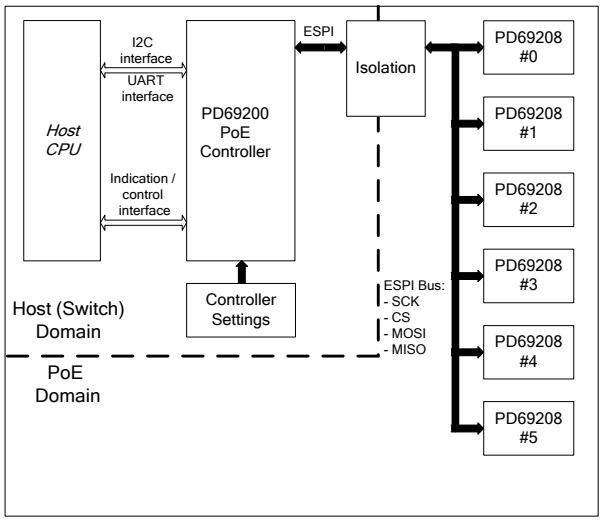

Figure 2: 48-port Configuration block diagram

General Circuit Description

The 48-port configuration for a PoE system shown in Figure 2, comprises six PoE managers circuits (PD69208) controlled by a PoE Controller (PD69200). The PoE Controller utilizes the ESPI bus to control the PoE managers. PoE operations are automatically performed by PoE manager circuits, while PoE Controller performs power management and other tasks. A configuration of 96 ports over two pairs of wires per port or 48 ports over four pairs of wires per port is also possible using 12 PoE

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managers circuits (PD69208) controlled by a single PoE Controller (PD69200).

Communication Interfaces

Communication between Host CPU and local PoE Controller is performed via an UART or an I^2C interface. For more information, refer to the *Serial Communication Protocol User Guide, catalogue number PD69200_UG_COMM_PROT.*

Communication Flow

Host CPU issues commands, utilizing a dedicated Serial Communication Protocol to the PoE Controller.

PoE Controller converts Serial Communication Protocol to ESPI Communication and sends it via isolated ESPI lines to appropriate PD69208. This isolation is a basic requirement of IEEE PoE standards.

ESPI Bus

The Enhanced Serial Peripheral Interface (ESPI) bus, used for internal communication, includes the following lines:

- MOSI (Master Out/Slave In) provides communication from PoE Controller to PD69208
- MISO (Master In/Slave Out) provides communication from PD69208 to PoE Controller
- SCK is the serial clock generated by the Controller
- CS (Chip Select) is utilized by PoE Controller to transmit data simultaneously to all PD69208 ICs, while only chosen PoE manager responds back

Control

Refer to Figure 3.

- An xReset_IN control signal driven by Host CPU is used to reset the PoE system
- An xDisable_ports control signal driven by Host CPU is used to disable all PoE ports at once

Indications

- An xSystem_ok signal is generate by The PoE Controller, indicates that the input main voltage is within range. this pin is determined by 15 byte serial communication protocol.
- An xInt_out interrupt signal, utilized to indicate PoE events such as Port On, Port Off, Port Fault, PoE manager Fault, Voltage out of range etc
- An xI2C_Message_Ready indicates signals message is ready to be read by Host.

  For full list of interrupt events, refer to *PD69200 Serial Communication Protocol User Guide, catalogue number PD69200_UG_COMM_PROT.*

Main Supply

PoE system operates within a range of 44 to $57V_{DC}$ (802.3at port's range is 50 to $57V_{DC}$). To comply with UL SELV regulations, maximum output voltage **should not** exceed $60V_{DC}$.

Grounds

Several grounds are utilized in the system.

- PoE Domain Analog
- PoE Domain Digital
- Chassis
- Host Domain Floating

Digital and analog grounds are electrically same ground, however, to reduce noise coupling, grounds are physically separated and connected only at a single point.

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Chassis ground is connected to switch's chassis ground. This ground plane should be $1500V_{rms}$ isolated from PoE circuitry.
PoE controller relates to Host domain floating ground which is isolated from PoE domain grounds.

$5V_{DC}$ and 3.3 V_{DC} Regulators

Each PD69208 has a $5V_{DC}$ and a $3.3V_{DC}$ regulators for internal IC circuitry and can provide up to 6mA together to be utilized for powering components in the PoE domain. The 5V is been powered from Vmain by internal regulator and the 3.3V is been powered from the 5V with another internal regulator. In order to minimize time delay between the 5V and 3.3V rise during first system power up a 4.7uF capacitor should be placed between those pin's (pin 20, 22).
An external boost transistor can be added to the $5V_{DC}$ regulator's output (instead of R166) to increase the current (see **Figure 11**). The transistor can provide a total of 30mA to the PoE Controller and to the isolation circuits. This total current is the sum of the 5V and 3.3V currents. All external components in this circuitry must also be isolated from the switch circuitry by $1500V_{rms}$.

Detailed Circuit Description

Communication Interfaces/Isolation

There are two communication interfaces in this circuitry:

- An interface between the Ethernet switch and the PoE Controller; this interface is an I^2C or an UART interface and does not require isolation
- An interface between PoE Controller and PoE managers with 1500Vrms isolation; this interface is a standard SPI

Isolation circuit comprises a digital isolator (U13 on Figure 10). Note that each side of the isolator circuitry is fed by a separate power supply.

Control and Indication Signals

Control/Indication signals are of the single H/W lines type running between Host CPU and PoE Controller (Refer to Figure 3).

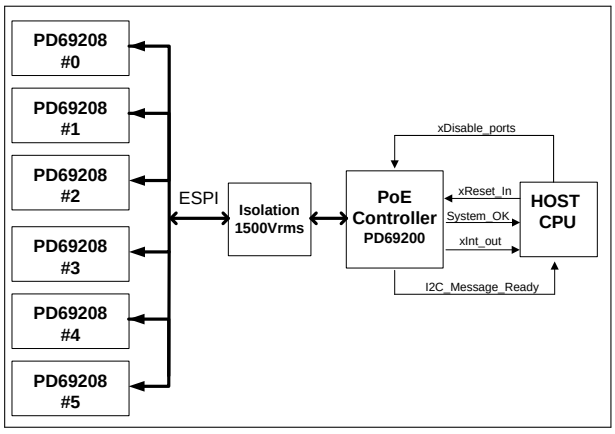

Figure 3: Control and Indication Signals

Control Signals

There are two control lines driven by Host CPU to PoE Controller:

- xDisable_ports: Disables all PoE ports. When PoE Controller detects low level voltage at PD69200 pin #31, it sends a disable command via ESPI to all PoE manager's ports
- xReset_In: Resets PoE Controller and all PoE managers. When PoE Controller detects low level voltage at PD96200 pin #19, it enters Reset mode and all its output pins switch to Tri-state mode. When xReset_In line returns to 'high', PoE Controller initializes and sends RESET command to PoE managers via the ESPI bus. xReset_In is also used by the PoE Controller watchdog to reset itself, and therefore the host should drive a reset using

an open drain output and a pull up to eliminate conflict.

PoE Controller Circuitry

Refer to Figure 8.

Interface to PoE manager:

PoE Controller features 1Mb/s ESPI for each of the PoE managers, and a communication interface with Host CPU via UART or I^2C protocol.

Interface to host:

UART (set to 19200 bps)or I^2C (up to 400KHz) communication between Host CPU and PoE Controller are managed by setting PoE Controller's address, pin #22 (I^2C_ADDR). For UART and I^2C communication address table, refer to Serial Communication Host-Controller on page 7 (See Table 1).

Clock: The PoE Controller runs at 47.972MHz, facilitated by an internal Clock.

Supply: PoE Controller requires stable, filtered power for its operation coming from the Host (3_3V_iso); hence, a number of decoupling capacitors are included in the design (C56, C71, C92). Expected current consumption of the PoE controller circuitry should be below 20mA.

SELF_RESET: As required by the application, the PoE Controller can reset itself. This reset can also be performed by an external source utilizing the **xReset_In** signal (usually by Host Controller). If the hose utilize the XReset_in it should drive a reset using an open drain output and a pull up to eliminate conflict.

LED Support

Refer to Figure 4.

LED support for port status indication is accomplished by utilizing the **ESPI bus** (SCK and MOSI), **xLED_CS, xLED_OE**, and **xLED_Latch** signals. Bus behavior is 1Mhz synchronous serial communication (clock, data) in one direction (write only) that transmits the status of up to 96 ports. For more details, refer to Technical Note-218, catalogue number PD69200_TN_218.

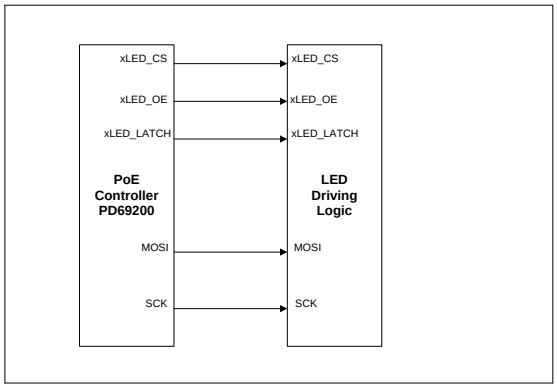

Figure 4: SPI Bus and LED Support

Emergency Power Management

PoE circuits can be powered by up to four separate power supplies. It is recommended each power supply will be capable of generating a logic signal, indicating its operate/fail status. Refer to Figure 5.

The used pins are as follows:

PD69208 PIN NUMBER	SIGNAL	REMARKS
#56	PG0	Power Good 0
#41	PG1	Power Good 1
#46	PG2	Power Good 2
#47	PG3	Power Good 3

PoE circuit allocates power to the system in 16 power levels (power banks) programmed by users. Power bank values are based on each supply's available power and on the state of the logic signals PG[0..3] coming from power supplies. If PG pin is not used, the pin must be connected to GND or VDD. Figure 5 illustrates the connections between power supplies' logic signals and PoE Manager.

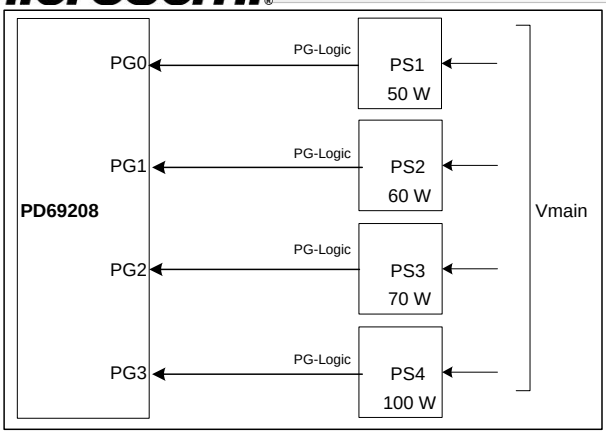

Figure 5: Power Good

For isolation requirements destined for Emergency Power Management, refer to *Technical Note-134, catalogue number 06-0014-081*, section "Isolation Requirements".

PoE Manager Circuitry

PD69208 performs a variety of internal operations and PoE functions, requiring a minimum of external components. Each PD69208 handles up to 8 ports.

Figure 9 shows PoE Manager #0 with its related components for an 8-port configuration. What's being presented in this figure is duplicated 6 times for 48 ports.

Reference Current Source

Reference for internal voltages within PD69208 is set by a precision resistor (R60) - 28.7KΩ 1%. In PoH system the precision resistor should be 0.1%.

Sense Resistors

PD69208 is providing an internal sense resistor of 100mΩ to each port sense pin. This resistor is utilized to measure port current.

Front End components

A single capacitor per port is the only external front end component been used. The capacitor value can be between 22nF to 220nF.

All other components such as reverse diode, port protection, sense resistor and switching mosfet are internal.

Fuses per port are not required for use in circuits with total power level of up to 3kW as the PD69208 designed to fulfill limited power source (LPS) requirements per the latest editions of IEC60950-1 and EN60950-1.

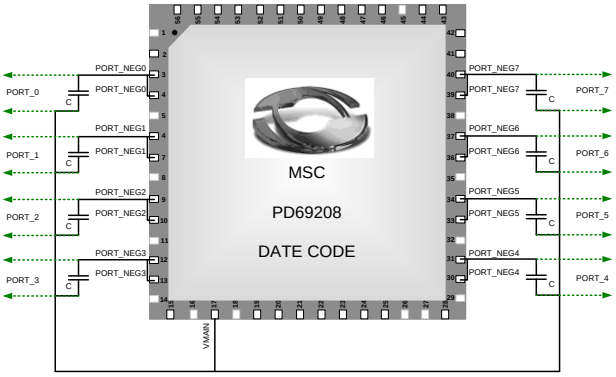

Figure 6: 8-ports Front End components

Line transformer

The designer should use a line transformer that dedicated to PoE. Moreover a special care should be taken in order to choose a line transformer with the application desired PoE current.

Serial Communication Host-Controller

PoE Controller can communicate with the hosting system using UART or I^2C communication. As for I^2C communication bus the PoE controller may be one of few controlled devices reporting to the host, the user need to configure a dedicated address for the PoE Controller. This is done by selecting a value for R93 (Figure 8). This resistor sets the analog level into pin #22 (I2C_ADDR_Meas_ADC0), as specified in the following table.

I^2C Address	Address (hex)	R93 (ohms)	I^2C Address	Address (hex)	R93 (ohms)
#0	UART	NA	#8	0x20	8870
#1	0x4	97600	#9	0x24	6810
#2	0x8	53600	#10	0x28	5230
#3	0xC	35700	#11	0x2C	3920

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#4	0x10	25500	#12	0x30	2800
#5	0x14	19100	#13	0x34	1870
#6	0x18	14700	#14	0x38	1020
#7	0x1C	11300	#15	0x3C	324

Table 1: Serial Communication configuration

UART

An Rx signal should be connected to pin #11 of PoE Controller.
A Tx signal should be connected to pin #12 of PoE Controller.
A pull up resistor is required on the UART communication line (see Figure 8).

I^2C

An SDA signal should be connected to pin #21 of PoE Controller.
An SCL signal should be connected to pin #20 of PoE Controller.
A pull up resistor is required on the I^2C communication line (pins 20 and 21).

Ground Interface Connection (AGND)

Power supplies ground connector enables the current path back to power supply. Ground connection should be capable of carrying all strings current back to power supplies.

Four Pair Connectivity

Designing a PoE port delivering power over RJ45 four pairs of wires is quite easy by utilizing PD69208T4. Just connect any two ports of the PD69208T4 to a single RJ45 connector and configure the PD69200 accordingly. The two ports utilized for the four pair output terminal can be taken from the same PD69208T4 or from any two PD69208T4 ICs in the system. PD69208T4 can deliver AT power, enabling delivery of 60W over 4-pairs, or PoH power delivering 95W over 4-pairs.

PD69200 configuration process is further explained in the Serial Communication Protocol User Guide, catalogue number PD69200_UG_COMM_PROT.

Thermal Design

The design should take into account power dissipation of PoE manager and associated circuitry and the maximum ambient operating temperature of the switch. Adequate ventilation and airflow should be part of the design to avoid thermal over-stress.

Ambient Temperature

Application's thermal design should take into account the temperature derived from Switch's power dissipation and from PoE daughter board powered at maximum load.

PD69208/69204

PoE design should ensure that PD69208/4 maximum operating junction temperature (130°C) is not exceeded under worst case conditions. Worst case conditions typically involve operation under maximum ambient temperature, output ports fully loaded at the maximum load according to the design, and all other product units functions and fully operational (such as the Ethernet Switch phy, power supply, LED drivers etc.). *PD69208 datasheet, catalogue number DS_69208 contains* additional thermal characteristics details.

PD69200

Layout considerations should ensure that:

- PD69200 is placed away from potential high temperature sources.
- Maximum case temperature does not exceed 85°C under worst case conditions.
- PD69200 thermal pad should be connected to the floating ground plan (F_GND).

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Block Diagram/Main

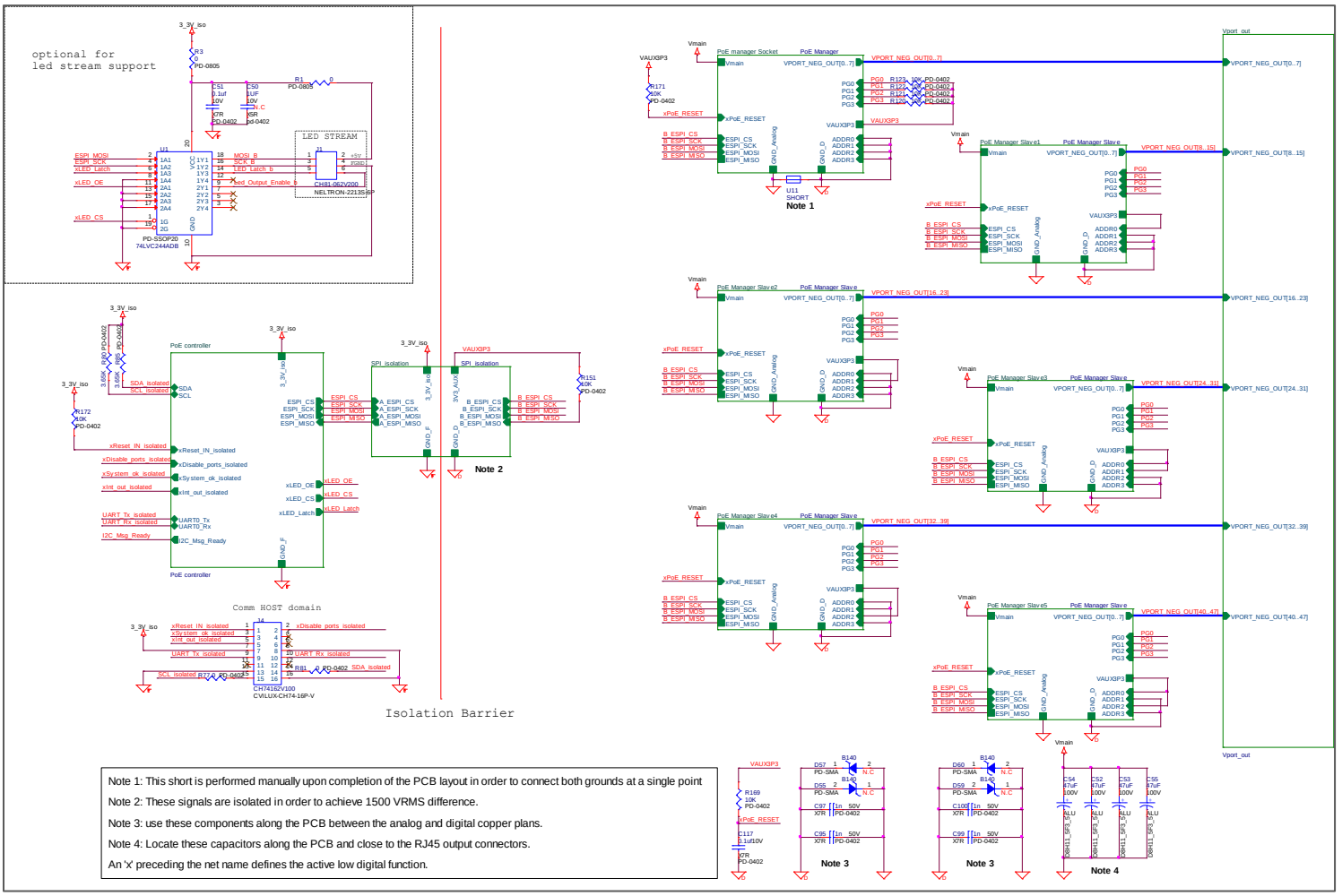

Figure 7 : 48-port System main blocks

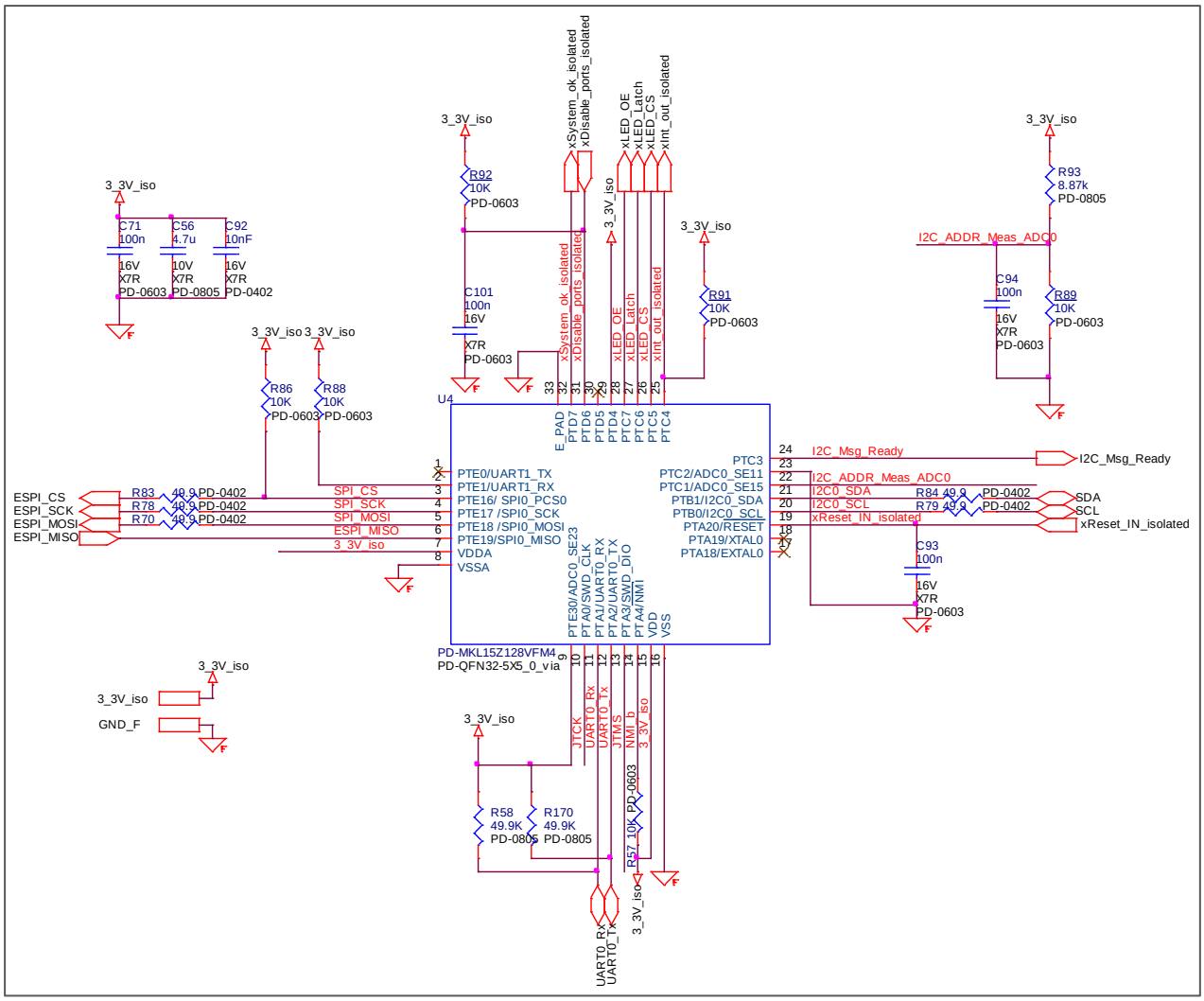

Figure 8: PD69200 PoE Controller Circuitry

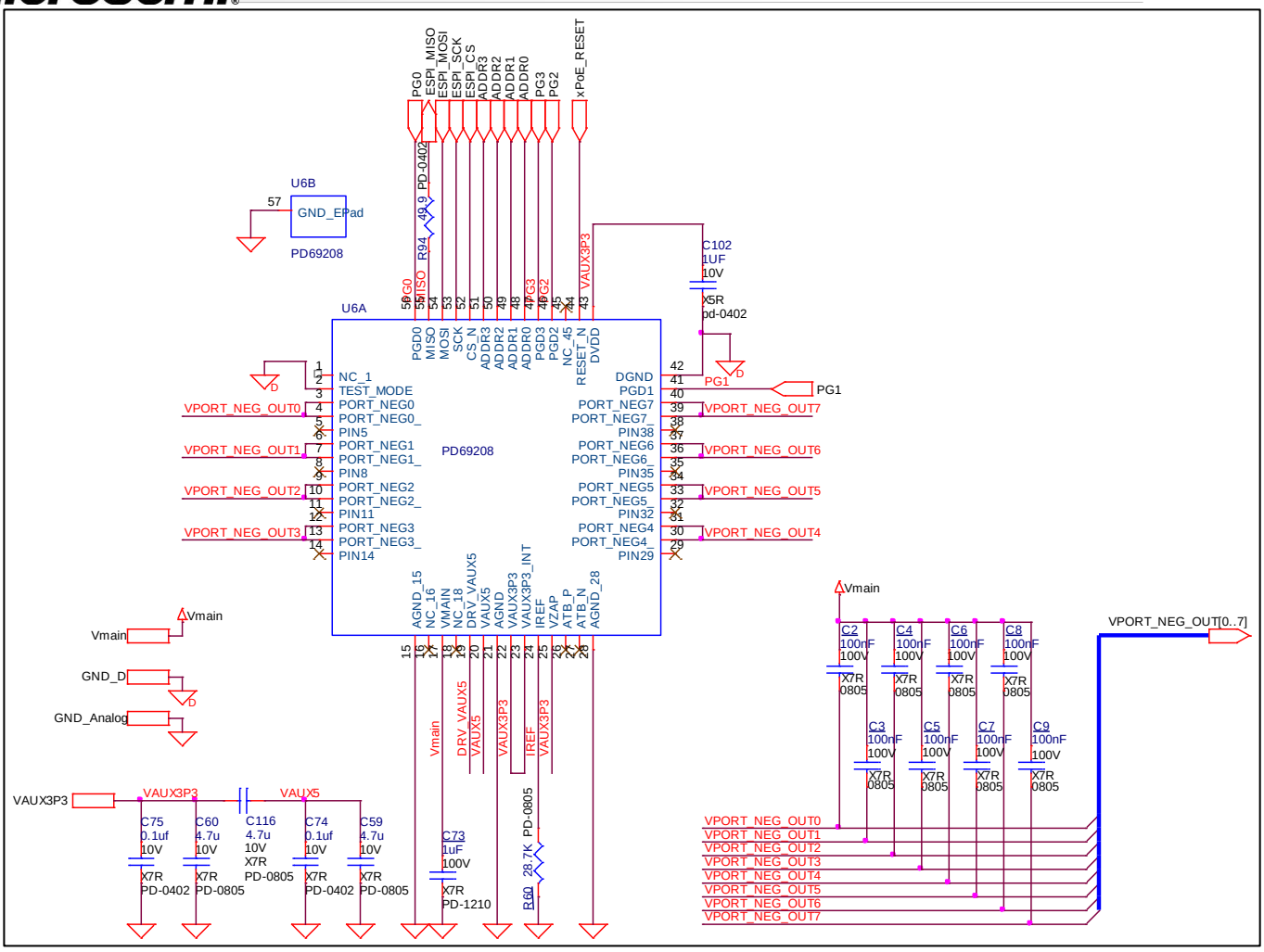

Figure 9: PD69208 Circuitry for PoE Manager #0 (6 PL)

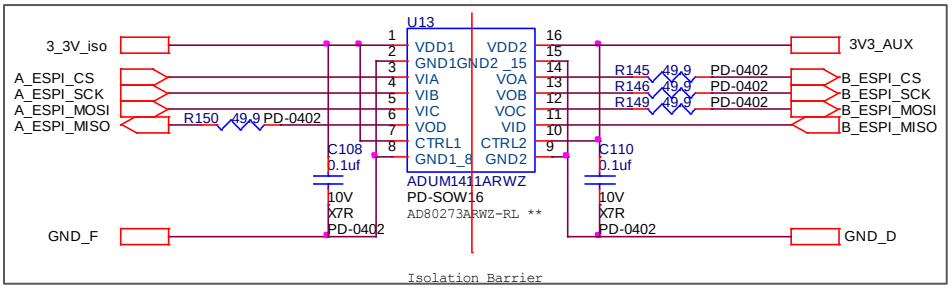

Figure 10: Digital Isolator

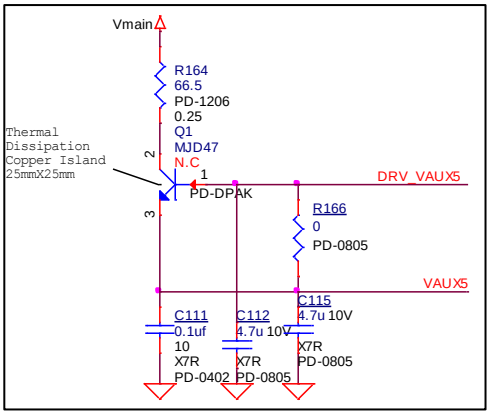

Figure 11: Boost Transistor to the 5VDC Regulator

Bill of Materials for a PoE System

Block	Qty	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
MAIN	4	C52,C53,C54,C55	47uF 100V 20% 8X11.5 105C	D8H11_5F3_5	Rubycon	100PX47M T7 8X11.5
	4	C95,C97,C99,C100	Cap X7R, 1nF 50V 10% 0402	PD-0402	Murata	GRM155R71H102KA01D
	1	C51	CAP 0.1uF 10V X7R 10% 0402	PD-0402	Murata	GRM155R71C104KA88D
	4	D55,D57,D59,D60	DIO SCHOTTKY 40V 1A SMAT	PD-SMA	Diodes Inc.	B140
	2	R80,R85	3.65K 125mW 1%0402	PD-0402	Yageo	RC0402FR-073K65L
	4	R169,R151,R171,R172	10K 1% 62.5mW 0402	PD-0402	Vishay	CRCW0402-10K01%ET1 E3
	2	C108,C110	CAP 0.1uF 10V X7R 10% 0402	PD-0402	Murata	GRM155R71C104KA88D
	4	R145,R146,R149,R150	49.9R 1% 62.5mW 0402	PD-0402	Yageo	RC0402FR-0749R9L
	1	U13	IC Dig.Isol SO16^	PD-SOW16	Analog Devices	AD80273ARWZ-RL **

Table 2: Main Block Components

Block	Qty	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
PD69200-PoE Controller	4	C71,C93,C94,C101	CAP 100nF 16V 10% X7R 0603	PD-0603	Samsung	CL10B104KO8NNNC
	1	C56	CAP 4.7uF 10V 10% X5R 0805	PD-0805	Taiyo Yuden	LMK212BJ475KD-T
	1	C92	Cap X7R 10nF 16V 10% 0402	PD-0402	Samsung	CL05B103KB5NNNC
	6	R57,R86,R88 R89,R91,R92	10K 62.5mW 1% 0603	PD-0603	Samsung	RC1608F1002CS
	1	R58,R170	49.9K 125mW 1% 0805	PD-0805	Rohm	MCR10-EZHEF-4992
	5	R70,R78,R83,R79,R84	49.9R 1% 62.5mW 0402	PD-0402	Yageo	RC0402FR-0749R9L
	1	R93	8.87K 125mW 1% 0805	PD-0805	Yageo	RC0805FR-078K87-L
	1	U4	MCU ARM CORTEX 128KB 32QFN 48Mhz	PD-QFN32-5X5_0_VIA	Freescale Semiconductor	MKL15Z128VFM4

Table 3: PoE Controller Components

Block	Qty*	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
PoE Manager	9	C2-C9	CAP 100nF 100V 10% X7R 0805	PD-0805	Samsung	CL21B104KCFSFNE
	3	C59,C60,C116	CAP 4.7uF 10V 10% X5R 0805	PD-0805	Murata	GRM219R61A475KE19D
	2	C74,C75	CAP 0.1uF 10V X7R 10% 0402	PD-0402	Murata	GRM155R71C104KA88D
	1	C102	CAP 1.0UF 10V X5R 10% 0402	pd-0402	Panasonic	ECJ-0EB1A105M
	1	C73	CAP 1uF 100V X7R 10% 1210	PD-1210	AVX	12101C105KAT2A
	1	R60	28.7K 125mW 1% 0805 (For PoH 99W should be 0.1%)	PD-0805	Vishay	CRCW080528K7FKEA
	1	R94	49.9R 1% 62.5mW 0402	PD-0402	Bourns	CR0402-FX-49R9-ELF
	1	U6	8 Port PSE PoE Manager SMT	PD-MLF56-HS	Microsemi	PD69208

Table 4: PoE Manager Components

*These quantities should be multiplied by the number of PD69208 (six managers in this paper)
**Special part number for Microsemi PoE application; preferential pricing for Microsemi customers.
***Fuses per port are not required for use in circuits with total power level of up to 3kW. That's because PD69208 is UL 2367 (category QVRQ2) recognized component and fulfills limited power source (LPS) requirements of latest editions of IEC60950-1 and EN60950-1.

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Layout Guidelines

This section provides detailed information and PCB design guidelines for the implementation of a 48-port Power over Ethernet (PoE) system, based on Microsemi's™ 8-channel PoE Manager- the PD69208.

Isolation and Termination

According to the IEEE 802.3af and the IEEE802.3at standard, certain isolation requirements need to be met in all PoE equipment. In addition, EMI limitations should be considered, as specified in the FCC and European EN regulations.

These requirements are taken into account by PoE switch vendors, while designing the switch circuitry. However, when a PoE Manager is integrated into a switch, special design considerations must be met, due to the unique combination of data and power circuitries.

The following paragraphs define these requirements and provide recommendations for their implementation, so as to assist designers in meeting those requirements and in integrating the Microsemi's PoE Chip Set and the daughter boards.

Isolation

As specified in the IEEE PoE standards, 1500 Vrms isolation is required between the switch's main board circuitry including protective and frame ground and the Media Dependent Interface (MDI). Figure 12 illustrates the overall isolation requirements.

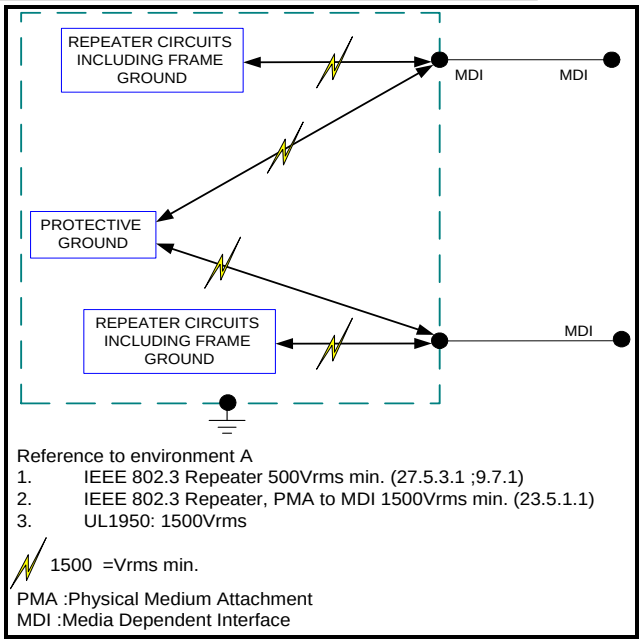

Figure 12: Isolation Requirements

High Voltage Isolation

- For a switch with no PoE circuitry: isolation requirements between the physical inputs and the data connectors are met by using an isolated AC/DC power supply and isolated pulse transformers (see Figure 13).
- When integrating a PoE circuitry into a switch, the output power can be supplied through the central tap of the pulse transformer's secondary side (unless power is provided over the spare pairs). This connectivity can bypass the pulse transformer's isolation, if the PoE ground or DC input is connected to the switch's circuitry/ground.

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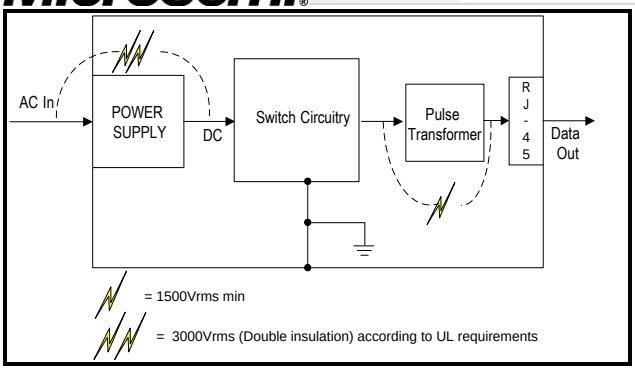

Figure 13: Standard Switch Circuitry

To comply with the above isolation requirements, the PoE managers must be isolated in regards to all other switch circuitries. Use one of the following methods:

- A separate DC input for the switch and the PoE circuitry and isolated serial communication between the PoE circuitry and the switch circuitry (see Figure 14).
- A single DC input (separate power supplies) for both the switch and PoE circuit as well as additional or integrated isolated DC/DC circuitry for the switch input and isolated serial communication port between the PoE circuitry and the switch's circuitry (see Figure 15).

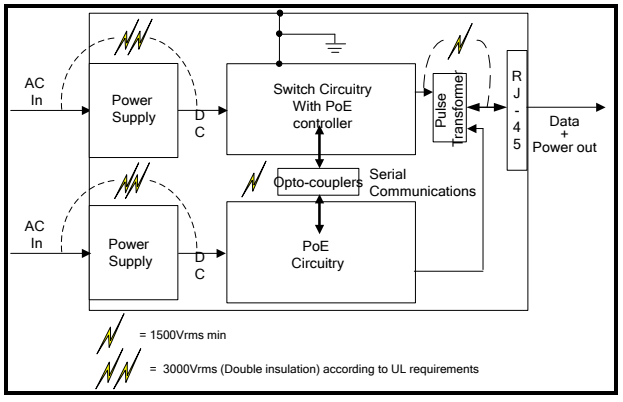

Figure 14: Switch Circuitry with Two DC Source

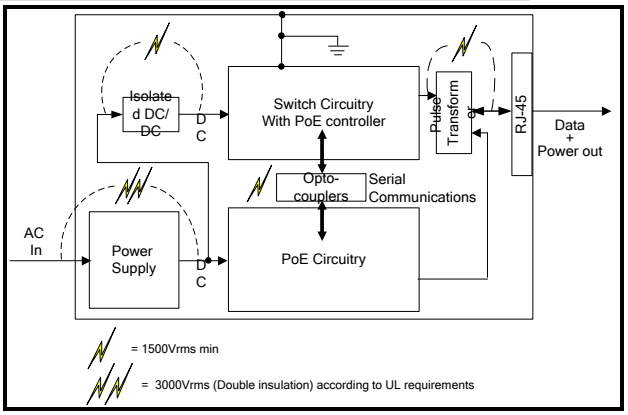

Figure 15: Switch Circuitry with a Single DC Source

To maintain 1500 Vrms isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is recommended, to provide a safe margin for hi-pot requirements.

PoE Output Ports Filtering and Terminations

A switch normally creates a noisy environment. To meet EMI requirements, high filtering and line terminations may be needed when connecting the PoE circuit outputs to the switch circuitry (see Figure 16). Note that in most PoE systems, it is recommended to use 0 Ω resistors for R1 and R2. However, certain systems may benefit from 75 Ω resistors. Filtering provisions should be made. Note that in quiet PoE systems the EMI filter can be replaced (bypassed) using R3 and R4.

A circuitry for the recommended filter includes:

- A common mode choke for conducted EMI performances (such as ICE CS01 series)
- Output differential cap filter for radiated EMI performances
- Y-capacitive/resistive network to chassis

Since each system is a unique EMI case, this circuit is a good starting point for EMI suppression.

Note For best EMI performance and to avoid additional noise accumulated on the lines between the filter and the port connectors, it is recommended to implement this circuitry on the switch's main board, located as close as possible to the port connectors.

As specified in the IEEE PoE standards, PoE output power can be supplied over the data pairs or the spare pairs. Both methods are detailed in Figure 17 which illustrates an MDI-X (or Auto MDI-X) connection associated with the switch.

Isolating the Stacked Modular Jack Assembly

The IEEE PoE standards require 1500 Vrms isolation between PoE voltages and frame ground (EGND). Notice that RJ-45 jack assemblies have a metal cover that 80 mils almost reaches to the PCB surface.

Maintain an 80 mils traces clearance between EGND traces for the RJ-45 modular jack assembly metal covering and adjacent circuit paths and components. To prevent 1500 Vrms isolation violation, it is necessary to provide layout clearances of PoE traces on the top layer, in the vicinity of the RJ-45 connector assemblies.

PoE technology involves voltages as high as VDC. Thus, plan adjacent traces for 100 VDC operational creepage. Operational creepage should be maintained to prevent breakdown between traces carrying these potentials.

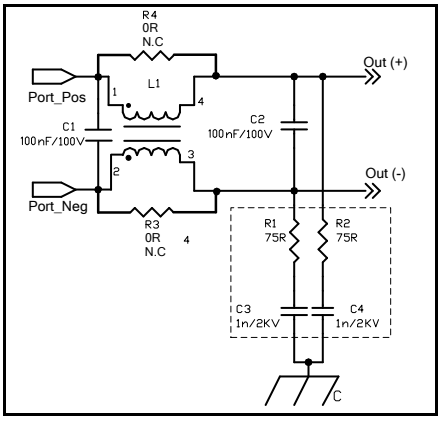

Figure 16: Recommended EMI Filter

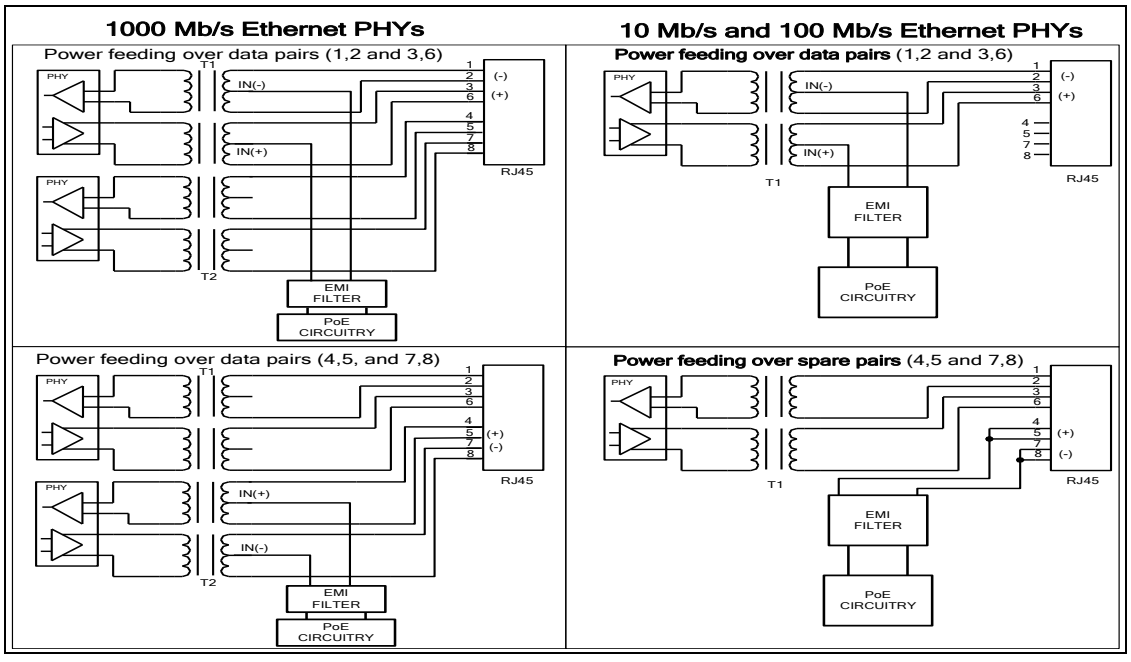

Figure 17: Output Ports Design Details

Layout Guidelines

Microsemi's PD69208 PoE Manager is designed to simplify the integration of PoE-circuitry, based on the IEEE PoE standards, into switches. The pin-out arrangement has been configured for optimal PCB routing.

Figure 18 describes the various circuits and elements surrounding the PD69208 PoE Manager in the block diagram. This block diagram includes the following peripheral elements, identified by numbers:

- 5 V Voltage source (VAUX5) (1)
- 3.3 V Voltage source (VAUX3P3) (2)
- Power Good Inputs (3)
- Output capacitor used for filtering (4)
- ESPI Bus, ESPI Address Lines (5)
- Vmain input (6)
- AGND – Analog ground (7)

Note The VAUX5 supply may include an external transistor connected to pin 20, destined to increase current drive for external circuitry. To prevent heat from being transferred to the PD69208, place this transistor away from the PoE Managers.

Locating PoE Circuitry in a Switch

To minimize the length of high current traces, as well as RFI pick-up, place the PoE circuitry as close as possible to the switch's pulse transformers. The circuit can be fully integrated into the switch's PCB, or can be easily placed on top of the switch's using daughter board. Typical integration of PoE modules inside a switch is shown in Figure 20 and Figure 21.

Ground and Power Planes

Since the PoE solution is a mixed-signal (analog and digital) circuitry, special care must be taken when routing the ground and power signals lines.

The reference design assumes a four layer board: top, mid1, mid2, bottom. The main planes are Vmain/AGND, DGND.

Ground planes are crucial for proper operation and should be designed in accordance with the following guidelines, as illustrated in Figure 22:

- Separate analog and digital grounds, with a gap of at least 40 mils
- Analog ground plane (AGND) is utilized to transfer the heat generated by the PD69208 (see Thermal Pad Definition and Design).
- The AGND should be located on external layer
- Earth ground is used to tie in the metal frame of the RJ-45 connectors. This ground is to be routed separately and connected to the switch's metal chassis/enclosure
- To prevent ground loop currents, use only a single connection point between the digital and analog grounds as shown in Figure 22.
- To connect various DGND points and to enable stable impedance to the ESPI bus traces, extend the digital ground (DGND) surface under pins 41 – 56 of the PD69208 Managers
- A focal interconnection point for the digital and analog grounds should be located at about the middle of the overlapping section
- Leave spacing for a ceramic 1 nF bypass capacitor + two parallel and inversed Schottky diodes near each PoE Manager (Figure 23) between the analog and digital layers. The capacitors form low impedance paths for digital driving signals

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- The power and return (ground) planes for the 48V supply must be designed to carry the system maximum continuous current, based on the design capacity. Minimize DC power losses on these planes by using a wide copper lands. When implementing the PoE circuitry on a daughter board, the high current does not have to be routed through the daughter board but only the return path as can be note from Figure 19

Current Flow through the PoE application

See Figure 19

The port's DC current flows in an application utilizing a PoE daughter board (DB) as follow:

1. Coming from the switch's power supply positive to the center taps of the line transformer via a mother board wide trace (not through the DB)

2. From the center tap of the line transformer via the switch's RJ45 to the PD side

3. The return current from the PD flows via the RJ45 and the line transformer to the DB PoE circuitry.

4. From the DB analog ground (AGND) the current flows back to the switch's power supply negative via harness

Note The positive port's heavy current flows directly to the PD side without going through the PoE Managers on the DB.

Specific Component Placement

Peripheral Components

To minimize heat transfer among various components a gap between them should be maintained. The following are suggested gaps however any gap can be used as long as the designer monitors the thermal performance during the design and follows the maximum temperatures allowed at the various components.

- Minimum gap between PD69208 ICs should be 50mm
- Minimum gap between PD69208 to PoE controller should be 30mm
- Minimum gap between PD69208 to NPN transistor regulator (if used) should be 50mm.

PoE Controller and Peripherals

Refer to the Freescale Semiconductor MKL15Z128VFM4 Data Sheet, for recommendations related to the PoE controller layout guidelines.

The following guidelines are destined for the integration of the PoE Controller into a PoE circuit.

- Locate the filtering capacitors for VDD and for VDDA close to power and ground pins.
- Termination resistors for the outgoing ESPI digital lines should be located close to the respective driving pins.

PD69208 PoE Manager and Peripherals

- The side of the PoE Manager that includes pins 41 to 56 should face the digital ground (DGND plane.) The pins function as communication and control pins for the Manager (connect between the PoE Manager and the PoE controller via isolation circuitry)
- Locate the bypass capacitors for the PoE Manager supply input close to the relevant pin. In cases where two bypass capacitors are placed on the same line, locate the lower value capacitor closer to the pin on the same layer and place the higher value capacitor at a more distant location.

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- Locate VAUX5 and VAUX3P3 0.1 µF and 4.7 µF filtering capacitors as close as possible to the PoE Manager pins 20 and 22 respectively.

Vmain Capacitors

It's a good design to have 3 x 47uF capacitors over Vmain in order to prevent noise and spikes events to penetrant into Vmain rail.(note 4 Figure 7).

Conductor Routing

General Guidelines

Conductor (or printed lands) routing is to be performed as practiced in general layout guidelines, specifically:

- Conductors that deliver a digital signal are to be routed between the analog and the digital ground planes.
- Avoid routing analog signals above the digital ground.

Specific Requirements for Clock and Sensitive Signals

Issues that require special design considerations:

- The IREF resistor (connects to pin 24), used for current reference, is directly connected to AGND and pin 24 using the shortest path.
- Carefully route the ESPI communication clock (SCK) line coming from the PoE Controller so that it will not disturb other lines. Two ground lines (connected to DGND) could be routed alongside the clock line to isolate it from the rest of the lines.

Port Outputs

For robust design, the ports output traces are to be 45-mil wide so as to handle maximum current and port power.

- However to obtain a 10° C (maximum) copper rise under 1A per port, set the minimum width for traces in accordance with the layer location and copper thickness:
- For two ounce copper, external layer: 15 mils
- For two ounce copper, internal layer: 20 mils
- For one ounce copper, external layer: 25 mils
- For one ounce copper, internal layer: 40 mils
- For 1/2 ounce copper, external layer: 30 mils
- For 1/2 ounce copper, internal layer: 55 mils (20° C copper rise)
- The ports output traces must be short and parallel to each other, to reduce RFI pickup and to keep the series resistance low.
- The PoE ports outputs must be connected to the switch's pulse transformers as shown in Figure 17. The common mode choke and 'Bob-Smith' termination (resistor-capacitor) to chassis ground are optional and used to reduce RFI noise. The circuit is to be located as close as possible to the pulse transformer.

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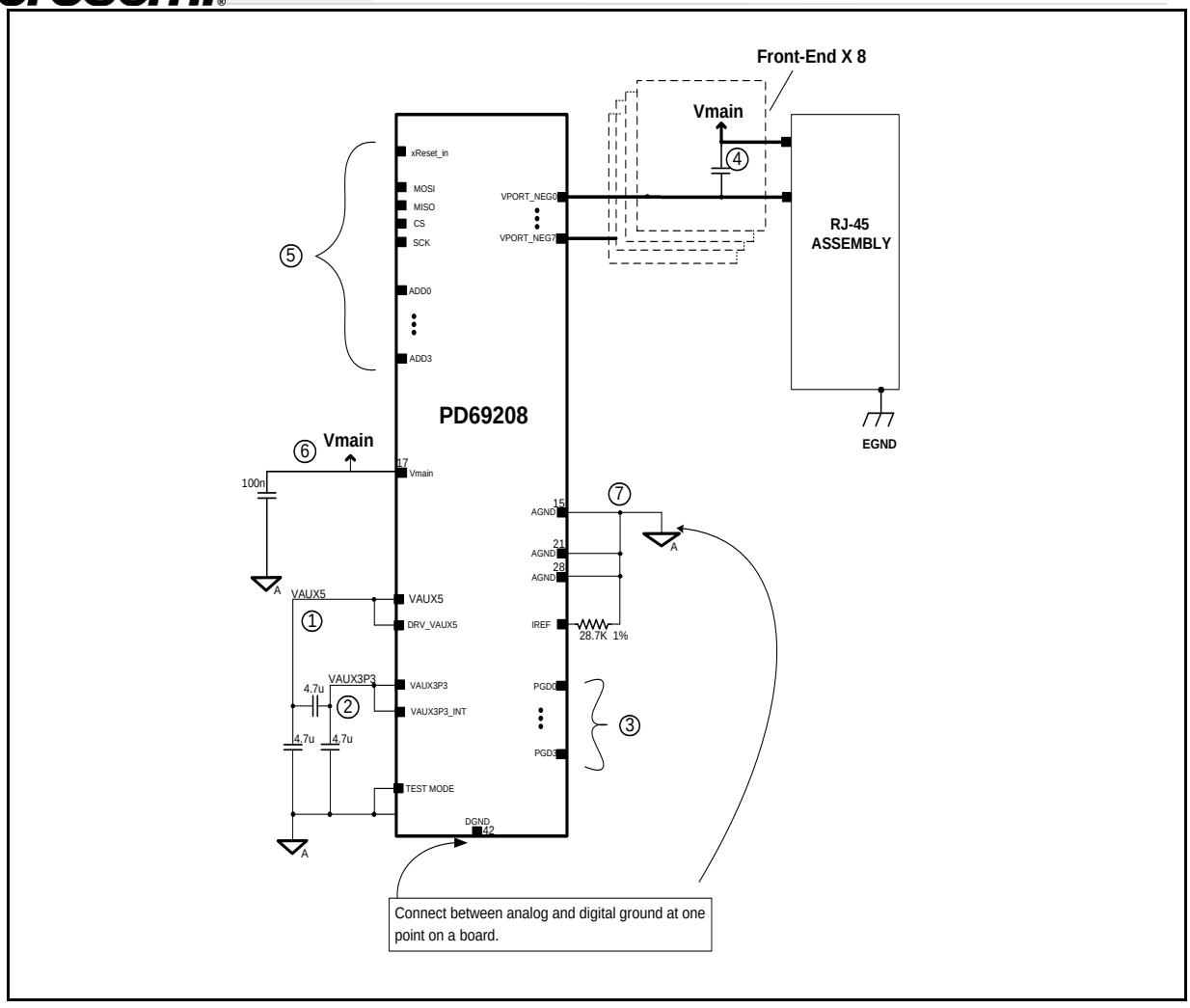

Figure 18: Component Identification for PD69208 Circuitry

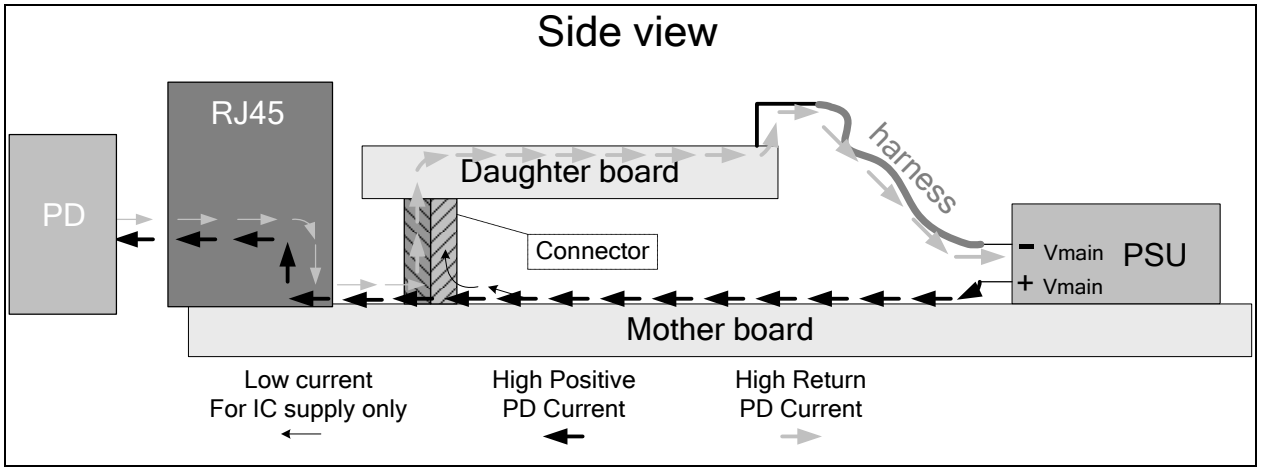

Figure 19: Component Identification for PD69208 Circuitry

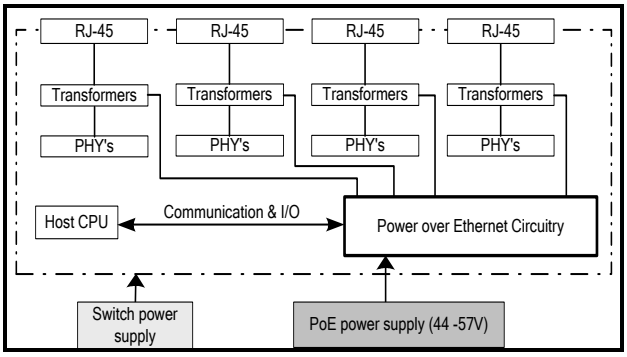

Figure 20: Block Diagram - PoE Circuitry Inside the Switch

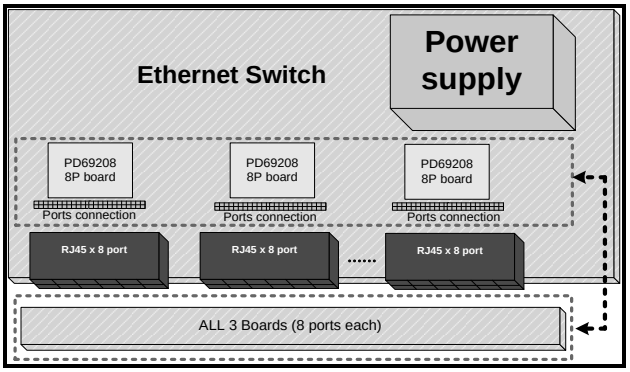

Figure 21: PoE DB Circuitry Inside the Switch

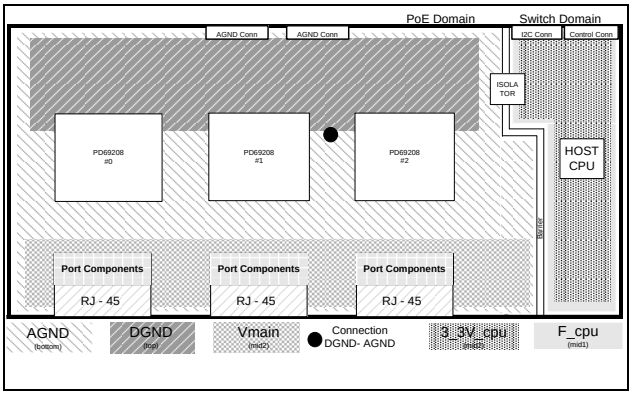

Figure 22: Ground and Power Planes

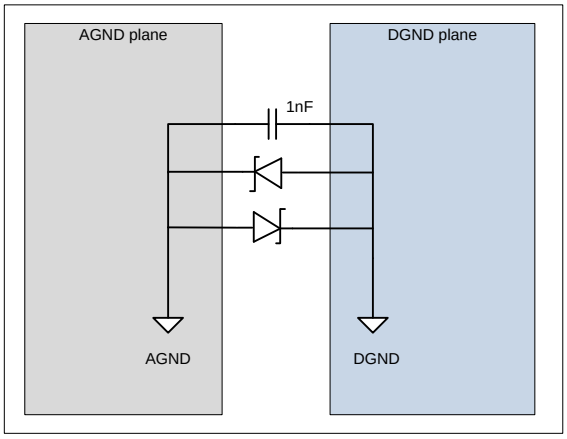

Figure 23: Grounding scheme

Thermal Pad Definition and Design

The PD69208 utilizes a thermal dissipation exposed pad in a 56-pin 8 x 8 mm QFN package. The package is molded in such a way that the lead frame is exposed at the bottom surface of the package.

Direct soldering of the exposed pad to a copper land provides an efficient thermal path. In multilayer board designs, a matrix of 6x6 vias thermally connects the exposed pad to the AGND copper planes.

Requirements

The PCB design should consider the exposed pad of the PD69208. This pad is used for thermal cooling of the package. Basically, the PCB should be designed as shown in Figure 25- Figure 28.

In these figures the PD69208 pad is soldered to a dedicated area on the PCB. This contact area is composed of a 36 vias array, each penetrating and thermally connecting to large ground areas in the PCB at various planes, providing efficient heat dissipation.

To ensure optimum thermal transfer through the thermal vias to internal planes or to the bottom side of the PCB, the vias system **should not be used** as used in web construction techniques. Web construction for PCB vias is a standard technique used to facilitate soldering, by designing the via to achieve high thermal resistance. This is not desirable for heat dissipation from the PD69208 package. It is recommended that vias used under the PD69208 package be internally connected to the planes, using continuous connection surrounding the whole diameter.

Thermal Pad Design

The PD69208 exposed pad is a metal substrate on the bottom of the package. The attachment process for the exposed pad package is equivalent to standard surface mount packages.

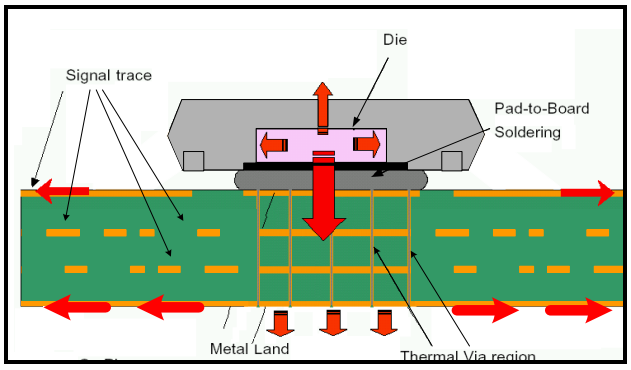

Figure 24: Heat Dissipation in PCB

See Figure 25 and Figure 26 (CS & PS) for a design layout of the recommended contact pad.

For proper heat dissipation, the following footprint / layout guidelines must be followed:

- All thermal vias are to be connected to the AGND area under the PD69208
- Via diameter should be approximately 0.3 mm with one ounce copper barrel plating. Solder flow into the vias from the component side can result in voids during the solder process and this must be avoided.

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- If copper plating does not plug the vias, apply stencil print solder paste onto the printed circuit side. This provides sufficient solder paste, filling those vias to avoid the above mentioned voids. Figure 27 and Figure 28 show the associated, solder printing masks (CS & PS). The solder mask openings are lined-up in respect to the 6 x 6 thermal via array. Since large solder printing mask openings may result in poor release, the opening should be subdivided as shown in these figures.
- For a nominal package standoff of 0.1 mm, a solder mask stencil thickness of 5 mils should be considered.

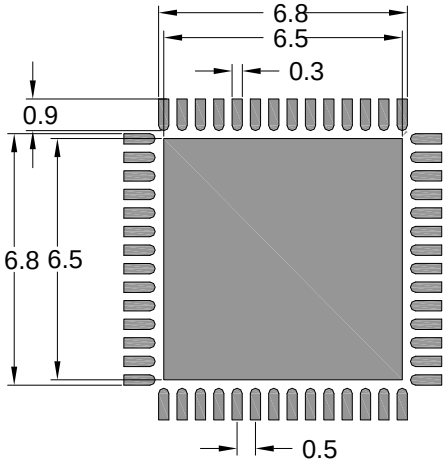


Figure 25: Thermal Pad Array Footprint (CS)

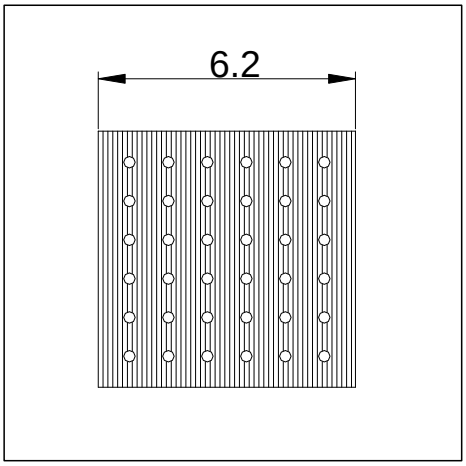


Figure 26: Thermal Pad Array Footprint (PS)

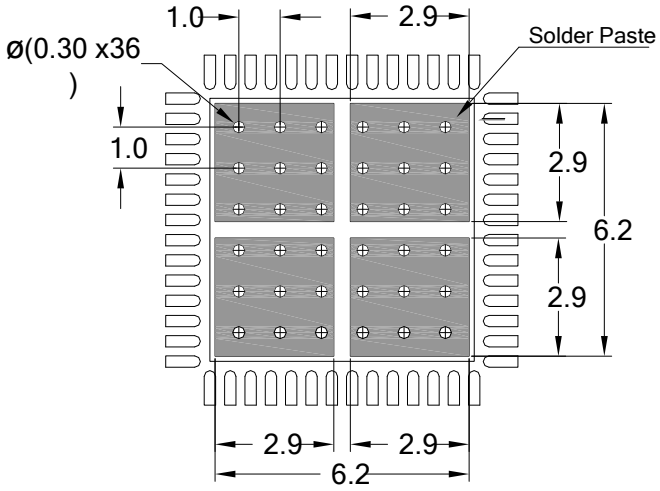


Figure 27: Top Solder Printing Mask (CS)

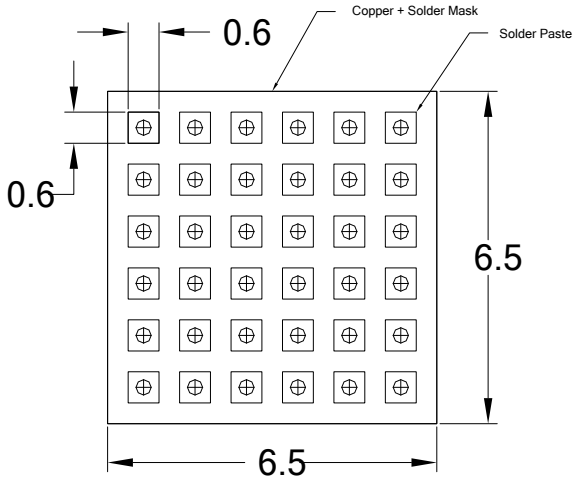
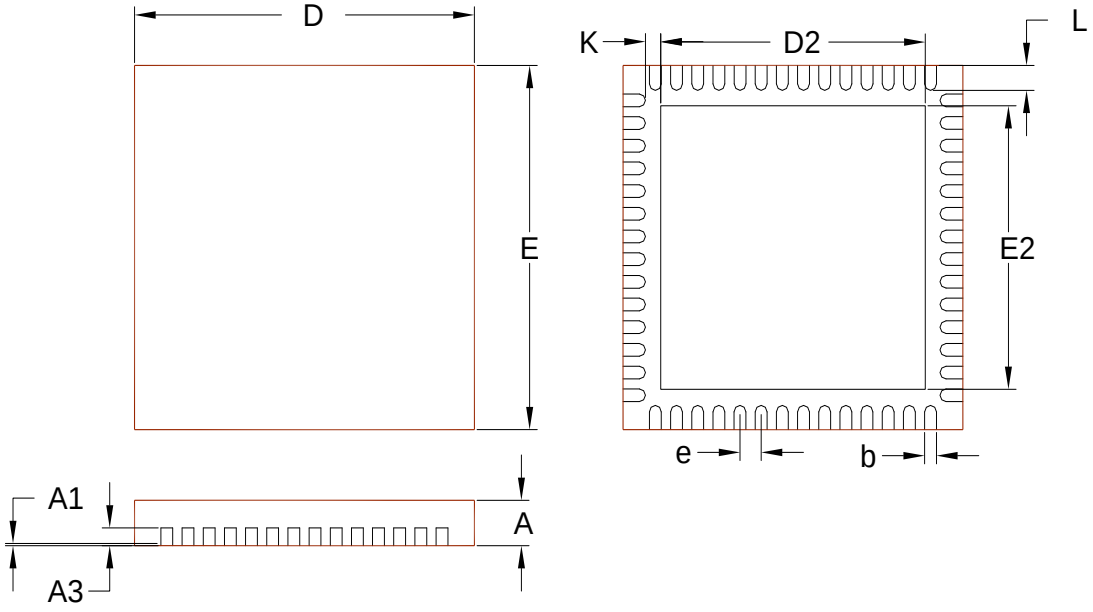


Figure 28: Bottom Solder Printing Mask (PS)

All dimensions are in mm.



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.50	6.75	0.256	0.267
E2	6.50	6.75	0.256	0.267
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

Figure 29: Package Outline Drawing 56 Pin QFN 8x8 mm

Note:

1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in millimeters, inches for reference only.

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Revision History

Revision Level / Date	Para. Affected	Description
0.1 / 11 Dec 2013	-	Preliminary Version Initial Release
0.2 / March 2014		Change Rref to 28.7K
0.3 / March 2014		Change output capacitors to 220nF
0.4 / May 2014		Page 6 – adding note at chapter about "Reference Current Source" that in PoH system the precision resistor should be 0.1%
0.5 /Nov 2014		Vmain capacitors – recommendation – page 21
1.0 /Jan 2015		General structural changes Adding PD69204 Adding comment on page 6 - output capacitor can be between 22nF to 220nF
1.1/Feb 2016		Fixing broken links and paragraphs Updating reference to communication protocol "PD69200_UG_COMM_PROT"
1.2/Nov 2016		• General udpates • Adding capacitor 4.7uF between VAUX5 to VAUX3P3, minimize time delay between the 5V and 3.3V rise.

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