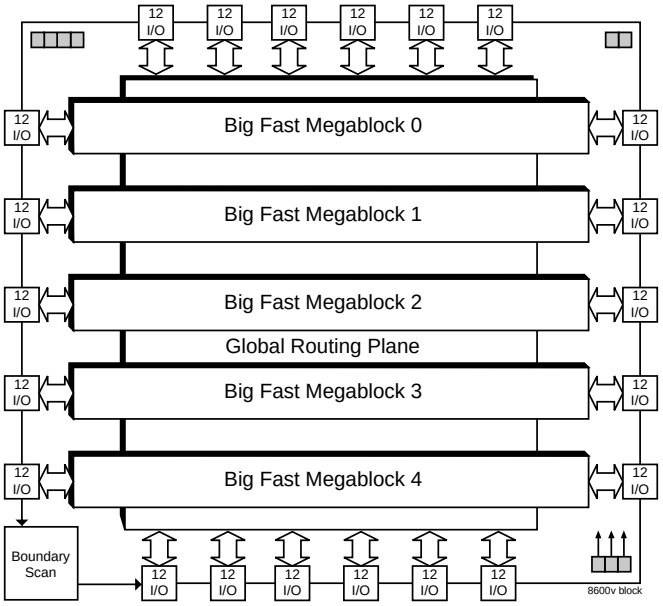
ispLSI® 8600V

3.3V In-System Programmable SuperBIG™ High Density PLD

Features

- **SuperBIG HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - **— 3.3V Power Supply**
  - **— 32,000 PLD Gates/600 Macrocells**
  - **— 192-264 I/O Pins Supporting 3.3V/2.5V I/O**
  - **— 864 Registers**
  - **— High-Speed Global and Big Fast Megablock (BFM) Interconnect**
  - **— Wide 20-Macrocell Generic Logic Block (GLB) for High Performance**
  - **— Wide Input Gating (44 Inputs per GLB) for Fast Counters, State Machines, Address Decoders, Etc.**
  - **— PCB-Efficient Ball Grid Array (BGA) Package Options**
- **HIGH-PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 125 MHz Maximum Operating Frequency**
  - **— t_{pd} = 8.5 ns Propagation Delay**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— Programmable Speed/Power Logic Path Optimization**
- **IN-SYSTEM PROGRAMMABLE**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE AND 3.3V IN-SYSTEM PROGRAMMABLE**
- **ARCHITECTURE FEATURES**
  - **— Enhanced Pin-Locking Architecture, Symmetrical Generic Logic Blocks Connected by Hierarchical Big Fast Megablock and Global Routing Planes**
  - **— Product Term Sharing Array Supports up to 28 Product Terms per Macrocell Output**
  - **— Macrocells Support Concurrent Combinatorial and Registered Functions**
  - **— Embedded Tristate Bus Can Be Used as an Internal Tristate Bus or as an Extension of an External Tristate Bus**
  - **— Macrocell and I/O Registers Feature Multiple Control Options, Including Set, Reset and Clock Enable**
  - **— I/O Pins Support Programmable Bus Hold, Pull-Up, Open-Drain and Slew Rate Options**
  - **— Separate VCCIO Power Supply to Support 3.3V or 2.5V Input/Output Logic Levels**
  - **— I/O Cell Register Programmable as Input Register for Fast Setup Time or Output Register for Fast Clock to Output Time**
- **ispDesignEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **— Superior Quality of Results**
  - **— Tightly Integrated with Leading CAE Vendor Tools**
  - **— Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **— PC and UNIX Platforms**

Functional Block Diagram



ispLSI 8000V Family Description

The ispLSI 8000V Family of Register-Intensive, 3.3V SuperBIG In-System Programmable Logic Devices is based on Big Fast Megablocks of 120 registered macrocells and a Global Routing Plane (GRP) structure interconnecting the Big Fast Megablocks. Each Big Fast Megablock contains 120 registered macrocells arranged in six groups of 20, a group of 20 being referred to as a Generic Logic Block, or GLB. Within the Big Fast Megablock, a Big Fast Megablock Routing Pool (BRP) interconnects the six GLBs to each other and to 24 Big Fast Megablock I/O cells with optional I/O registers. The Global Routing Plane which interconnects the Big Fast Megablocks has additional global I/Os with optional I/O registers. The 192-I/O version contains 72 Big Fast Megablock I/O and 120 global I/O, while the 264-I/O

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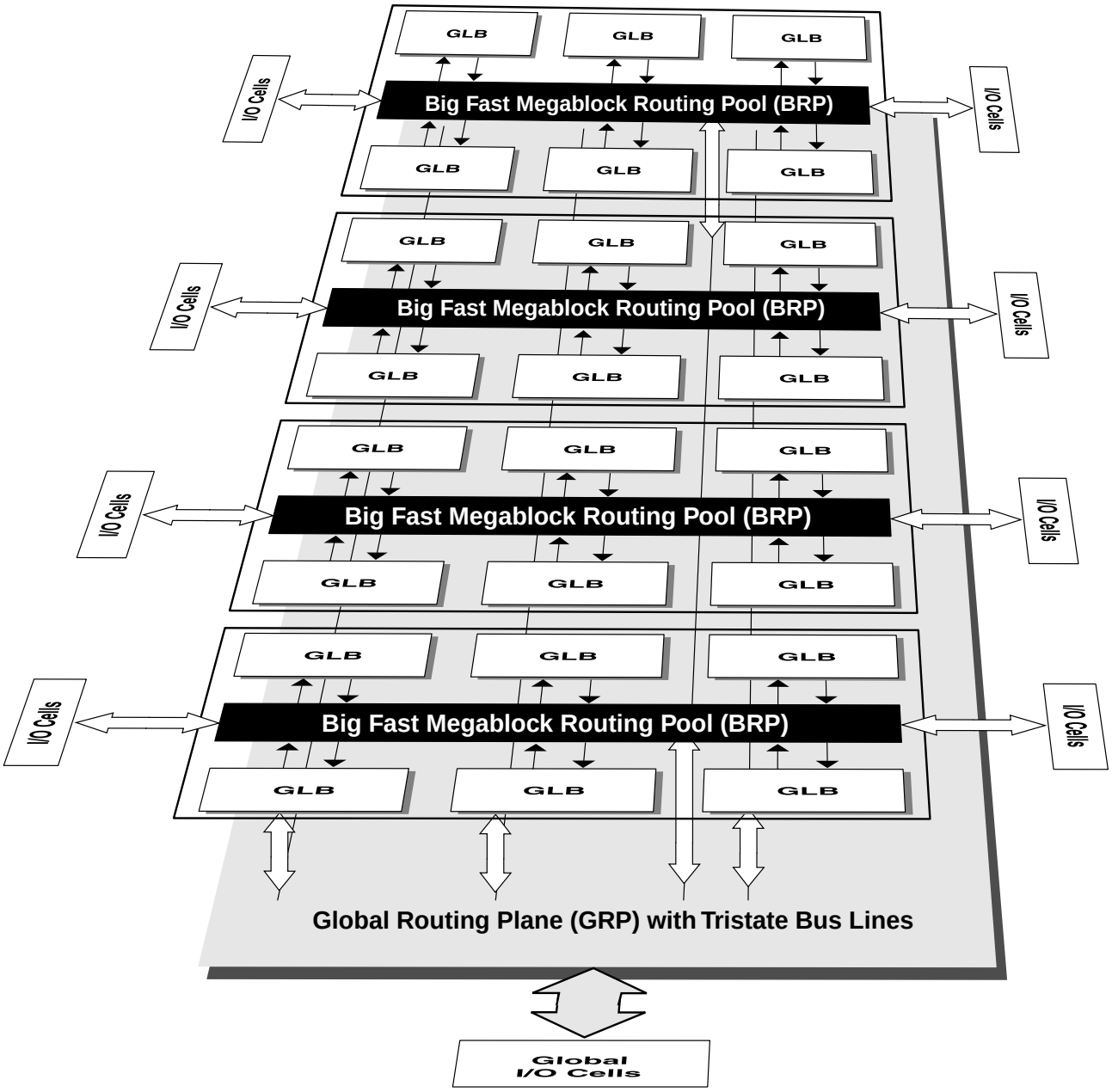
Functional Block Diagram

Figure 1. ispLSI 8600V Functional Block Diagram (Perspective)



ispLSI 8000V Family Description (Continued)

version contains 120 Big Fast Megablock I/O and 144 global I/O.

Outputs from the GLBs in a Big Fast Megablock can drive both the Big Fast Megablock Routing Pool within the Big Fast Megablock and the Global Routing Plane between the Big Fast Megablocks. Switching resources are provided to allow signals in the Global Routing Plane to drive any or all the Big Fast Megablocks in the device. This mechanism allows fast, efficient connections, both within the Big Fast Megablocks and between them.

Each GLB contains 20 macrocells and a fully populated, programmable AND-array with 82 logic product terms. The GLB has 44 inputs from the Big Fast Megablock Routing Pool which are available in both true and complement form for every product term. Up to 20 of these inputs can be switched to provide local feedback into the GLB for logic functions that require it. The 80 general-purpose product terms can be grouped into 20 sets of four and sent into a Product Term Sharing Array (PTSA) which allows sharing up to a maximum of 28 product terms for a single function. Alternatively, the PTSA can be bypassed for functions of four product terms or less.

The 20 registered macrocells in the GLB are driven by the 20 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch/toggle flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. Each macrocell has two outputs, one output can be fed back inside the GLB to the AND-array, while the other output drives both the Big Fast Megablock Routing Pool and the Global Routing Plane. This dual output capability from the macrocell allows efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function.

Macrocell registers can be clocked from one of several global, local or product term clocks available on the device. A global, local and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers. Reset and preset for the macrocell register is provided from both global and product term signals. The polarity of all of these control signals is selectable on an individual macrocell basis. The macrocell register can be programmed to operate as a D-type register, a D-type flow-through latch or a T-type flip flop.

The 20 outputs from the GLB can drive both the Big Fast Megablock Routing Pool within the Big Fast Megablock and the Global Routing Plane between the Big Fast Megablocks. The Big Fast Megablock Routing Pool contains general purpose tracks which interconnect the six GLBs within the Big Fast Megablock and dedicated tracks for the signals from the Big Fast Megablock I/O cells. The Global Routing Plane contains general purpose tracks that interconnect the Big Fast Megablocks and also carry the signals from the I/Os connected to the Global Routing Plane.

Control signals for the I/O cell registers are generated using an extra product term within each GLB, or using dedicated input pins. Each GLB has two extra product terms beyond the 80 available for the macrocell logic. The first additional product term is used as an optional shared product term clock for all the macrocells within the GLB. The second additional product term is then routed to an I/O Control Bus using a separate routing structure from the Big Fast Megablock Routing Pool and Global Routing Plane. Use of a separate control bus routing structure allows the I/O registers to have many control signals with no impact on the interconnection of the GLBs and Big Fast Megablocks. The I/O Control Bus is split into four quadrants, each servicing the I/O cell control requirements for one edge of the device. Signals in the control bus can be independently selected by any or all I/O cells to act as clock, clock enable, output enable, reset or preset.

Each Big Fast Megablock has 24 I/O cells. The Global Routing Pool has 144 I/O cells. Each I/O cell can be configured as a combinatorial input, combinatorial output, registered input, registered output or bidirectional I/O. I/O cell registers can be clocked from one of several global, local or product term clocks which are selected from the I/O control bus. A global and product term clock enable is also provided, eliminating the need for the user to gate the clock to the I/O cell registers. Reset and preset for the I/O cell register is provided from both global and product term signals. The polarity of all of these control signals is selectable on an individual I/O cell basis. The I/O cell register can be programmed to operate as a D-type register or a D-type latch.

The input thresholds are fixed at levels which comply with both 3.3V and 2.5V interfaces. The output driver can source 4mA and sink 8mA (3.3V output supply). The output drivers have a separate VCCIO power supply which is independent of the main VCC supply for the device. This feature allows the output drivers to run from either 3.3V or 2.5V while the device logic is always

ispLSI 8000V Family Description (Continued)

powered from 3.3V. The output drivers also provide individually programmable edge rates and open drain capability. A programmable pullup resistor is provided to tie off unused inputs and a programmable bus-hold latch is available to hold tristate outputs in their last valid state until the bus is driven again by another device.

The ispLSI 8000V Family features 3.3V, non-volatile in-system programmability for both the logic and the interconnect structures, providing the means to develop truly reconfigurable systems. Programming is achieved through the industry standard IEEE 1149.1-compliant Boundary Scan interface using the JTAG protocol. Boundary Scan test is also supported through the same interface.

An enhanced, multiple cell security scheme is provided that prevents reading of the JEDEC programming file when secured. After the device has been secured using this mechanism, the only way to clear the security is to execute a bulk-erase instruction.

ispLSI 8600V Description

The ispLSI 8600V device has five Big Fast Megablocks for a total of 5 x 120 = 600 macrocells.

Each Big Fast Megablock has a total of 24 I/O cells and the Global Routing Plane has a total of 144 I/O cells. This gives (5 x 24) + 144 = 264 I/Os for the full I/O version, while the partial I/O version contains 72 BFM I/O + 120 Global I/O = 192 I/Os.

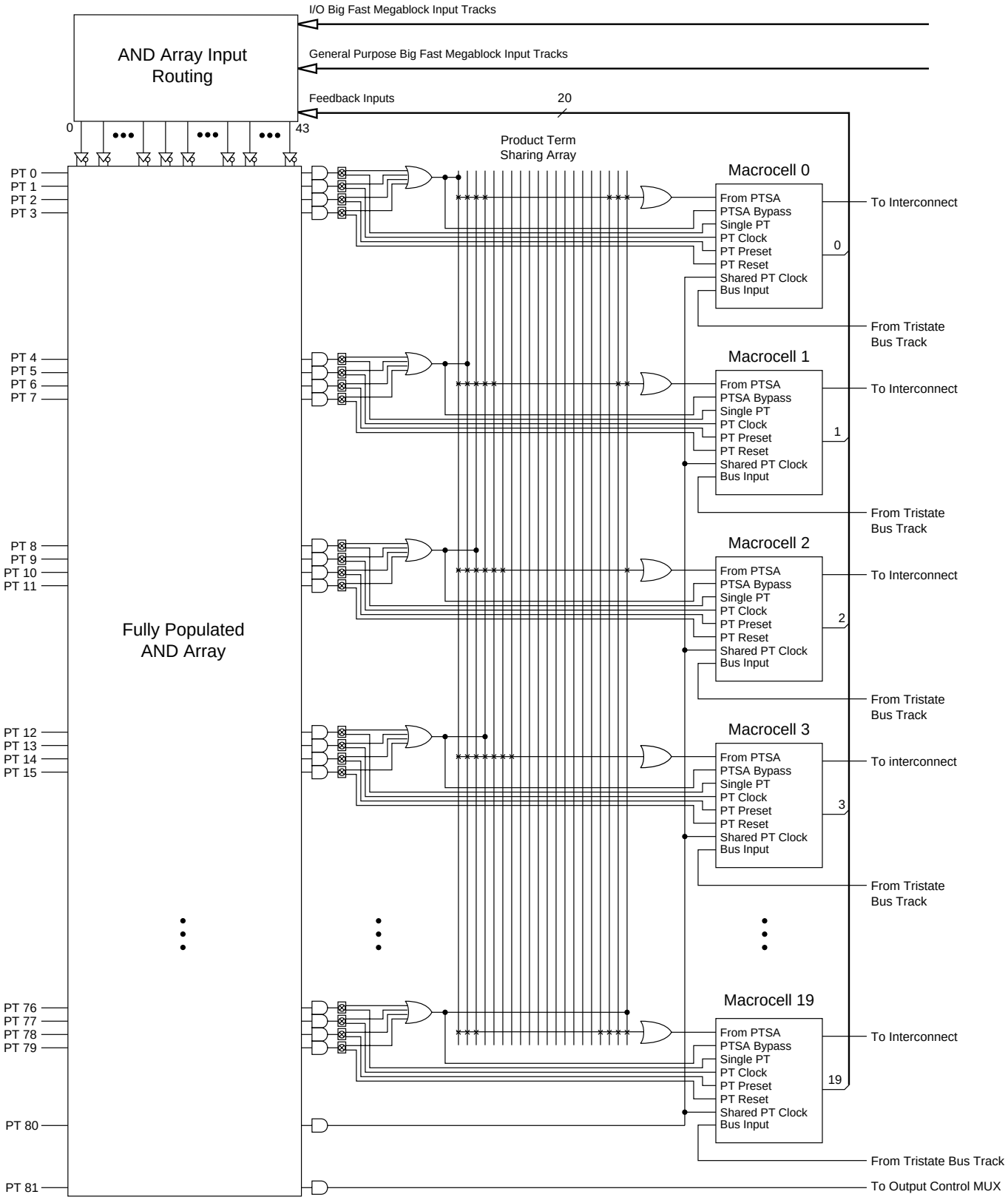
The total registers in the device is the sum of macrocells plus I/O cells, 600 + 264 = 864 registers.

Embedded Tristate Bus

There is a 108-line embedded internal tristate bus as part of the Global Routing Plane (GRP), enabling multiple GLBs to drive the same tracks. This bus can be partitioned into various bus widths such as twelve 9-line buses, six 18-line buses or three 36-line buses. The GLBs can dynamically share a subset of the Global Routing Plane tracks. This feature eliminates the need to convert tristate buses to wide multiplexers on the programmable device. Up to 18 macrocells per GLB can participate in driving the embedded tristate bus. The remaining two macrocells per GLB are used to generate the internal tristate driver control signals on each data byte (with parity). The embedded tristate bus can also be configured as an extension of an external tristate bus using the bidirectional capability of the I/O cells connected to the Global Routing Plane. The Global Routing Plane I/Os 0-8 and 15-23 from each group (I/OGx as defined in the I/O Pin Location Table) can connect to the internal tristate bus as well as the unidirectional/non-tristate global routing channels. I/Os 9-14 connect only to the global routing channel.

The embedded tristate bus has internal bus hold and arbitration features in order to make the function more “user friendly”. The bus hold feature keeps the internal bus at the previously driven logic state when the bus is not driven to eliminate bus float. The bus arbitration is performed on a “first come, first served” priority. In other words, once a logic block drives the bus, other logic blocks cannot drive the bus until the first releases the bus. This arbitration feature prevents internal bus contention when there is an overlap between two bus enable signals. Typically, it takes about 3ns to resolve one bus signal coming off the bus to another bus signal driving the bus. The arbitration feature, combined with the predictability of the CPLD, makes the embedded tristate bus the most practical for real world bus implementation.

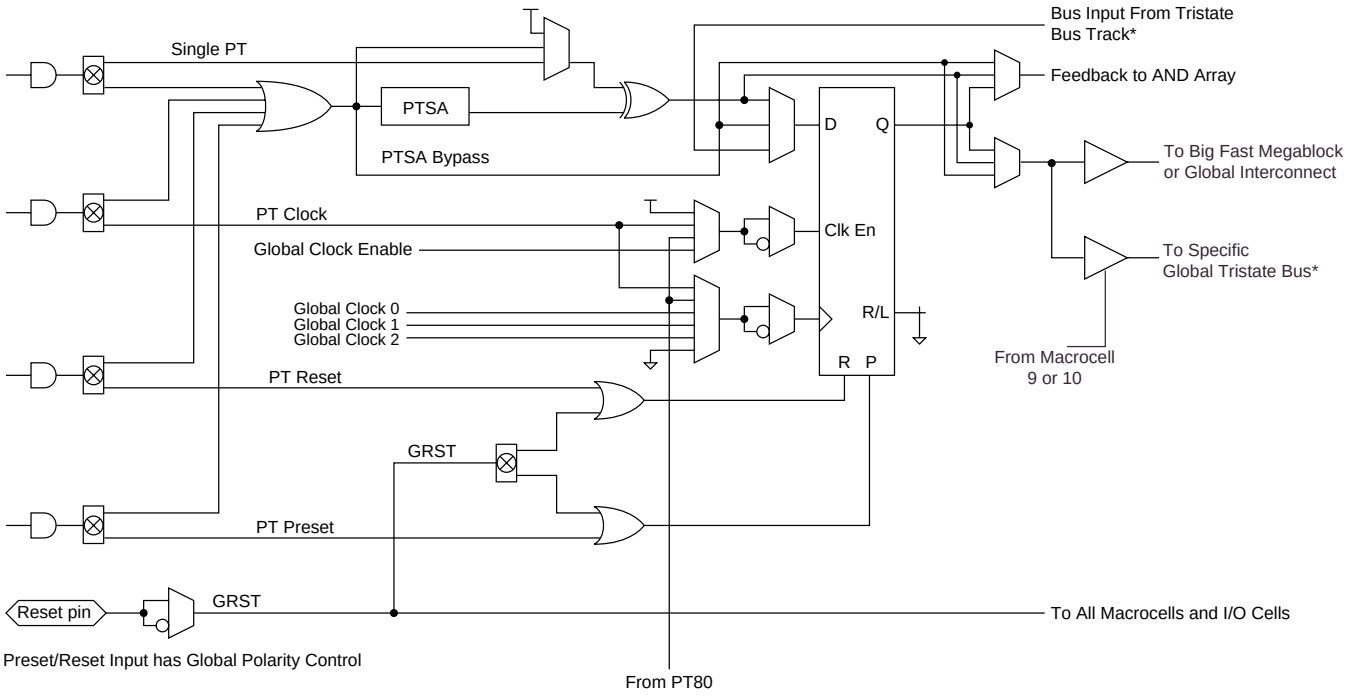
Figure 2. ispLSI 8000V GLB Overview



Note: Macrocells 9 and 10 do not support Tristate Bus Feedback.

⊠ Function Selector (E^2 Cell Controlled)

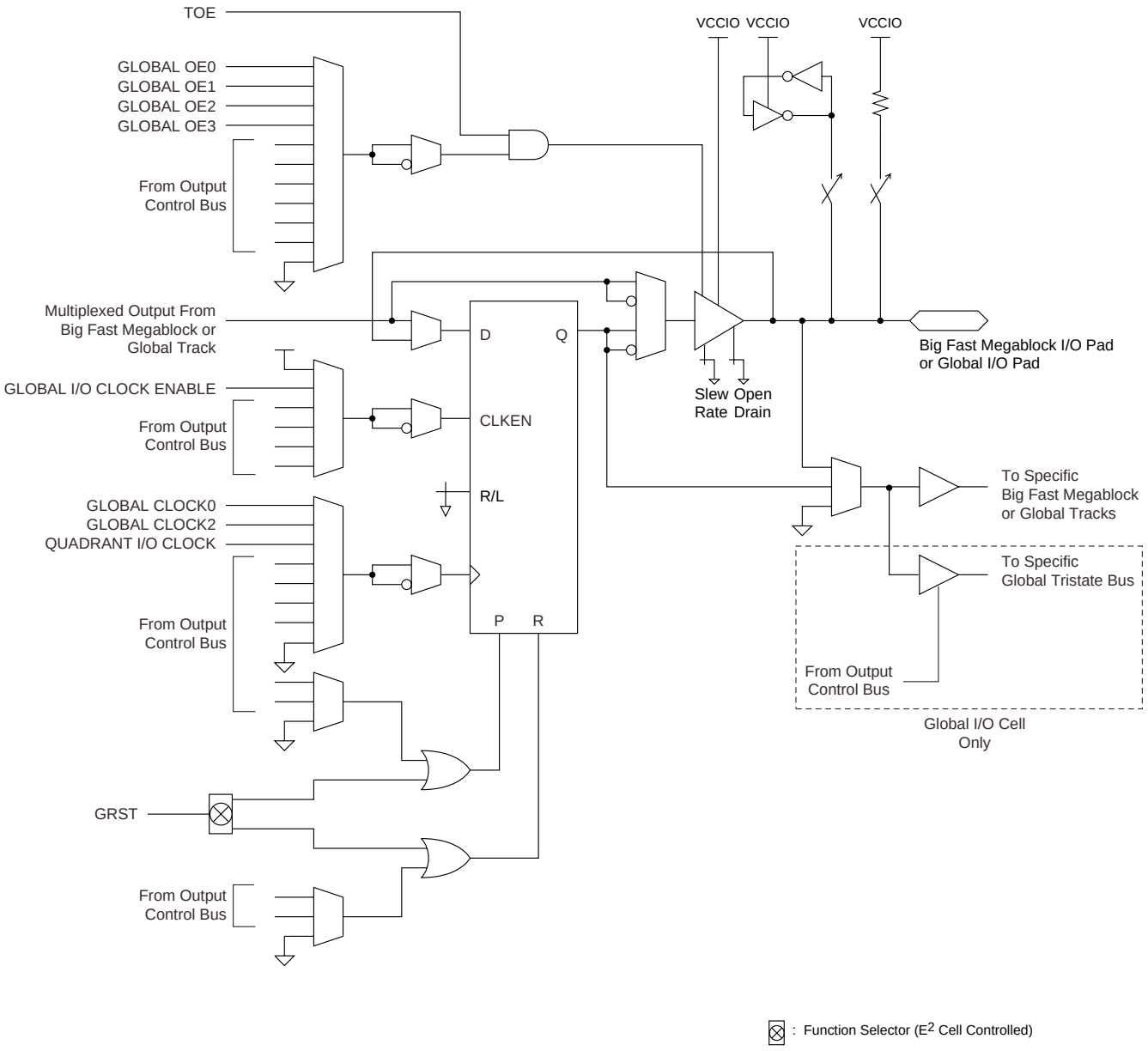
Figure 3. ispLSI 8000V Macrocell Overview



*Not available for Macrocells 9 and 10.

⊗ : Function Selector (E^2 Cell Controlled)

Figure 4. ispLSI 8000V I/O Cell



Output Control Organization

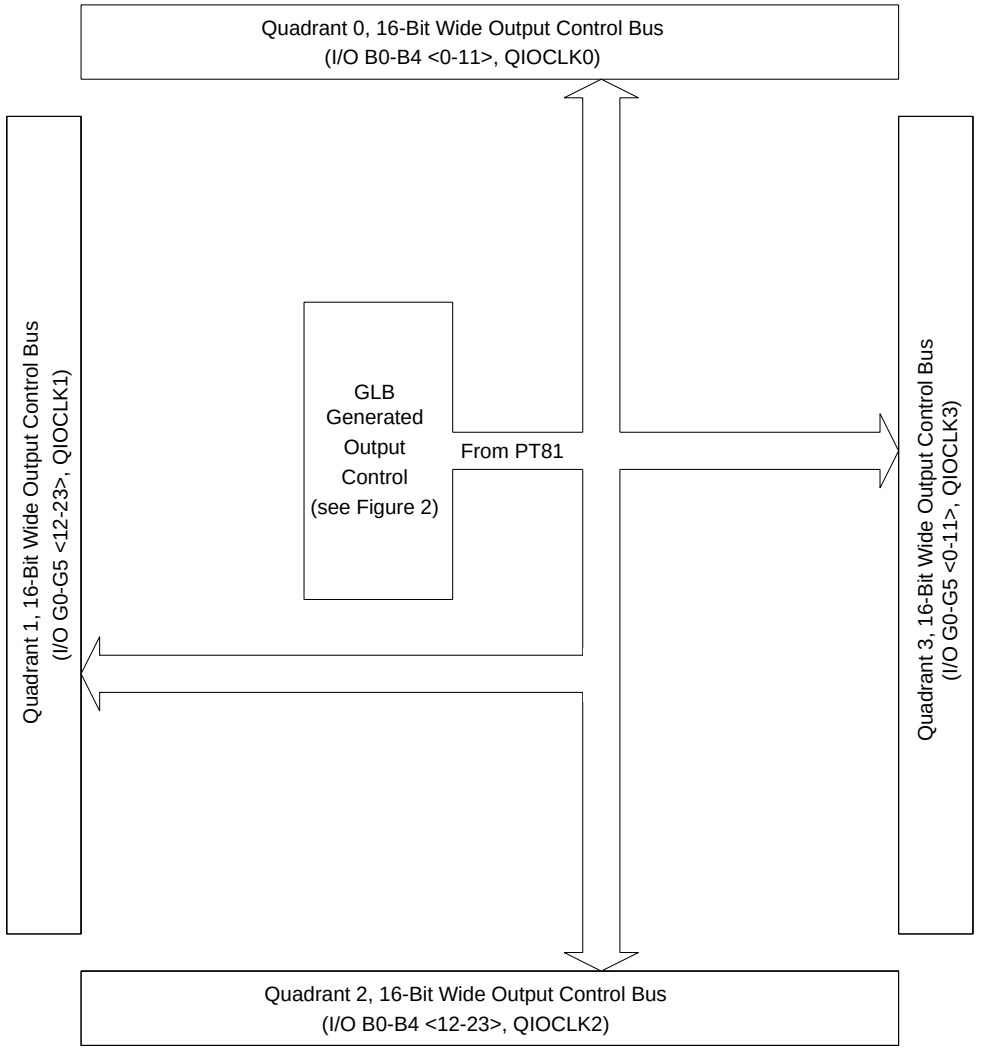
In addition to the data input and output to the I/O cells, each I/O cell can have up to six different I/O cell control signals. In addition to the internal OE control, the five control signals for each I/O cell consist of pin OE control, clock enable, clock input, asynchronous preset and asynchronous reset. All of the I/O control signals can be driven either from the dedicated external input pins or from the internal control bus.

The output enable of each I/O cell can be driven by 21 different sources – 16 from the output control bus, four from the Global OE pins and one from the Test OE pin. The Global OE signals and Test OE signal are driven from the dedicated external control input pins.

The 16-bit wide output control buses are organized in four different quadrants as shown in Figure 5. Since each GLB is capable of generating the output control signals, each of the output control bus signals can be driven from a unique GLB. The 30 GLBs can generate a total of 30 unique I/O control signals. Referring to Figure 2, the GLB generates its output control signal from control product term (PT81).

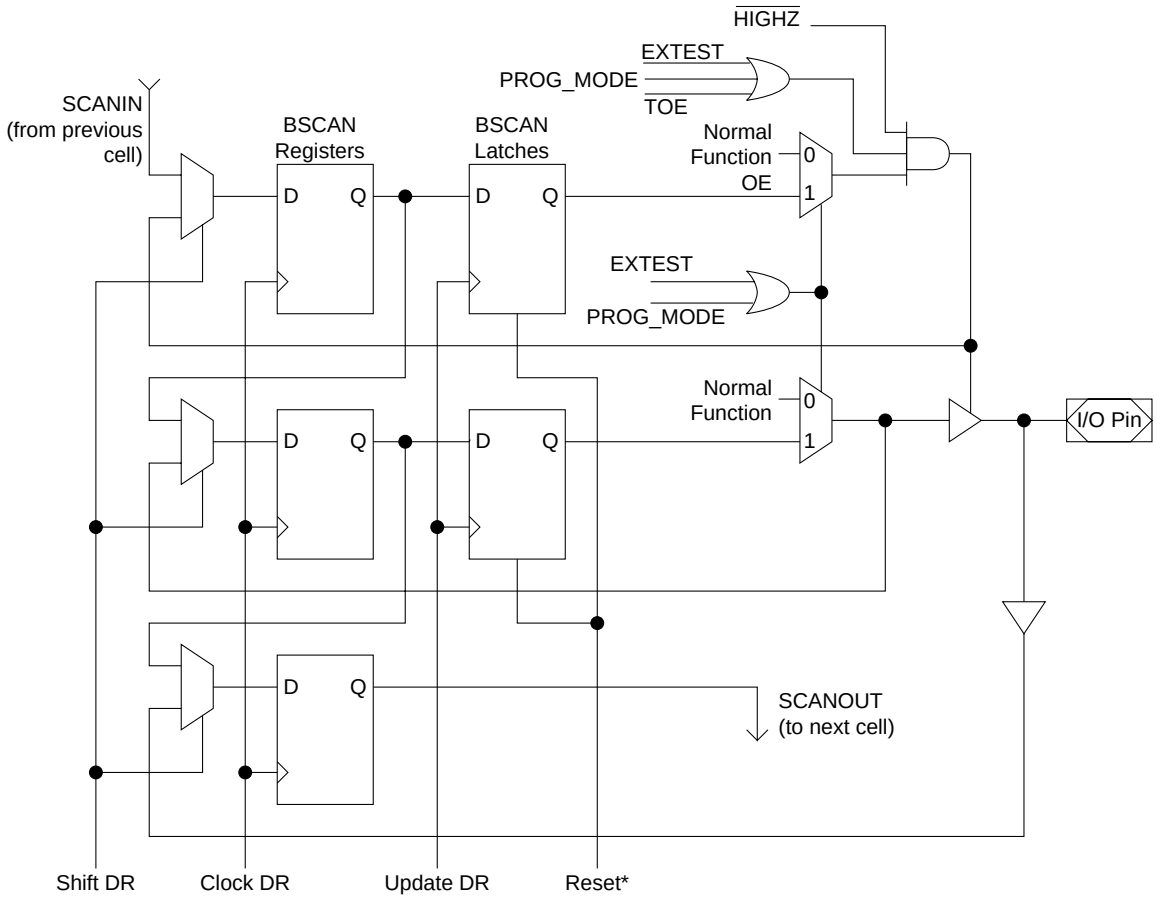
Figure 5 also illustrates how the quadrant clocks are routed to the appropriate quadrant I/O cells.

Figure 5. Output Control Bus and Quadrant Organization



OE Bus/8600V.eps

Figure 6. Boundary Scan Register Circuit for I/O Pins



*Internal power-up reset signal. Not connected to external reset pin.

Figure 7. Boundary Scan Register Circuit for Input-Only Pins

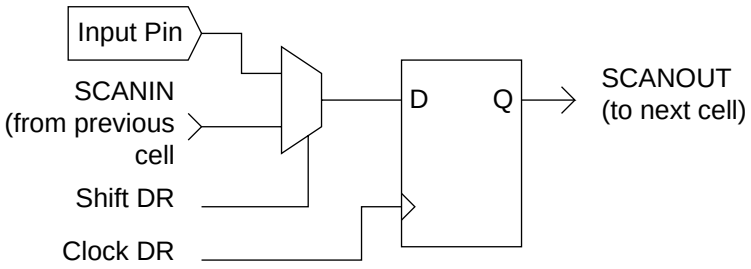
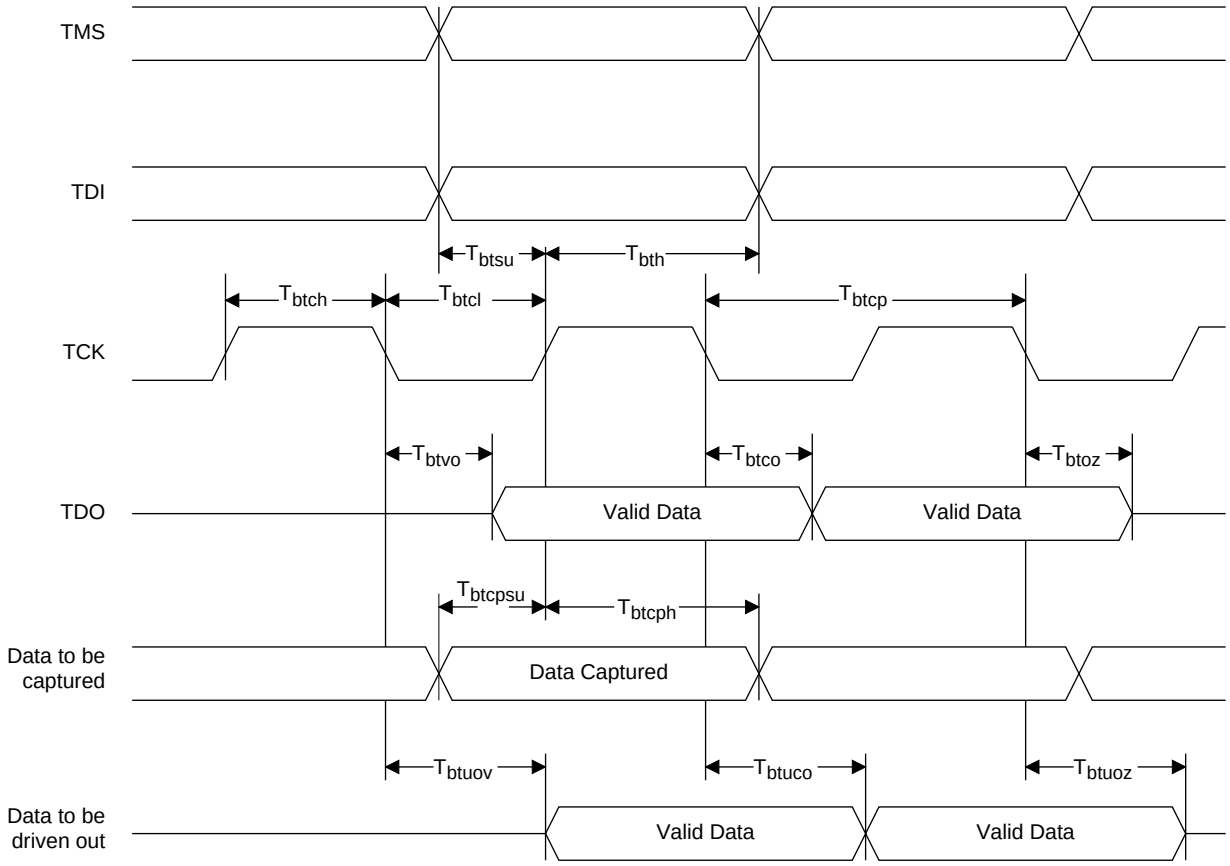


Figure 8. Boundary Scan Waveforms and Timing Specifications



SYMBOL	PARAMETER	MIN	MAX	UNITS
tbtcp	TCK Clock Pulse Width	100	—	ns
tbtch	TCK Pulse Width High	50	—	ns
tbtcl	TCK Pulse Width Low	50	—	ns
tbtsu	TDI, TMS Setup Time to TCK	25	—	ns
tbth	TDI, TMS Hold Time from TCK	25	—	ns
trf	TCK, TDI, TMS Rise and Fall Time	50	—	mV/ns
tbtco	TAP Controller, TCK to TDO Valid	—	25	ns
tbtoz	TAP Controller, TCK to TDO High-Impedance	—	25	ns
tbtvo	TAP Controller, TCK to TDO High-Impedance to Valid Output	—	25	ns
tbtcpsu	BSCAN Test Capture Register Setup Time	25	—	ns
tbtcph	BSCAN Test Capture Register Hold Time	25	—	ns
tbtuco	BSCAN Test Update Register Clock to Valid Output	—	65	ns
tbtuoz	BSCAN Test Update Register Clock to High-Impedance	—	65	ns
tbtuov	BSCAN Test Update Register High-Impedance to Valid Output	—	65	ns

Table 2-0010/8600V

Absolute Maximum Ratings [1,2]

Supply Voltage V_{CC} ..... -0.5 to +5.4V

Input Voltage Applied ..... -0.5 to +5.6V

Tri-Stated Output Voltage Applied ..... -0.5 to +5.6V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

DC Recommended Operating Condition

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial T_A = 0°C to 70°C	3.0	3.6	V
V_{CCIO}	I/O Supply Voltage		2.3	3.6	V

Table 2-0005/8600V

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC} = 3.3V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	10	pf	V_{CC} = 3.3V, V_{CK} = 2.0V
C_3	Global Input Capacitance	10	pf	V_{CC} = 3.3V, V_G = 2.0V

Table 2-0006/8600V

Erase/Reprogram Specification

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/8600V

Switching Test Conditions

Input Pulse Levels	GND to $VCCIO_{min}$
Input Rise and Fall Time	≤ 1.5 ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See Figure 9

Table 2-0003/8600V

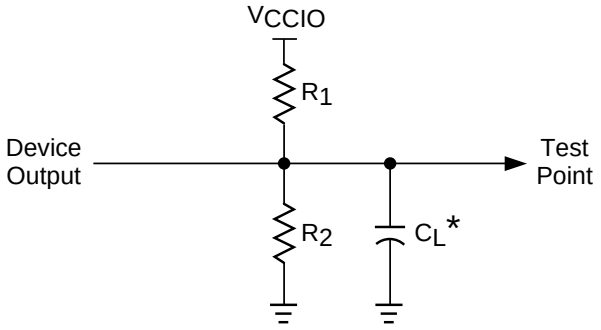
3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (See Figure 9)

		3.3V		2.5V		
TEST CONDITION		**R1**	**R2**	**R1**	**R2**	**CL**
A		316Ω	348Ω	511Ω	475Ω	35pF
B	Active High	∞	348Ω	∞	475Ω	35pF
	Active Low	316Ω	∞	511Ω	∞	35pF
C	Active High to Z at V_{OH}-0.5V	∞	348Ω	∞	475Ω	5pF
	Active Low to Z at V_{OL}+0.5V	316Ω	∞	511Ω	∞	5pF
D	Slow Slew	∞	∞	∞	∞	35pF

Table 2-0004A/8600V

Figure 9. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A/8600V

DC Electrical Characteristics for 3.3V Range

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNITS
V_{CCIO}	I/O Supply Voltage	T_A = 0°C to + 70°C	3.0	3.6	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2.0	5.25	V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	V

Table 2-0007/8600V

DC Electrical Characteristics for 2.5V Range

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNITS
V_{CCIO}	I/O Supply Voltage	T_A = 0°C to + 70°C	2.3	2.7	V
V_{IL}	Input Low Voltage		-0.3	0.7	V
V_{IH}	Input High Voltage		1.7	5.25	V
V_{OL}	Output Low Voltage	$V_{CCIO=min}$, $V_{IN}=V_{IH}$ or V_{IL}, I_{OL}= 100µA	–	0.2	V
		$V_{CCIO=min}$, $V_{IN}=V_{IH}$ or V_{IL}, I_{OL}= 2mA	–	0.7	V
V_{OH}	Output High Voltage	$V_{CCIO=min}$, $V_{IN}=V_{IH}$ or V_{IL}, I_{OH}= -100µA	2.1	–	V
		$V_{CCIO=min}$, $V_{IN}=V_{IH}$ or V_{IL}, I_{OH}= -2mA	1.7	–	V

Table 2-0007B/8600V

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[2]	MAX.	UNITS
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CCIO}-0.2)V \le V_{IN} \le V_{CCIO}$		–	–	10	µA
		$V_{CCIO} \le V_{IN} \le 5.25V$		–	–	50	µA
I_{PU}[4]	I/O Active Pullup Current	$0V \le V_{IN} \le V_{IL}$		–	–	-250	µA
I_{BHL}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL(max)}$		40	–	–	µA
I_{BHH}	Bus Hold High Sustaining Current	$V_{IN} = V_{IH(min)}$		-40	–	–	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{CCIO}$		–	–	550	µA
I_{BHLH}	Bus Hold High Overdrive Current	$0V \le V_{IN} \le V_{CCIO}$		–	–	-550	µA
I_{BHT}	Bus Hold Trip Points			V_{IL}	–	V_{IH}	V
I_{CC}[1,3,5]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V, f_{TOGGLE} = 1 MHz	High Speed Mode	–	330	–	mA
			Low Power Mode	–	160	–	

Table 2-0007C/8600V

1. Measured at a frequency of 1MHz using 30 20-bit counters.
2. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
3. Maximum I_{CC} varies widely with specific device configuration and operating frequency.
4. Pullup is capable of pulling minimum voltage of V_{OH} under no-load conditions.
5. Unused inputs held at GND.

External Switching Characteristics[1]

Over Recommended Operating Conditions

PARA-METER	TEST COND.[4]	#[2]	DESCRIPTION	-125		-90		-60		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Prop Delay, BFM Input to Same BFM Output, 4 PT Bypass	—	8.5	—	10.0	—	15.0	ns
t_{pd2}	A	2	Prop Delay, Global Input to Global Output	—	13.5	—	16.0	—	24.0	ns
f_{max}	—	3	Clk Frequency, Local Feedback, Same GLB [3]	125.0	—	90.0	—	60.0	—	MHz
t_{suq}	—	4	I/O Cell Reg, Data Setup Time, Quadrant I/O Clock	5.0		8.0	—	12.0	—	ns
t_{hq}	—	5	I/O Cell Reg, Data Hold Time, Quadrant I/O Clock	0.0	—	0.0	—	0.0	—	ns
t_{coq}	A	6	I/O Cell Reg, Quadrant Clock to Output Delay	—	4.0	—	6.0	—	9.0	ns
t_{sug}	—	7	I/O Cell Reg, Data Setup Time, Global Clock	3.5	—	6.0	—	9.0	—	ns
t_{hg}	—	8	I/O Cell Reg, Data Hold Time, Global Clock	0.0	—	0.0	—	0.0	—	ns
t_{cog}	A	9	I/O Cell Reg, Global Clock to Output Delay	—	6.0	—	7.5	—	11.0	ns
t_{su1}	—	10	GLB Reg Setup, BFM Input to Same BFM GLB, 4 PT Bypass	4.5	—	7.0	—	10.0	—	ns
t_{h1}	—	11	GLB Reg Hold Time, BFM Input to Same BFM GLB	0.0	—	0.0	—	0.0	—	ns
t_{co1}	A	12	GLB Reg, Global Clock to Same BFM Output Delay	—	8.0	—	10.0	—	15.0	ns
t_{suceq}	—	13	I/O Cell Reg, CLKEN Setup Time, Quadrant I/O Clock	5.5	—	6.5	—	9.5	—	ns
t_{hceq}	—	14	I/O Cell Reg, CLKEN Hold Time, Quadrant I/O Clock	0.0	—	0.0	—	0.0	—	ns
t_{suceg}	—	15	GLB Reg, CLKEN Setup Time, Global Clock	3.5	—	4.5	—	6.5	—	ns
t_{hceg}	—	16	GLB Reg, CLKEN Hold Time, Global Clock	0.0	—	0.0	—	0.0	—	ns
t_{goe}	B/C	17	Global Output Enable/Disable Delay	—	7.0	—	10.0	—	15.0	ns
t_{rglb}	—	18	Global Reset/Preset Time, GLB Reg	—	14.0	—	15.0	—	22.0	ns
t_{rio}	—	19	Global Reset/Preset Time, I/O Cell Reg	—	8.5	—	10.0	—	15.0	ns
t_{rw}	—	20	Global Reset/Preset Pulse Duration	5.0	—	6.5	—	9.5	—	ns
t_{wh}	—	21	Global or Quadrant Clock Pulse, High Duration	4.0	—	6.0	—	9.0	—	ns
t_{wl}	—	22	Global or Quadrant Clock Pulse, Low Duration	4.0	—	6.0	—	9.0	—	ns

Table 2-0030/8600V

1. Unless noted otherwise, all parameters use PTSA and CLK0.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 20-bit counter with local feedback.
4. Refer to Switching Test Conditions section.

Internal Timing Parameters

Over Recommended Operating Conditions

PARA-METER	#[2]	DESCRIPTION	-125		-90		-60		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
I/O Cell Delay									
tidcom	23	Input Pad and Input Buffer, Combinatorial Input	–	0.3	–	0.4	–	0.6	ns
tidreg	24	Input Pad and Input Buffer, Registered Input	–	6.4	–	7.6	–	11.2	ns
tobp	25	Output Register/Latch Bypass to Output Buffer	–	0.0	–	0.0	–	0.0	ns
tibp	26	Input Register/Latch Bypass to BFM Routing or GRP	–	0.4	–	0.5	–	0.8	ns
tiolat	27	I/O Cell Latch, Transparent Mode	–	2.0	–	2.4	–	3.6	ns
tioco	28	I/O Cell Register/Latch, Clk/Gate to Output	–	0.5	–	1.2	–	1.6	ns
tiosu	29	I/O Cell Register/Latch, Setup Time	0.5	–	2.4	–	3.9	–	ns
tioh	30	I/O Cell Register/Latch, Hold Time	2.5	–	3.2	–	4.7	–	ns
tiorst	31	I/O Cell Register/Latch, Reset or Set Time	–	1.5	–	1.7	–	2.5	ns
tiosuce	32	I/O Cell Register/Latch, Setup Time for Clk Enable	0.9	–	1.0	–	1.2	–	ns
tiohce	33	I/O cell Register/Latch, Hold Time for Clk Enable	4.6	–	4.6	–	6.9	–	ns
todreg	34	I/O Cell Output Buffer Delay, Registered Output	–	1.6	–	1.9	–	2.9	ns
todcom	35	I/O Cell Output Buffer Delay, Combinatorial Output	–	1.6	–	1.9	–	2.9	ns
todz	36	Output Driver Disable Time	–	1.4	–	1.7	–	2.6	ns
tslf	37	Slew Rate Adder, Fast Slew Rate	–	0.0	–	0.0	–	0.0	ns
tsls	38	Slew Rate Adder, Slow Slew Rate	–	6.2	–	7.3	–	10.9	ns
GLB / Macrocell Delay									
tandhs	39	AND Array, High Speed Mode	–	2.6	–	2.9	–	4.2	ns
tandlp	40	AND Array, Low Power Mode	–	6.5	–	7.7	–	11.5	ns
t1pt	41	Single Product Term Bypass	–	1.9	–	2.2	–	3.4	ns
t4ptcom	42	Four Product Term Bypass, Combinatorial Macrocell	–	0.5	–	0.6	–	0.9	ns
t4ptreg	43	Four Product Term Bypass, Registered Macrocell	–	1.4	–	1.7	–	2.2	ns
tptsa	44	Product Term Sharing Array	–	2.4	–	2.7	–	4.1	ns
tmbp	45	Macrocell Register/Latch Bypass	–	0.0	–	0.0	–	0.0	ns
tmlat	46	Macrocell Latch, Transparent Mode	–	4.6	–	5.5	–	8.2	ns
tmco	47	Macrocell Register/Latch, Clk/Gate to Output	–	0.2	–	0.8	–	0.9	ns
tmsu	48	Macrocell Register/Latch, Setup Time	2.7	–	4.5	–	6.9	–	ns
tmh	49	Macrocell Register/Latch, Hold Time	1.0	–	1.2	–	1.1	–	ns
tmrst	50	Macrocell Register/Latch, Reset or Set Time	–	2.0	–	1.5	–	1.6	ns
tmsuce	51	Macrocell Register/Latch, Setup Time for Clk Enable	1.0	–	1.3	–	1.7	–	ns
tmhce	52	Macrocell Register/Latch, Hold Time for Clk Enable	2.3	–	2.6	–	3.9	–	ns
tfloc	54	Local Feedback to AND Array	–	0.1	–	0.1	–	0.6	ns
tpck	55	Single Product Term, Clk	1.3	1.3	1.6	1.6	2.5	2.5	ns
tpcken	56	Single Product Term, Clk Enable	–	1.7	–	2.0	–	3.1	ns
tsck	57	Shared Product Term, Clk	1.7	1.9	2.0	2.3	3.1	3.5	ns
tscken	58	Shared Product Term, Clk Enable	1.7	1.9	2.0	2.3	3.1	3.5	ns
tprst	59	Single Product Term, Reset or Set Delay	–	1.5	–	1.7	–	2.6	ns
trdir	60	Macrocell Register, Direct Input from GRP	–	7.2	–	8.4	–	12.7	ns

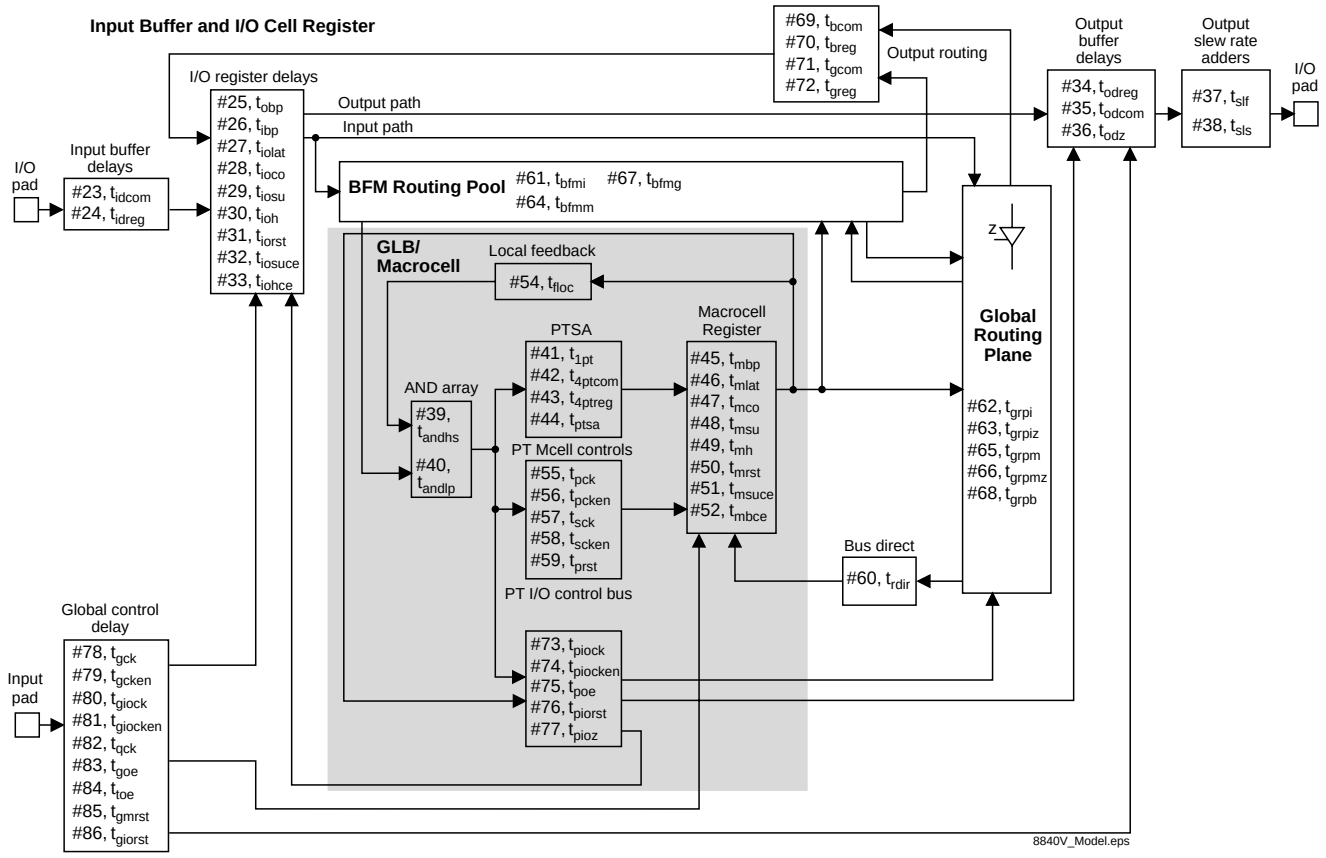
Internal Timing Parameters

Over Recommended Operating Conditions

PARA-METER	#[2]	DESCRIPTION	-125		-90		-60		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
BFM / Global Routing Pool Delay									
t_{bfmi}	61	BFM Routing Delay, Signal from I/O Cell	0.4	1.0	0.6	1.3	0.8	1.9	ns
t_{grpi}	62	GRP Delay, Signal from I/O Cell	–	1.6	–	1.9	–	2.8	ns
t_{grpiz}	63	Internal Tristate Bus Enable/Disable, I/O Cell Buffer	–	4.1	–	4.9	–	7.3	ns
t_{bfmm}	64	BFM Routing Delay, Signal from Macrocell	–	0.6	–	0.7	–	1.1	ns
t_{grpm}	65	GRP Delay, Signal from Macrocell	–	2.0	–	3.0	–	4.5	ns
t_{grpmz}	66	Internal Tristate Bus Enable/Disable, Macrocell Buffer	–	3.0	–	4.3	–	6.5	ns
t_{bfmg}	67	BFM Routing Delay, Signal from GRP	–	2.5	–	3.3	–	4.9	ns
t_{grpb}	68	GRP Delay, Signal from BFM Routing	–	1.3	–	1.5	–	2.3	ns
t_{bcom}	69	BFM Routing to I/O Cell, Combinatorial Path	–	1.5	–	1.7	–	2.6	ns
t_{breg}	70	BFM Routing to I/O Cell, Registered Path	–	2.3	–	2.6	–	4.0	ns
t_{gcom}	71	GRP to I/O Cell, Combinatorial Path	–	0.8	–	0.8	–	1.2	ns
t_{greg}	72	GRP to I/O Cell, Registered Path	–	1.6	–	1.7	–	2.6	ns
I/O Control Bus Delay									
t_{piock}	73	Product Term as I/O Cell Register Clock	–	4.1	–	4.7	–	7.2	ns
$t_{piocken}$	74	Product Term as I/O Cell Register Clock Enable	–	4.6	–	5.3	–	8.1	ns
t_{poe}	75	Product Term as Output Buffer Enable/Disable	–	5.6	–	6.5	–	9.9	ns
t_{piorst}	76	Product Term as I/O Cell Register Reset or Set Delay	–	4.3	–	5.0	–	7.6	ns
t_{pioz}	77	Internal Tristate Bus Control Signal for I/O Cell Buffer	–	3.3	–	3.8	–	5.8	ns
Global Control Delay									
t_{gck}	78	Global Macrocell Register Clk	3.9	4.1	4.3	4.9	6.6	7.5	ns
t_{gcken}	79	Global Macrocell Register Clk Enable	6.4	6.4	7.5	7.5	11.4	11.4	ns
t_{giock}	80	Global I/O Register Clk	3.4	3.9	4.0	4.4	6.1	6.5	ns
$t_{giocken}$	81	Global I/O Register Clk Enable	6.5	6.5	7.5	7.5	11.4	11.4	ns
t_{qck}	82	Quadrant I/O Register Clk	1.9	1.9	2.0	2.9	3.1	4.5	ns
t_{goe}	83	Global Output Enable	–	5.6	–	8.3	–	12.4	ns
t_{toe}	84	Test Output Enable	–	8.5	–	10.1	–	15.2	ns
t_{gmrst}	85	Global GLB Register Reset	–	7.6	–	7.8	–	11.8	ns
t_{giorst}	86	Global I/O Cell Register Reset	–	5.4	–	6.4	–	9.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 8600V Timing Model



Example Timing Calculations

tpd1 = (BFM Input Path Delay) + (GLB Delay) + (Output Path Delay)
= (**t**idcom + **t**ibp + **t**bfmi max) + (**t**andhs + **t**4ptcom + **t**mbp) + (**t**bfmm + **t**bcom + **t**obp + **t**odcom + **t**slf)
= (#23 + #26 + #61) + (#39 + #42 + #45) + (#64 + #69 + #25 + #35 + #37)
= (0.3 + 0.4 + 1.0) + (2.6 + 0.5 + 0.0) + (0.6 + 1.5 + 0.0 + 1.6 + 0.0)
= 8.5 ns

tpd (within BFM)
= (BFM Delay) + (GLB Delay)
= (**t**bfmm) + (**t**andhs + **t**4ptcom + **t**mbp)
= (#64) + (#39 + #42 + #45)
= (0.6) + (2.6 + 0.5 + 0.0)
= 3.7 ns

tpd (between BFMs)
= (GRP Delay) + (BFM Delay) + (GLB Delay)
= (**t**grpm) + (**t**bfmg) + (**t**andhs + **t**4ptcom + **t**mbp)
= (#65) + (#67) + (#39 + #42 + #45)
= (2.0) + (2.5) + (2.6 + 0.5 + 0.0)
= 7.6 ns

BFM I/O to internal tri-state Enable/Disable
= (BFM Input Path Delay) + (GLB Delay, 1PT) + (Tri-state Control Delay)
= (**t**idcom + **t**ibp + **t**bfmi max) + (**t**andhs + **t**1pt + **t**mbp) + (**t**grpmz)
= (#23 + #26 + #61) + (#39 + #41 + #45) + (#66)
= (0.3 + 0.4 + 1.0) + (2.6 + 1.9 + 0.0) + (3.0)
= 9.2 ns

tsu1 = (BFM Input Path Delay) + (GLB Setup Time) - (Min. Global Clock Delay)
= (**t**idcom + **t**ibp + **t**bfmi max) + (**t**andhs + **t**4ptreg + **t**msu) – (**t**gck min)
= (#23 + #26 + #61) + (#39 + #43 + #48) – (#78)
= (0.3 + 0.4 + 1.0) + (2.6 + 1.4 + 2.7) – (3.9)
= 4.5 ns

1/**F**max = (Global Clk to MC Output) + (Local Feedback) + (GLB Setup Time)
= (**t**mco) + (**t**floc) + (**t**andhs + **t**ptsa + **t**msu)
= (#47) + (#54) + (#39 + #44 + #48)
= (0.2) + (0.1) + (2.6 + 2.4 + 2.7)
= 8.0 ns

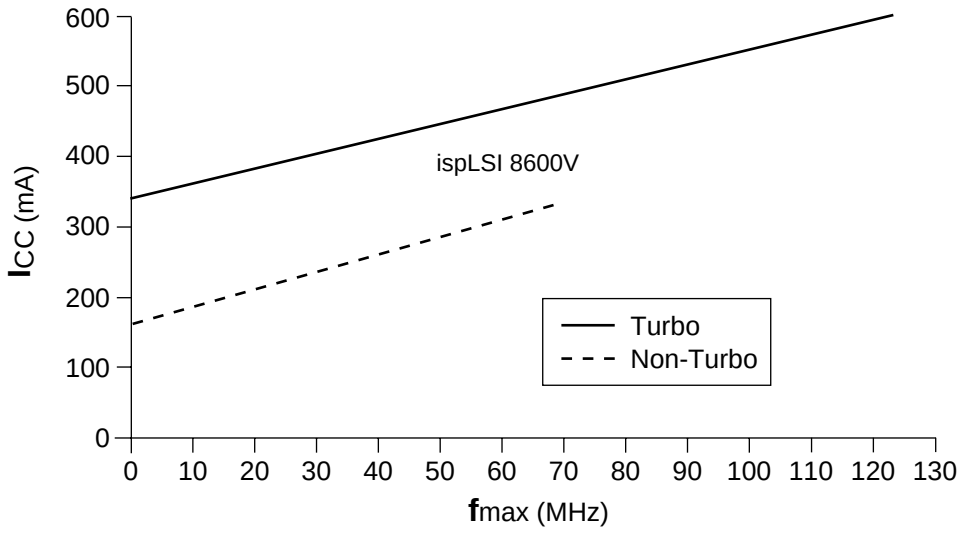
Fmax = 125 MHz

Note: Calculations are based upon timing specifications for the ispLSI 8600V-125L

Power Consumption

Power consumption in the ispLSI 8600V device depends on two primary factors: the speed at which the device is operating and the number of product terms used. The product terms have a fuse-selectable speed/power tradeoff setting. Each group of four product terms has a single speed/power tradeoff control fuse that acts on the complete group of four. The fast “high-speed” setting operates product terms at their normal full power consumption. For portions of the logic that can tolerate longer propagation delays, selecting the slower “low-power” setting will significantly reduce the power dissipation for these product terms. Figure 10 shows the relationship between power and operating speed.

Figure 10. Typical Device Power Consumption vs fmax



Notes: Configuration of 30 20-bit counters
Typical current at 3.3V, 25¡ C

I_{CC} can be estimated for the ispLSI 8600V using the following equation:

I_{CC} = 25.0 + (# of Turbo PTs * 0.25) + (# of Non-Turbo PTs * 0.11) + (# of Macrocells Used * fmax * AF * 0.04)
# of Turbo PTs = Number of Turbo Product Terms Used in Design
# of Non-Turbo PTs = Number of Non-Turbo Product Terms Used in Design
fmax = Maximum Operating Frequency

$$\text{AF (Activity Factor)} = \frac{\text{Average Macrocell Toggle Frequency}}{\text{Fmax}}$$

Note: An Activity Factor of 1.0 means all macrocell registers toggle at fmax. An Activity Factor of 0.5 means the average macrocell register toggles at half of fmax.

The I_{CC} estimate is based on typical conditions (V_{CC} = 3.3V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127/8600V

Signal Descriptions

Signal Name	Description
CLK0, CLK1, CLK2	Dedicated clock input for the GLB registers only. These clock inputs are connected to one of the clock inputs of all GLB registers in the device.
CLKEN	Dedicated clock enable input for the GLB registers only. This input is available as a clock enable for each GLB register in the device. Use of the clock enable input eliminates the need for the user to gate the clock to the register.
GND	Ground (GND)
GOE0, GOE1, GOE2, GOE3	Global Output Enable inputs.
SET/RESET	Dedicated, reset/preset pin connected to ALL registers in the device, GLB registers and I/O registers. Each register can independently choose to be reset or preset when this signal goes active. The active polarity is user selectable.
IOCLKEN	Dedicated clock enable input for the I/O registers only. This input is available as a clock enable input for all I/O registers in the device. Use of the clock enable input eliminates the need for the user to tie the clock to the I/O register.
I/O	Input/Output – These are the general purpose I/O used by the logic array.
EPEN	Embedded Port Enable Pin – When this pin is high, the port is enabled. When this pin is low, the state machine is held at reset asynchronously and TCK, TMS and TDI are ignored.
TMS	Input – This signal is the Test Mode Select input signal.
QIOCLK0, QIOCLK1, QIOCLK2, QIOCLK3	Dedicated clock inputs for the I/O registers only. These clock inputs are connected to the I/O registers on the same side of the device only, they are not connected to all of the I/O registers. Use of these quadrant I/O clocks gives the fastest tco from the device.
TCK	Input – This signal is the Test Clock input signal.
TDI	Input – This signal is the Test Data input signal.
TDO	Output – This signal is the Test Data Out Output Signal.
TOE	Test Output Enable. Tristates all I/O pins when a logic low is driven.
VCC	Vcc
VCCIO	Power supply for the output drivers. The internal logic of the device is connected to VCC which is always 3.3V. The output drivers are connected to VCCIO which can be equal to VCC or 2.5V. This allows the output drivers to be powered from 2.5V, for example, to interface directly with another 2.5V device.
NC[1]	No connect.

1. NC pins are not to be connected to any active signals, VCC or GND.

Signal Locations

Signal Name	272-Ball BGA	492-Ball BGA
QIOCLK0, QIOCKL1, QIOCLK2, QIOCLK3	Y8, M20, C8, N2	AE14, P22, A15, N3
CLK0, CLK1, CLK2	Y9, P18, D8	AC15, R24, B15
CLKEN	V9	AB17
IOCLKEN	B9	E16
EPEN	C17	B26
TCK	A4	A2
TDI	U5	AF1
TDO	C4	B3
TMS	W4	AC4
GOE0, GOE1, GOE2, GOE3	Y10, M19, C9, N1	AF15, P23, D16, N5
TOE	L3	L5
SET/RESET	P3	P2
VCC	D9, D10, D11, D12, J4, J17, K4, K17, L4, L17, M4, M17, U9, U10, U11, U12	E9, E12, E15, E18, F5, F10, F17, F22, G5, G22, K5, K22, L22, M5, N22, P5, R22, T5, U5, U22, Y5, Y22, AA5, AA10, AA17, AA22, AB9, AB12, AB15, AB18
VCCIO	A7, A8, A20, B16, C5, C12, E4, G20, H4, M1, N17, U2, U20, V2, V6, W7, W8, W16, W19, Y13	E8, E13, E19, F7, F20, J6, J21, K3, L24, N1, P24, T3, U25, V6, Y23, AA7, AA20, AB8, AB14, AB19
GND	D4, D16, D17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, U4, U17	E5, E11, E14, E22, F6, F21, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N11, N12, N13, N14, N15, N16, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, AA6, AA21, AB5, AB13, AB16, AB22
NC[1]	A9, V17, W9	A1, A6, A7, A8, A16, A20, A21, A22, , B1, B2, B7, B8, B9, B20, B21, C1, C2, C3, C7, C8, C9, C19, C20, C21, C24, C25, C26, D1, D2, D3, D4, D7, D8, D9, D19, D20, D21, D24,D25, D26, E6, E17, E20, E21, E23, E24, E25, E26, F8, F9, F18, F19, G6, G21, Y6, Y21, AA8, AA9, AA18, AA19, AB1, AB2, AB3, AB4, AB6, AB10, AB20, AB21, AB23, AC1, AC2, AC3, AC6, AC7, AC8, AC18, AC19, AC20, AC23, AC24, AC25, AC26, AD1, AD2, AD3, AD6, AD7, AD8, AD15, AD19, AD20, AD25, AD26, AE1, AE6, AE7, AE8, AE19, AE20, AE21, AE25, AE26, AF6, AF7, AF8, AF19, AF20, AF21, AF25, AF26

1. NC pins are not to be connected to any active signals, VCC or GND.

I/O Pin Locations (272-Ball BGA Package)

Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA
I/O G0 <0>	V4	I/O G2 <15>	P19	I/O G4 <6>	F1	I/O G5 <21>	E17	I/O B3 <12>	B14
I/O G0 <1>	Y3	I/O G2 <16>	P17	I/O G4 <7>	F2	I/O G5 <22>	B18	I/O B3 <13>	D13
I/O G0 <2>	Y2	I/O G2 <17>	P20	I/O G4 <8>	F4	I/O G5 <23>	A18	I/O B3 <14>	B13
I/O G0 <3>	W3	I/O G2 <18>	R20	I/O G4 <9>	E1	I/O B0 <0>	Y4	I/O B3 <15>	A13
I/O G0 <4>	Y1	I/O G2 <19>	R19	I/O G4 <10>	E2	I/O B0 <1>	V5	I/O B3 <16>	A12
I/O G0 <5>	W2	I/O G2 <20>	R18	I/O G4 <11>	E3	I/O B0 <2>	W5	I/O B3 <17>	B12
I/O G0 <6>	W1	I/O G2 <21>	T20	I/O G4 <12>	D20	I/O B0 <3>	Y5	I/O B3 <18>	B11
I/O G0 <7>	V3	I/O G2 <22>	T19	I/O G4 <13>	F17	I/O B0 <4>	U6	I/O B3 <19>	A11
I/O G0 <8>	V1	I/O G2 <23>	T18	I/O G4 <14>	E19	I/O B0 <5>	U7	I/O B3 <20>	C11
I/O G0 <9>	U3	I/O G3 <0>	H2	I/O G4 <15>	G17	I/O B0 <6>	W6	I/O B3 <21>	B10
I/O G0 <10>	R4	I/O G3 <1>	H1	I/O G4 <16>	G18	I/O B0 <7>	V7	I/O B3 <22>	A10
I/O G0 <11>	T4	I/O G3 <2>	J3	I/O G4 <17>	F18	I/O B0 <8>	Y6	I/O B3 <23>	C10
I/O G0 <12>	U19	I/O G3 <3>	J2	I/O G4 <18>	E20	I/O B0 <9>	Y7	I/O B4 <0>	W14
I/O G0 <13>	R17	I/O G3 <4>	J1	I/O G4 <19>	F19	I/O B0 <10>	U8	I/O B4 <1>	V14
I/O G0 <14>	V20	I/O G3 <5>	K3	I/O G4 <20>	H17	I/O B0 <11>	V8	I/O B4 <2>	U14
I/O G0 <15>	V19	I/O G3 <6>	K2	I/O G4 <21>	F20	I/O B0 <12>	B8	I/O B4 <3>	Y15
I/O G0 <16>	U18	I/O G3 <7>	K1	I/O G4 <22>	H18	I/O B0 <13>	C7	I/O B4 <4>	W15
I/O G0 <17>	V18	I/O G3 <8>	L2	I/O G4 <23>	G19	I/O B0 <14>	D7	I/O B4 <5>	V15
I/O G0 <18>	T17	I/O G3 <9>	L1	I/O G5 <0>	A3	I/O B0 <15>	B7	I/O B4 <6>	U15
I/O G0 <19>	W20	I/O G3 <10>	M2	I/O G5 <1>	B2	I/O B0 <16>	B6	I/O B4 <7>	Y16
I/O G0 <20>	Y20	I/O G3 <11>	M3	I/O G5 <2>	B3	I/O B0 <17>	C6	I/O B4 <8>	V16
I/O G0 <21>	Y19	I/O G3 <12>	M18	I/O G5 <3>	A2	I/O B0 <18>	A6	I/O B4 <9>	U16
I/O G0 <22>	W18	I/O G3 <13>	L20	I/O G5 <4>	A1	I/O B0 <19>	D6	I/O B4 <10>	W17
I/O G0 <23>	Y18	I/O G3 <14>	L19	I/O G5 <5>	B1	I/O B0 <20>	B5	I/O B4 <11>	Y17
I/O G2 <0>	U1	I/O G3 <15>	L18	I/O G5 <6>	D3	I/O B0 <21>	A5	I/O B4 <12>	B17
I/O G2 <1>	T3	I/O G3 <16>	K20	I/O G5 <7>	D2	I/O B0 <22>	D5	I/O B4 <13>	A17
I/O G2 <2>	T2	I/O G3 <17>	K19	I/O G5 <8>	C3	I/O B0 <23>	B4	I/O B4 <14>	C16
I/O G2 <3>	T1	I/O G3 <18>	K18	I/O G5 <9>	C2	I/O B3 <0>	V10	I/O B4 <15>	D15
I/O G2 <4>	R3	I/O G3 <19>	J20	I/O G5 <10>	D1	I/O B3 <1>	W10	I/O B4 <16>	C15
I/O G2 <5>	R2	I/O G3 <20>	H20	I/O G5 <11>	C1	I/O B3 <2>	Y11	I/O B4 <17>	A16
I/O G2 <6>	R1	I/O G3 <21>	J19	I/O G5 <12>	D19	I/O B3 <3>	W11	I/O B4 <18>	B15
I/O G2 <7>	P4	I/O G3 <22>	H19	I/O G5 <13>	E18	I/O B3 <4>	V11	I/O B4 <19>	D14
I/O G2 <8>	P2	I/O G3 <23>	J18	I/O G5 <14>	C20	I/O B3 <5>	Y12	I/O B4 <20>	C14
I/O G2 <9>	N4	I/O G4 <0>	G2	I/O G5 <15>	B20	I/O B3 <6>	W12	I/O B4 <21>	A15
I/O G2 <10>	N3	I/O G4 <1>	G1	I/O G5 <16>	A19	I/O B3 <7>	V12	I/O B4 <22>	A14
I/O G2 <11>	P1	I/O G4 <2>	H3	I/O G5 <17>	C19	I/O B3 <8>	W13	I/O B4 <23>	C13
I/O G2 <12>	N18	I/O G4 <3>	G3	I/O G5 <18>	D18	I/O B3 <9>	U13		
I/O G2 <13>	N19	I/O G4 <4>	G4	I/O G5 <19>	B19	I/O B3 <10>	V13		
I/O G2 <14>	N20	I/O G4 <5>	F3	I/O G5 <20>	C18	I/O B3 <11>	Y14		

I/O Pin Locations (492-Ball BGA Package)

Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA
I/O G0 <0>	AA4	I/O G2 <5>	R3	I/O G4 <10>	H4	I/O B0 <15>	D6	I/O B2 <20>	A13
I/O G0 <1>	AA3	I/O G2 <6>	R4	I/O G4 <11>	K6	I/O B0 <16>	A5	I/O B2 <21>	B13
I/O G0 <2>	AA2	I/O G2 <7>	R5	I/O G4 <12>	H26	I/O B0 <17>	B5	I/O B2 <22>	D12
I/O G0 <3>	AA1	I/O G2 <8>	P1	I/O G4 <13>	J23	I/O B0 <18>	C5	I/O B2 <23>	C12
I/O G0 <4>	Y4	I/O G2 <9>	P3	I/O G4 <14>	J24	I/O B0 <19>	D5	I/O B3 <0>	AE15
I/O G0 <5>	Y3	I/O G2 <10>	P4	I/O G4 <15>	J25	I/O B0 <20>	A4	I/O B3 <1>	AF16
I/O G0 <6>	Y2	I/O G2 <11>	N4	I/O G4 <16>	J22	I/O B0 <21>	B4	I/O B3 <2>	AC16
I/O G0 <7>	Y1	I/O G2 <12>	P26	I/O G4 <17>	J26	I/O B0 <22>	C4	I/O B3 <3>	AD16
I/O G0 <8>	W4	I/O G2 <13>	P25	I/O G4 <18>	K23	I/O B0 <23>	A3	I/O B3 <4>	AE16
I/O G0 <9>	W3	I/O G2 <14>	R23	I/O G4 <19>	K24	I/O B1 <0>	AC9	I/O B3 <5>	AF17
I/O G0 <10>	W2	I/O G2 <15>	T22	I/O G4 <20>	K25	I/O B1 <1>	AD9	I/O B3 <6>	AE17
I/O G0 <11>	U6	I/O G2 <16>	R26	I/O G4 <21>	H22	I/O B1 <2>	AE9	I/O B3 <7>	AD17
I/O G0 <12>	U21	I/O G2 <17>	R25	I/O G4 <22>	K26	I/O B1 <3>	AF9	I/O B3 <8>	AC17
I/O G0 <13>	Y26	I/O G2 <18>	T26	I/O G4 <23>	L25	I/O B1 <4>	AC10	I/O B3 <9>	AF18
I/O G0 <14>	Y25	I/O G2 <19>	T23	I/O G5 <0>	E4	I/O B1 <5>	AD10	I/O B3 <10>	AE18
I/O G0 <15>	Y24	I/O G2 <20>	W21	I/O G5 <1>	E3	I/O B1 <6>	AE10	I/O B3 <11>	AD18
I/O G0 <16>	V21	I/O G2 <21>	T24	I/O G5 <2>	E2	I/O B1 <7>	AF10	I/O B3 <12>	B19
I/O G0 <17>	AA26	I/O G2 <22>	T25	I/O G5 <3>	E1	I/O B1 <8>	AE11	I/O B3 <13>	A19
I/O G0 <18>	AA25	I/O G2 <23>	U26	I/O G5 <4>	F4	I/O B1 <9>	AD11	I/O B3 <14>	D18
I/O G0 <19>	AA24	I/O G3 <0>	K2	I/O G5 <5>	F3	I/O B1 <10>	AB11	I/O B3 <15>	C18
I/O G0 <20>	AA23	I/O G3 <1>	K1	I/O G5 <6>	F2	I/O B1 <11>	AC11	I/O B3 <16>	B18
I/O G0 <21>	AB26	I/O G3 <2>	L2	I/O G5 <7>	F1	I/O B1 <12>	A12	I/O B3 <17>	A18
I/O G0 <22>	AB25	I/O G3 <3>	H6	I/O G5 <8>	G4	I/O B1 <13>	E10	I/O B3 <18>	D17
I/O G0 <23>	AB24	I/O G3 <4>	L3	I/O G5 <9>	G3	I/O B1 <14>	B12	I/O B3 <19>	C17
I/O G1 <0>	T2	I/O G3 <5>	L4	I/O G5 <10>	G2	I/O B1 <15>	A11	I/O B3 <20>	B17
I/O G1 <1>	W5	I/O G3 <6>	L1	I/O G5 <11>	G1	I/O B1 <16>	D11	I/O B3 <21>	A17
I/O G1 <2>	U1	I/O G3 <7>	M2	I/O G5 <12>	K21	I/O B1 <17>	C11	I/O B3 <22>	B16
I/O G1 <3>	U2	I/O G3 <8>	M1	I/O G5 <13>	H25	I/O B1 <18>	B11	I/O B3 <23>	C16
I/O G1 <4>	U3	I/O G3 <9>	M3	I/O G5 <14>	H24	I/O B1 <19>	A10	I/O B4 <0>	AD21
I/O G1 <5>	U4	I/O G3 <10>	M4	I/O G5 <15>	H23	I/O B1 <20>	B10	I/O B4 <1>	AC21
I/O G1 <6>	V1	I/O G3 <11>	N2	I/O G5 <16>	G26	I/O B1 <21>	C10	I/O B4 <2>	AF22
I/O G1 <7>	V5	I/O G3 <12>	N23	I/O G5 <17>	G25	I/O B1 <22>	D10	I/O B4 <3>	AE22
I/O G1 <8>	V2	I/O G3 <13>	N24	I/O G5 <18>	G24	I/O B1 <23>	A9	I/O B4 <4>	AD22
I/O G1 <9>	V3	I/O G3 <14>	N26	I/O G5 <19>	G23	I/O B2 <0>	AF11	I/O B4 <5>	AC22
I/O G1 <10>	V4	I/O G3 <15>	N25	I/O G5 <20>	F26	I/O B2 <1>	AE12	I/O B4 <6>	AF23
I/O G1 <11>	W1	I/O G3 <16>	M22	I/O G5 <21>	F25	I/O B2 <2>	AF12	I/O B4 <7>	AE23
I/O G1 <12>	W23	I/O G3 <17>	M23	I/O G5 <22>	F24	I/O B2 <3>	AD12	I/O B4 <8>	AD23
I/O G1 <13>	W24	I/O G3 <18>	M24	I/O G5 <23>	F23	I/O B2 <4>	AC12	I/O B4 <9>	AF24
I/O G1 <14>	W25	I/O G3 <19>	M26	I/O B0 <0>	AE2	I/O B2 <5>	AE13	I/O B4 <10>	AE24
I/O G1 <15>	W26	I/O G3 <20>	H21	I/O B0 <1>	AF2	I/O B2 <6>	AF13	I/O B4 <11>	AD24
I/O G1 <16>	V22	I/O G3 <21>	M25	I/O B0 <2>	AE3	I/O B2 <7>	AD13	I/O B4 <12>	A26
I/O G1 <17>	V23	I/O G3 <22>	L26	I/O B0 <3>	AF3	I/O B2 <8>	AC13	I/O B4 <13>	D23
I/O G1 <18>	V24	I/O G3 <23>	L23	I/O B0 <4>	AD4	I/O B2 <9>	AC14	I/O B4 <14>	B25
I/O G1 <19>	V25	I/O G4 <0>	K4	I/O B0 <5>	AE4	I/O B2 <10>	AD14	I/O B4 <15>	A25
I/O G1 <20>	V26	I/O G4 <1>	H5	I/O B0 <6>	AF4	I/O B2 <11>	AF14	I/O B4 <16>	B24
I/O G1 <21>	W22	I/O G4 <2>	J1	I/O B0 <7>	AC5	I/O B2 <12>	C15	I/O B4 <17>	A24
I/O G1 <22>	U23	I/O G4 <3>	J2	I/O B0 <8>	AD5	I/O B2 <13>	D15	I/O B4 <18>	C23
I/O G1 <23>	U24	I/O G4 <4>	J3	I/O B0 <9>	AE5	I/O B2 <14>	B14	I/O B4 <19>	B23
I/O G2 <0>	T4	I/O G4 <5>	J4	I/O B0 <10>	AB7	I/O B2 <15>	A14	I/O B4 <20>	A23
I/O G2 <1>	T1	I/O G4 <6>	H1	I/O B0 <11>	AF5	I/O B2 <16>	C14	I/O B4 <21>	D22
I/O G2 <2>	W6	I/O G4 <7>	J5	I/O B0 <12>	B6	I/O B2 <17>	D14	I/O B4 <22>	C22
I/O G2 <3>	R2	I/O G4 <8>	H2	I/O B0 <13>	E7	I/O B2 <18>	D13	I/O B4 <23>	B22
I/O G2 <4>	R1	I/O G4 <9>	H3	I/O B0 <14>	C6	I/O B2 <19>	C13		

Signal Configuration

ispLSI 8600V 272-Ball BGA Signal Diagram

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VCCIO	I/O G5 <16>	I/O G5 <23>	I/O B4 <13>	I/O B4 <17>	I/O B4 <21>	I/O B4 <22>	I/O B3 <15>	I/O B3 <16>	I/O B3 <19>	I/O B3 <22>	NC[1]	VCCIO	VCCIO	I/O B0 <18>	I/O B0 <21>	TCK	I/O G5 <0>	I/O G5 <3>	I/O G5 <4>	A
B	I/O G5 <15>	I/O G5 <19>	I/O G5 <22>	I/O B4 <12>	VCCIO	I/O B4 <18>	I/O B3 <12>	I/O B3 <14>	I/O B3 <17>	I/O B3 <18>	I/O B3 <21>	IOCLKEN	I/O B0 <12>	I/O B0 <15>	I/O B0 <16>	I/O B0 <20>	I/O B0 <23>	I/O G5 <2>	I/O G5 <1>	I/O G5 <5>	B
C	I/O G5 <14>	I/O G5 <17>	I/O G5 <20>	EPEN	I/O B4 <14>	I/O B4 <16>	I/O B4 <20>	I/O B4 <23>	VCCIO	I/O B3 <20>	I/O B3 <23>	GOE 2	QIOCLK 2	I/O B0 <13>	I/O B0 <17>	VCCIO	TDO	I/O G5 <8>	I/O G5 <9>	I/O G5 <11>	C
D	I/O G4 <12>	I/O G5 <12>	I/O G5 <18>	GND	GND	I/O B4 <15>	I/O B4 <19>	I/O B3 <13>	VCC	VCC	VCC	VCC	CLK 2	I/O B0 <14>	I/O B0 <19>	I/O B0 <22>	GND	I/O G5 <6>	I/O G5 <7>	I/O G5 <10>	D
E	I/O G4 <18>	I/O G4 <14>	I/O G5 <13>	I/O G5 <21>													VCCIO	I/O G4 <11>	I/O G4 <10>	I/O G4 <9>	E
F	I/O G4 <21>	I/O G4 <19>	I/O G4 <17>	I/O G4 <13>													I/O G4 <8>	I/O G4 <5>	I/O G4 <7>	I/O G4 <6>	F
G	VCCIO	I/O G4 <23>	I/O G4 <16>	I/O G4 <15>													I/O G4 <4>	I/O G4 <3>	I/O G4 <0>	I/O G4 <1>	G
H	I/O G3 <20>	I/O G3 <22>	I/O G4 <22>	I/O G4 <20>													VCCIO	I/O G4 <2>	I/O G3 <0>	I/O G3 <1>	H
J	I/O G3 <19>	I/O G3 <21>	I/O G3 <23>	VCC													VCC	I/O G3 <2>	I/O G3 <3>	I/O G3 <4>	J
K	I/O G3 <16>	I/O G3 <17>	I/O G3 <18>	VCC													VCC	I/O G3 <5>	I/O G3 <6>	I/O G3 <7>	K
L	I/O G3 <13>	I/O G3 <14>	I/O G3 <15>	VCC													VCC	TOE	I/O G3 <8>	I/O G3 <9>	L
M	QIOCLK 1	GOE 1	I/O G3 <12>	VCC													VCC	I/O G3 <11>	I/O G3 <10>	VCCIO	M
N	I/O G2 <14>	I/O G2 <13>	I/O G2 <12>	VCCIO													I/O G2 <9>	I/O G2 <10>	QIOCLK 3	GOE 3	N
P	I/O G2 <17>	I/O G2 <15>	CLK 1	I/O G2 <16>													I/O G2 <7>	SET/ RESET	I/O G2 <8>	I/O G2 <11>	P
R	I/O G2 <18>	I/O G2 <19>	I/O G2 <20>	I/O G0 <13>													I/O G0 <10>	I/O G2 <4>	I/O G2 <5>	I/O G2 <6>	R
T	I/O G2 <21>	I/O G2 <22>	I/O G2 <23>	I/O G0 <18>													I/O G0 <11>	I/O G2 <1>	I/O G2 <2>	I/O G2 <3>	T
U	VCCIO	I/O G0 <12>	I/O G0 <16>	GND	I/O B4 <9>	I/O B4 <6>	I/O B4 <2>	I/O B3 <9>	VCC	VCC	VCC	VCC	I/O B0 <10>	I/O B0 <5>	I/O B0 <4>	TDI	GND	I/O G0 <9>	VCCIO	I/O G2 <0>	U
V	I/O G0 <14>	I/O G0 <15>	I/O G0 <17>	NC[1]	I/O B4 <8>	I/O B4 <5>	I/O B4 <1>	I/O B3 <10>	I/O B3 <7>	I/O B3 <4>	I/O B3 <0>	CLKEN	I/O B0 <11>	I/O B0 <7>	VCCIO	I/O B0 <1>	I/O G0 <0>	I/O G0 <7>	VCCIO	I/O G0 <8>	V
W	I/O G0 <19>	VCCIO	I/O G0 <22>	I/O B4 <10>	VCCIO	I/O B4 <4>	I/O B4 <0>	I/O B3 <8>	I/O B3 <6>	I/O B3 <3>	I/O B3 <1>	NC[1]	VCCIO	VCCIO	I/O B0 <6>	I/O B0 <2>	TMS	I/O G0 <3>	I/O G0 <5>	I/O G0 <6>	W
Y	I/O G0 <20>	I/O G0 <21>	I/O G0 <23>	I/O B4 <11>	I/O B4 <7>	I/O B4 <3>	I/O B3 <11>	VCCIO	I/O B3 <5>	I/O B3 <2>	GOE 0	CLK 0	QIOCLK 0	I/O B0 <9>	I/O B0 <8>	I/O B0 <3>	I/O B0 <0>	I/O G0 <1>	I/O G0 <2>	I/O G0 <4>	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispLSI 8600V

Bottom View

GND	GND	GND	GND
GND	GND	GND	GND
GND	GND	GND	GND
GND	GND	GND	GND

1. NCs are not to be connected to any active signals, Vcc or GND.

Note: Ball A1 indicator dot on top side of package.

Signal Configuration

ispLSI 8600V 492-Ball BGA Signal Diagram

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O B4 <12>	I/O B4 <15>	I/O B4 <17>	I/O B4 <20>	NC[1]	NC[1]	NC[1]	I/O B3 <13>	I/O B3 <17>	I/O B3 <21>	NC[1]	QIOCLK 2	I/O B2 <15>	I/O B2 <20>	I/O B2 <23>	I/O B1 <12>	I/O B1 <15>	I/O B1 <19>	I/O B1 <23>	NC[1]	NC[1]	NC[1]	I/O B0 <16>	I/O B0 <20>	I/O B0 <23>	TCK	NC[1]	A
B	EPEN	I/O B4 <14>	I/O B4 <16>	I/O B4 <19>	I/O B4 <23>	NC[1]	NC[1]	I/O B3 <12>	I/O B3 <16>	I/O B3 <20>	I/O B3 <22>	CLK2	I/O B2 <14>	I/O B2 <21>	I/O B1 <14>	I/O B1 <18>	I/O B1 <20>	NC[1]	NC[1]	NC[1]	I/O B0 <12>	I/O B0 <17>	I/O B0 <21>	TDO	NC[1]	NC[1]	B
C	NC[1]	NC[1]	NC[1]	I/O B4 <18>	I/O B4 <22>	NC[1]	NC[1]	NC[1]	I/O B3 <15>	I/O B3 <19>	I/O B3 <23>	I/O B2 <12>	I/O B2 <16>	I/O B2 <19>	I/O B2 <23>	I/O B1 <17>	I/O B1 <21>	NC[1]	NC[1]	NC[1]	I/O B0 <14>	I/O B0 <18>	I/O B0 <22>	NC[1]	NC[1]	NC[1]	C
D	NC[1]	NC[1]	NC[1]	I/O B4 <13>	I/O B4 <21>	NC[1]	NC[1]	NC[1]	I/O B3 <14>	I/O B3 <18>	GOE 2	I/O B2 <13>	I/O B2 <17>	I/O B2 <18>	I/O B2 <22>	I/O B1 <16>	I/O B1 <22>	NC[1]	NC[1]	NC[1]	I/O B0 <15>	I/O B0 <19>	NC[1]	NC[1]	NC[1]	NC[1]	D
E	NC[1]	NC[1]	NC[1]	NC[1]	GND	NC[1]	NC[1]	VCCIO	VCC	NC[1]	IOCLKEN	VCC	GND	VCCIO	VCC	GND	I/O B1 <13>	VCC	VCCIO	I/O B0 <13>	NC[1]	GND	I/O G5 <0>	I/O G5 <1>	I/O G5 <2>	I/O G5 <3>	E
F	I/O G5 <20>	I/O G5 <21>	I/O G5 <22>	I/O G5 <23>	VCC	GND	VCCIO	NC[1]	NC[1]	VCC							VCC	NC[1]	NC[1]	VCCIO	GND	VCC	I/O G5 <4>	I/O G5 <5>	I/O G5 <6>	I/O G5 <7>	F
G	I/O G5 <16>	I/O G5 <17>	I/O G5 <18>	I/O G5 <19>	VCC	NC[1]															NC[1]	VCC	I/O G5 <8>	I/O G5 <9>	I/O G5 <10>	I/O G5 <11>	G
H	I/O G4 <12>	I/O G5 <13>	I/O G5 <14>	I/O G5 <15>	I/O G4 <21>	I/O G3 <20>															I/O G3 <3>	I/O G4 <1>	I/O G4 <10>	I/O G4 <9>	I/O G4 <8>	I/O G4 <6>	H
J	I/O G4 <17>	I/O G4 <15>	I/O G4 <14>	I/O G4 <13>	I/O G4 <16>	VCCIO															VCCIO	I/O G4 <7>	I/O G4 <5>	I/O G4 <4>	I/O G4 <3>	I/O G4 <2>	J
K	I/O G4 <22>	I/O G4 <20>	I/O G4 <19>	I/O G4 <18>	VCC	I/O G5 <12>															I/O G4 <11>	VCC	I/O G4 <0>	VCCIO	I/O G3 <0>	I/O G3 <1>	K
L	I/O G3 <22>	I/O G4 <23>	VCCIO	I/O G3 <23>	VCC						GND	GND	GND	GND	GND	GND						TOE	I/O G3 <5>	I/O G3 <4>	I/O G3 <2>	I/O G3 <6>	L
M	I/O G3 <19>	I/O G3 <21>	I/O G3 <18>	I/O G3 <17>	I/O G3 <16>						GND	GND	GND	GND	GND	GND						VCC	I/O G3 <10>	I/O G3 <9>	I/O G3 <7>	I/O G3 <8>	M
N	I/O G3 <14>	I/O G3 <15>	I/O G3 <13>	I/O G3 <12>	VCC						GND	GND	GND	GND	GND	GND						GOE 3	I/O G2 <11>	QIOCLK 3	I/O G3 <11>	VCCIO	N
P	I/O G2 <12>	I/O G2 <13>	VCCIO	GOE 1	QIOCLK 1						GND	GND	GND	GND	GND	GND						VCC	I/O G2 <10>	I/O G2 <9>	SET/ RESET	I/O G2 <8>	P
R	I/O G2 <16>	I/O G2 <17>	CLK 1	I/O G2 <14>	VCC						GND	GND	GND	GND	GND	GND						I/O G2 <7>	I/O G2 <6>	I/O G2 <5>	I/O G2 <3>	I/O G2 <4>	R
T	I/O G2 <18>	I/O G2 <22>	I/O G2 <21>	I/O G2 <19>	I/O G2 <15>						GND	GND	GND	GND	GND	GND						VCC	I/O G2 <0>	VCCIO	I/O G1 <0>	I/O G2 <1>	T
U	I/O G2 <23>	VCCIO	I/O G1 <23>	I/O G1 <22>	VCC	I/O G0 <12>															I/O G0 <11>	VCC	I/O G1 <5>	I/O G1 <4>	I/O G1 <3>	I/O G1 <2>	U
V	I/O G1 <20>	I/O G1 <19>	I/O G1 <18>	I/O G1 <17>	I/O G1 <16>	I/O G0 <16>															VCCIO	I/O G1 <7>	I/O G1 <10>	I/O G1 <9>	I/O G1 <8>	I/O G1 <6>	V
W	I/O G1 <15>	I/O G1 <14>	I/O G1 <13>	I/O G1 <12>	I/O G1 <21>	I/O G2 <20>															I/O G2 <2>	I/O G1 <1>	I/O G0 <8>	I/O G0 <9>	I/O G0 <10>	I/O G1 <11>	W
Y	I/O G0 <13>	I/O G0 <14>	I/O G0 <15>	VCCIO	VCC	NC[1]															NC[1]	VCC	I/O G0 <4>	I/O G0 <5>	I/O G0 <6>	I/O G0 <7>	Y
AA	I/O G0 <17>	I/O G0 <18>	I/O G0 <19>	I/O G0 <20>	VCC	GND	VCCIO	NC[1]	NC[1]	VCC							VCC	NC[1]	NC[1]	VCCIO	GND	VCC	I/O G0 <0>	I/O G0 <1>	I/O G0 <2>	I/O G0 <3>	AA
AB	I/O G0 <21>	I/O G0 <22>	I/O G0 <23>	NC[1]	GND	NC[1]	NC[1]	VCCIO	VCC	CLKEN	GND	VCC	VCCIO	GND	VCC	I/O B1 <10>	NC[1]	VCC	VCCIO	I/O B0 <10>	NC[1]	GND	NC[1]	NC[1]	NC[1]	NC[1]	AB
AC	NC[1]	NC[1]	NC[1]	NC[1]	I/O B4 <5>	I/O B4 <1>	NC[1]	NC[1]	NC[1]	I/O B3 <8>	I/O B3 <2>	CLK 0	I/O B2 <9>	I/O B2 <8>	I/O B2 <4>	I/O B1 <11>	I/O B1 <4>	I/O B1 <0>	NC[1]	NC[1]	NC[1]	I/O B0 <7>	TMS	NC[1]	NC[1]	NC[1]	AC
AD	NC[1]	NC[1]	I/O B4 <11>	I/O B4 <8>	I/O B4 <4>	I/O B4 <0>	NC[1]	NC[1]	I/O B3 <11>	I/O B3 <7>	I/O B3 <3>	NC[1]	I/O B2 <10>	I/O B2 <7>	I/O B2 <3>	I/O B1 <9>	I/O B1 <5>	I/O B1 <1>	NC[1]	NC[1]	NC[1]	I/O B0 <8>	I/O B0 <4>	NC[1]	NC[1]	NC[1]	AD
AE	NC[1]	NC[1]	I/O B4 <10>	I/O B4 <7>	I/O B4 <3>	NC[1]	NC[1]	NC[1]	I/O B3 <10>	I/O B3 <6>	I/O B3 <4>	I/O B3 <0>	QIOCLK 0	I/O B2 <5>	I/O B2 <1>	I/O B1 <8>	I/O B1 <6>	I/O B1 <2>	NC[1]	NC[1]	NC[1]	I/O B0 <9>	I/O B0 <5>	I/O B0 <2>	I/O B0 <0>	NC[1]	AE
AF	NC[1]	NC[1]	I/O B4 <9>	I/O B4 <6>	I/O B4 <2>	NC[1]	NC[1]	NC[1]	I/O B3 <9>	I/O B3 <5>	I/O B3 <1>	GOE 0	I/O B2 <11>	I/O B2 <6>	I/O B2 <2>	I/O B2 <0>	I/O B1 <7>	I/O B1 <3>	NC[1]	NC[1]	NC[1]	I/O B0 <11>	I/O B0 <6>	I/O B0 <3>	I/O B0 <1>	TDI	AF
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

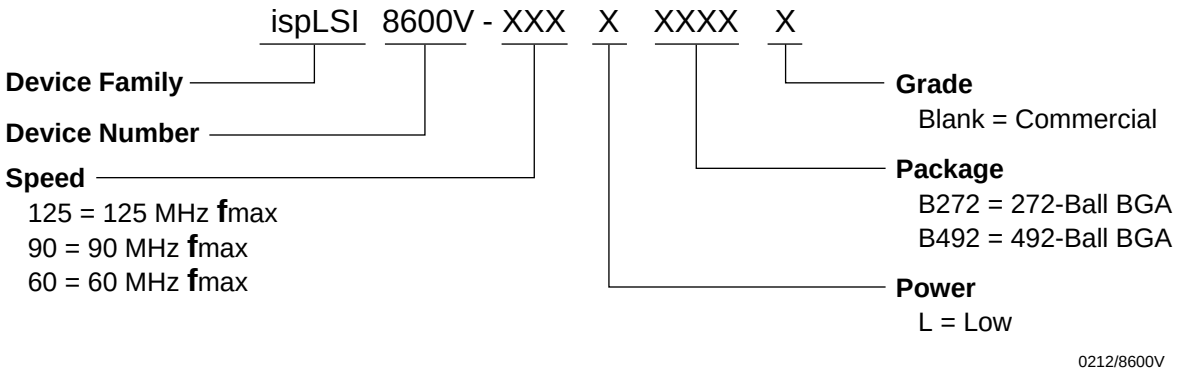
ispLSI 8600V

Bottom View

1. NC pins are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



0212/8600V

Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	125	8.5	ispLSI 8600V-125LB272	272-Ball BGA
	125	8.5	ispLSI 8600V-125LB492	492-Ball BGA
	90	10	ispLSI 8600V-90LB272	272-Ball BGA
	90	10	ispLSI 8600V-90LB492	492-Ball BGA
	60	15	ispLSI 8600V-60LB272	272-Ball BGA
	60	15	ispLSI 8600V-60LB492	492-Ball BGA

Table 2-0041/8600V