TSA1002

10-BIT, 50MSPS, 50mW A/D CONVERTER

NOT FOR NEW DESIGN

- 10-bit A/D converter in deep submicron CMOS technology
- Single supply voltage: 2.5V
- Input range: 2Vpp differential
- 50Msps sampling frequency
- Ultra low power consumption: 50mW @ 50Msps
- ENOB=9.6 @ 40Msps, Fin=24MHz
- SFDR typically up to 72dB @ 50Msps, Fin=5MHz
- Built-in reference voltage with external bias capability
- Pinout compatibility with TSA0801, TSA1001 and TSA1201

DESCRIPTION

The TSA1002 is a 10-bit, 50Msps sampling frequency Analog to Digital converter using a CMOS technology combining high performances and very low power consumption.

The TSA1002 is based on a pipeline structure and digital error correction to provide excellent static linearity and guarantee 9.6 effective bits at Fs=40Msps, and Fin=24MHz.

A voltage reference is integrated in the circuit to simplify the design and minimize external components. It is nevertheless possible to use the circuit with an external reference.

Especially designed for high speed, low power applications, the TSA1002 only dissipates 50mW at 50Msps. A tri-state capability, available on the output buffers, enables to address several slave ADCs by a unique master.

The output data can be coded into two different formats. A Data Ready signal is raised as the data is valid on the output and can be used for synchronization purposes.

The TSA1002 is available in commercial (0 to +70 C) and extended (-40 to +85 C) temperature range, in a small 48 pins TQFP package.

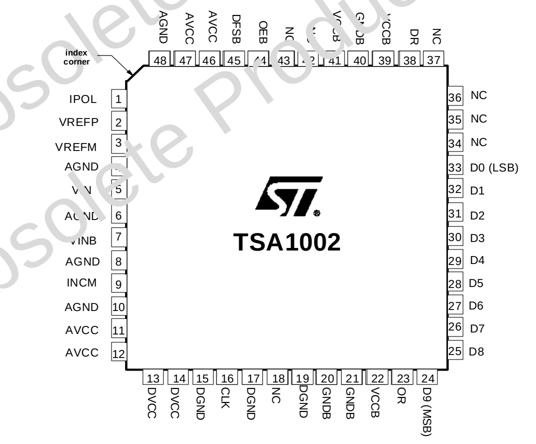
APPLICATIONS

- Medical imaging and ultrasound
- Portable instrumentation
- Cable Modem Receivers
- High resolution fax and scanners
- High speed DSP interface

ORDER CODE

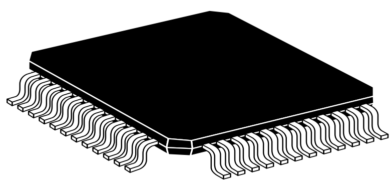
Part Number	Temperature Range	Package	Conditioning	Marking
TSA1002CF	0 C to +70 C	TQFP48	Tray	SA1002C
TSA1002CFT	0 C to +70 C	TQFP48	Tape & Reel	SA1002C
TSA1002IF	-40 C to +85 C	TQFP48	Tray	SA1002I
TSA1002IFT	-40 C to +85 C	TQFP48	Tape & Reel	SA1002I
EVAL1002/AA	Evaluation board			

PIN CONNECTIONS (top view)



PACKAGE

7 x 7 mm TQFP48



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
AVCC	Analog Supply voltage 1)	0 to 3.3	V
DVCC	Digital Supply voltage 1)	0 to 3.3	V
VCCB	Digital buffer Supply voltage 1)	0 to 3.3	V
IDout	Digital output current	-100 to 100	mA
Tstg	Storage temperature	+150	C
ESD	Electrical Static Discharge - HBM - CDM-JEDEC Standard	 2 1.5	 KV KV
Latch-up	Class2)	A	

1) All voltages values, except differential voltage, are with respect to network ground terminal. The magnitude of input and output voltages must never exceed -0.3V or VCC+0V

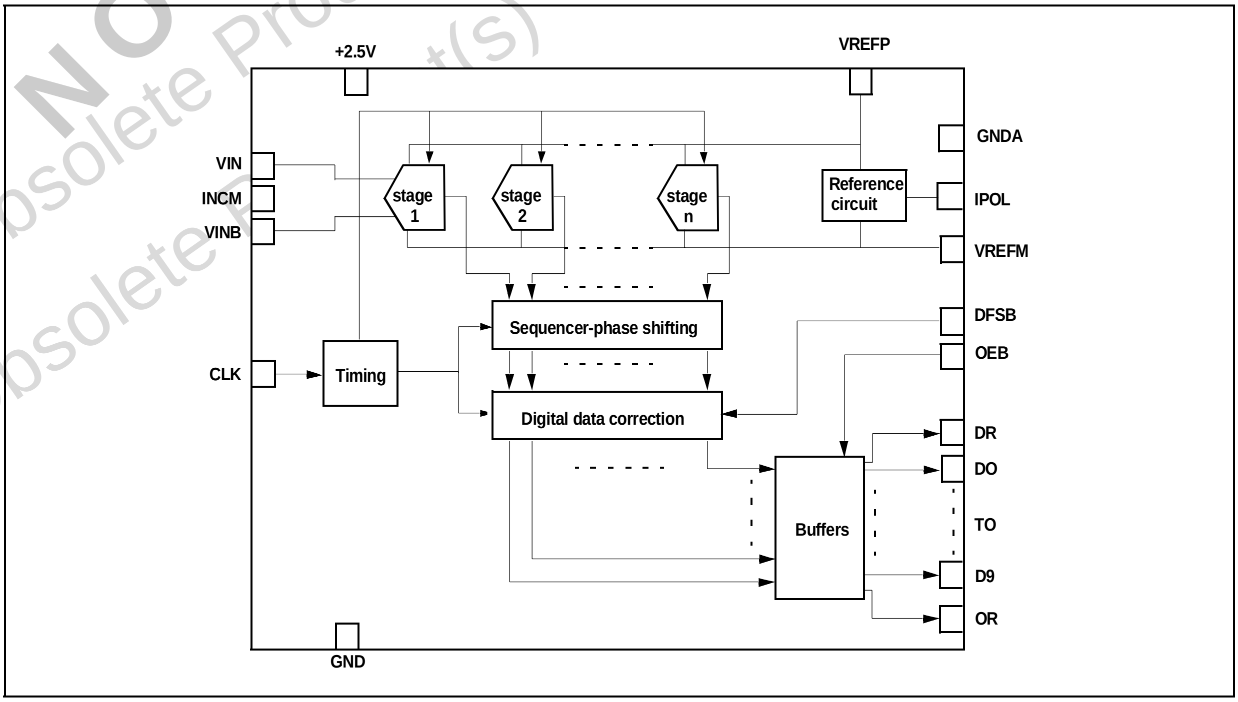
2) Corporate ST Microelectronics procedure number 0018695

OPERATING CONDITIONS

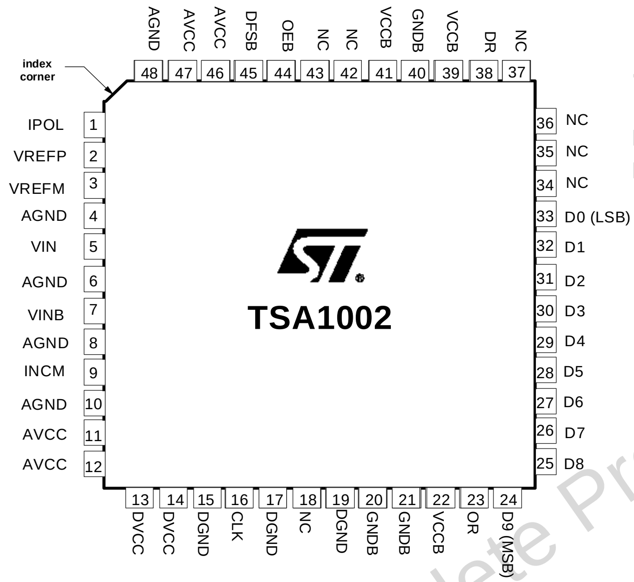
Symbol	Parameter	Min	Typ	Max	Unit
AVCC	Analog Supply voltage	2.25	2.5	2.7	V
DVCC	Digital Supply voltage	2.25	2.5	2.7	V
VCCB	Digital buffer Supply voltage	2.25	2.5	2.7	V
VREFP	Forced top reference voltage 1)	0.5	1	1.8	V
VREFM	Forced bottom reference voltage1)	0	0	0.5	V
INCM	Forced input common mode voltage	0.2	0.5	1.1	V

1)Condition VRefP-VRefM>0.3V

BLOCK DIAGRAM



PIN CONNECTIONS (top view)



PIN DESCRIPTION

Pin No	Name	Description	Observation	Pin No	Name	Description	Observation
1	IPOL	Analog bias current input		25	D8	Digital output	CMOS output (2.5V)
2	VREFP	Top voltage reference	1V	26	D7	Digital output	CMOS output (2.5V)
3	VREFM	Bottom voltage reference	0V	27	D6	Digital output	CMOS output (2.5V)
4	AGND	Analog ground	0V	28	D5	Digital output	CMOS output (2.5V)
5	VIN	Analog input	1Vpp	29	D4	Digital output	CMOS output (2.5V)
6	AGND	Analog ground	0V	30	D3	Digital output	CMOS output (2.5V)
7	VINB	Inverted analog input	1Vpp	31	D2	Digital output	CMOS output (2.5V)
8	AGND	Analog ground	0V	32	D1	Digital output	CMOS output (2.5V)
9	INCM	Input common mode	0.5V	33	D0(LSB)	Least Significant Bit output	CMOS output (2.5V)
10	AGND	Analog ground	0V	34	NC	Non connected	
11	AVCC	Analog power supply	2.5V	35	NC	Non connected	
12	AVCC	Analog power supply	2.5V	36	NC	Non connected	
13	DVCC	Digital power supply	2.5V	37	NC	Non connected	
14	DVCC	Digital power supply	2.5V	38	DR	Data Ready output	CMOS output (2.5V)
15	DGND	Digital ground	0V	39	VCCB	Digital Buffer power supply	2.5V
16	CLK	Clock input	2.5V compatible CMOS input	40	GNDB	Digital Buffer ground	0V
17	DGND	Digital ground	0V	41	VCCB	Digital Buffer power supply	2.5V
18	NC	Non connected		42	NC	Non connected	
19	DGND	Digital ground	0V	43	NC	Non connected	
20	GNDB	Digital buffer ground	0V	44	OEB	Output Enable input	2.5V compatible CMOS input
21	GNDB	Digital buffer ground	0V	45	DFSB	Data Format Select input	2.5V compatible CMOS input
22	VCCB	Digital buffer power supply	2.5V	46	AVCC	Analog power supply	2.5V
23	OR	Out Of Range output	CMOS output (2.5V)	47	AVCC	Analog power supply	2.5V
24	D9(MSB)	Most Significant Bit output	CMOS output (2.5V)	48	AGND	Analog ground	0V

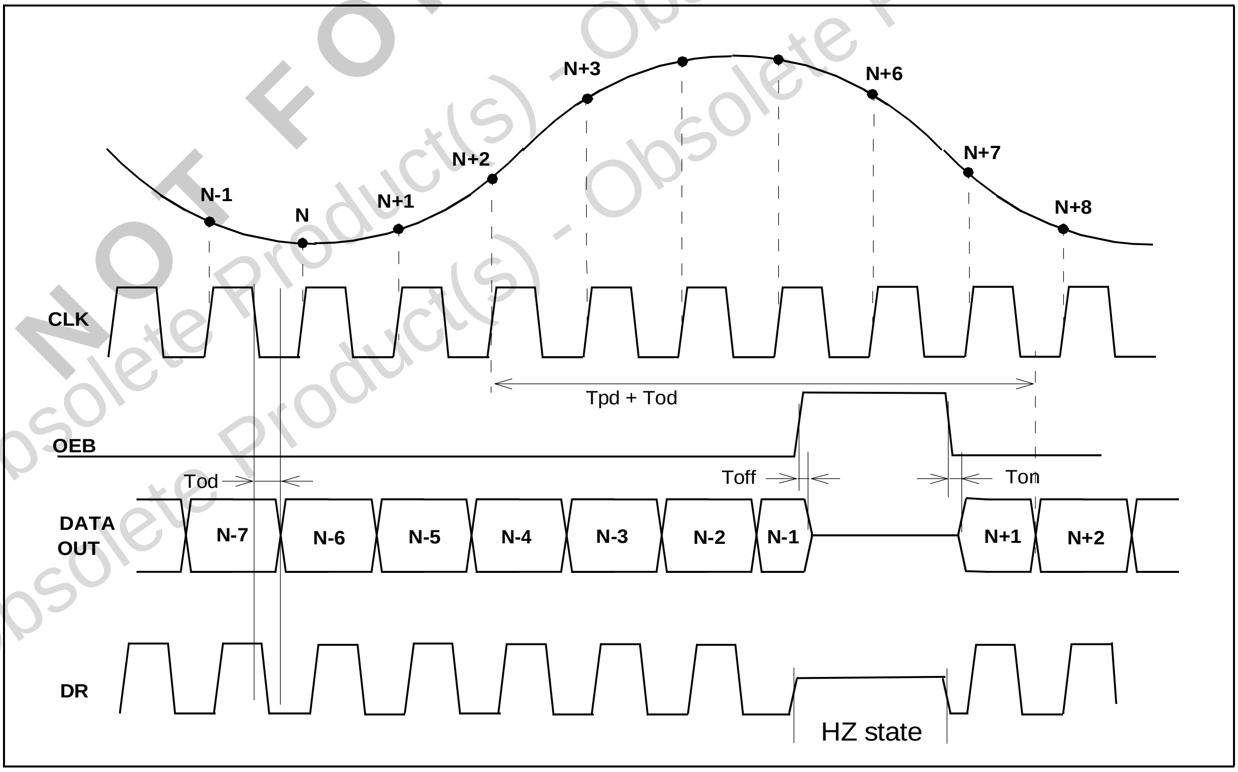
ELECTRICAL CHARACTERISTICS

AVCC = DVCC = VCCB = 2.5V, Fs= 40Msps,Fin= 1MHz, Vin@ -1.0dBFS, VREFM= 0V
Tamb = 25 C (unless otherwise specified)

TIMING CHARACTERISTICS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
FS	Sampling Frequency		0.5		50	Msps
DC	Clock Duty Cycle		40	50	60	%
TC1	Clock pulse width (high)		9	10		ns
TC2	Clock pulse width (low)		9	10		ns
Tod	Data Output Delay (Fall of Clock to Data Valid)	10pF load capacitance		5		ns
Tpd	Data Pipeline delay			5.5		cycles
Ton	Falling edge of OEB to digital output valid data			1		ns
Toff	Rising edge of OEB to digital output tri-state			1		ns

TIMING DIAGRAM



CONDITIONS

AVCC = DVCC = VCCB = 2.5V, Fs= 40Msps,Fin= 1MHz, Vin@ -1.0dBFS, VREFM= 0V
Tamb = 25 C (unless otherwise specified)

ANALOG INPUTS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
VIN-VINB	Full scale reference voltage			2.0		Vpp
Req	Equivalent input resistance			13		kΩ
Cin	Input capacitance			5.0		pF
BW	Analog Input Bandwidth	Vin@ Full scale, FS=50Msps		1000		MHz
ERB	Effective Resolution Bandwidth [1)]			60		MHz

1) See parameters definition for more information

REFERENCE VOLTAGE

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
VREFP	Top internal reference voltage		0.91	1.03	1.14	V
		Tmin= -40 C to Tmax= 85 C[1)]	0.88		1.16	V
Vpol	Analog bias voltage		1.20	1.27	1.35	V
		Tmin= -40 C to Tmax= 85 C[1)]	1.18		1.36	V
Ipol	Analog bias current	Normal operating mode	50	70	100	µA
Ipol	Analog bias current	Shutdown mode		0		µA
VINCM	Input common mode voltage		0.47	0.57	0.68	V
		Tmin= -40 C to Tmax= 85 C[1)]	0.46		0.66	V

1) Not fully tested over the temperature range. Guaranteed by sampling.

CONDITIONS

AVCC = DVCC = VCCB = 2.5V, Fs= 40Msps,Fin= 1MHz, Vin@ -1.0dBFS, VREFP=1V, VREFM= 0V
Tamb = 25 C (unless otherwise specified)

POWER CONSUMPTION

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ICCA	Analog Supply current	1)		15.6	18	mA
		Tmin= -40 C to Tmax= 85 C 2)			21	mA
ICCD	Digital Supply Current	1)		1.3	2	mA
		Tmin= -40 C to Tmax= 85 C 2)			2	mA
ICCB	Digital Buffer Supply Current	1)		2.5	5	mA
		Tmin= -40 C to Tmax= 85 C 2)			5	mA
ICCBZ	Digital Buffer Supply Current in High Impedance Mode	1)		40	100	µA
Pd	Power consumption in normal operation mode	1)		48	60	mW
		Tmin= -40 C to Tmax= 85 C 2)			62	mW
PdZ	Power consumption in High Impedance mode	1)		43	48	mW
Rthja	Junction-ambient thermal resistor (TQFP48)			80		C/W

1) Rpol= 18KΩ. Equivalent load: Rload= 470Ω and Cload= 6pF
2) Not fully tested over the temperature range. Guaranteed by sampling.

DIGITAL INPUTS AND OUTPUTS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Digital inputs						
VIL	Logic "0" voltage				0.8	V
VIH	Logic "1" voltage		2.0			V
Digital Outputs						
VOL	Logic "0" voltage	Iol=10µA			0.4	V
VOH	Logic "1" voltage	Ioh=-10µA	2.4			V
IOZ	High Impedance leakage current	OEB set to VIH	-1.5		1.5	µA
C_L	Output Load Capacitance				15	pF

ACCURACY

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
OE	Offset Error	Fin= 2MHz, VIN@+1dBFS	-40	-2	40	mV
DNL	Differential Non Linearity	Fin= 2MHz, VIN@+1dBFS	-0.7	±0.2	+0.7	LSB
INL	Integral Non Linearity	Fin= 2MHz, VIN@+1dBFS	-0.8	±0.3	+0.8	LSB
-	Monotonicity and no missing codes		Guaranteed			

CONDITIONS

AVCC = DVCC = 2.5V, Fs= 40Msps Vin@ -1.0dBFS, VREFP=1V, VREFM= 0V
Tamb = 25 C (unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SFDR	Spurious Free Dynamic Range	Fin= 5MHz Fin= 10MHz 1) Fin= 24MHz		-79.2 -77 -69	-65.5 -68.5 -63.4	dBc
		Fin= 5MHz Fin= 10MHz 2) Fin= 24MHz			-61.5 -62.8 -58.5	dBc
SNR	Signal to Noise Ratio	Fin= 5MHz Fin= 10MHz 1) Fin= 24MHz	58.5 58.3 57.4	59.5 59.4 59.0		dB
		Fin= 5MHz Fin= 10MHz 2) Fin= 24MHz	57.9 57.1 55.9			dB
THD	Total Harmonic Distortion	Fin= 5MHz Fin= 10MHz 1) Fin= 24MHz		-77.8 -76 -68.1	-63.5 -67.4 -62.5	dB
		Fin= 5MHz Fin= 10MHz 2) Fin= 24MHz			-62.3 -60.7 -57.6	dB
SINAD	Signal to Noise and Distortion Ratio	Fin= 5MHz Fin= 10MHz 1) Fin= 24MHz	58.5 58.2 57.0	59.4 59.3 58.5		dB
		Fin= 5MHz Fin= 10MHz 2) Fin= 24MHz	57.8 56.9 55.3			dB
ENOB	Effective Number of Bits	Fin= 5MHz Fin= 10MHz 1) Fin= 24MHz	9.6 9.5 9.3	9.76 9.71 9.60		bits
		Fin= 5MHz Fin= 10MHz 2) Fin= 24MHz	9.4 9.3 9			bits

1) Rpol= 18KΩ. Equivalent load: Rload= 470Ω and Cload= 6pF
2) Tmin= -40 C to Tmax= 85 C. Not fully tested over the temperature range. Guaranteed by sampling.

DEFINITIONS OF SPECIFIED PARAMETERS

STATIC PARAMETERS

Static measurements are performed through method of histograms on a 2MHz input signal, sampled at 40Msps, which is high enough to fully characterize the test frequency response. The input level is +1dBFS to saturate the signal.

Differential Non Linearity (DNL)

The average deviation of any output code width from the ideal code width of 1 LSB.

Integral Non linearity (INL)

An ideal converter presents a transfer function as being the straight line from the starting code to the ending code. The INL is the deviation for each transition from this ideal curve.

DYNAMIC PARAMETERS

Dynamic measurements are performed by spectral analysis, applied to an input sine wave of various frequencies and sampled at 40Msps.

The input level is -1dBFS to measure the linear behavior of the converter. All the parameters are given without correction for the full scale amplitude performance except the calculated ENOB parameter.

Spurious Free Dynamic Range (SFDR)

The ratio between the power of the worst spurious signal (not always an harmonic) and the amplitude of fundamental tone (signal power) over the full Nyquist band. It is expressed in dBc.

Total Harmonic Distortion (THD)

The ratio of the rms sum of the first five harmonic distortion components to the rms value of the fundamental line. It is expressed in dB.

Signal to Noise Ratio (SNR)

The ratio of the rms value of the fundamental component to the rms sum of all other spectral components in the Nyquist band ($f_S/2$) excluding DC, fundamental and the first five harmonics. SNR is reported in dB.

Signal to Noise and Distortion Ratio (SINAD)

Similar ratio as for SNR but including the harmonic distortion components in the noise figure (not DC signal). It is expressed in dB.

From the SINAD, the Effective Number of Bits (ENOB) can easily be deduced using the formula:

$SINAD = 6.02 \times ENOB + 1.76\ dB$.

When the applied signal is not Full Scale (FS), but has an A_0 amplitude, the SINAD expression becomes:

$SINAD_{2Ao} = SINAD_{Full\ Scale} + 20 \log (2A_0/FS)$

$SINAD_{2Ao} = 6.02 \times ENOB + 1.76\ dB + 20 \log (2A_0/FS)$

The ENOB is expressed in bits.

Analog Input Bandwidth

The maximum analog input frequency at which the spectral response of a full power signal is reduced by 3dB. Higher values can be achieved with smaller input levels.

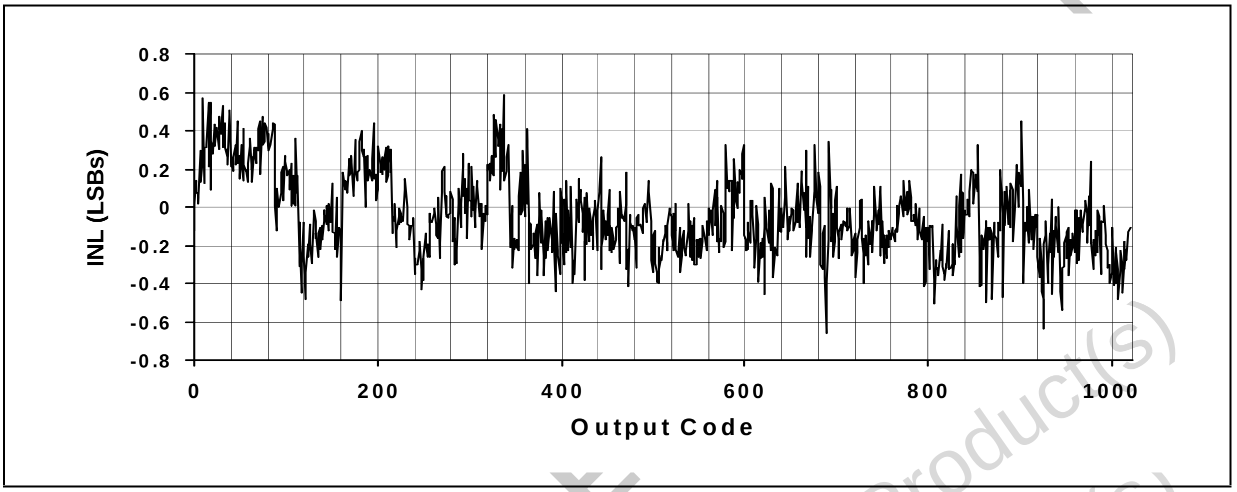
Effective Resolution Bandwidth (ERB)

The band of input signal frequencies that the ADC is intended to convert without loosing linearity i.e. the maximum analog input frequency at which the SINAD is decreased by 3dB or the ENOB by 1/2 bit.

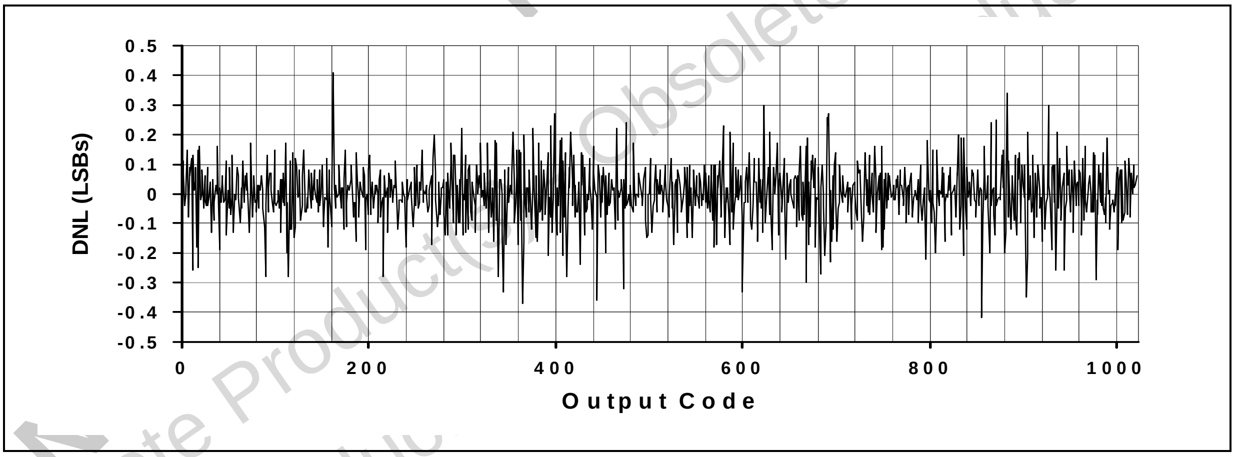
Pipeline delay

Delay between the initial sample of the analog input and the availability of the corresponding digital data output, on the output bus. Also called data latency. It is expressed as a number of clock cycles.

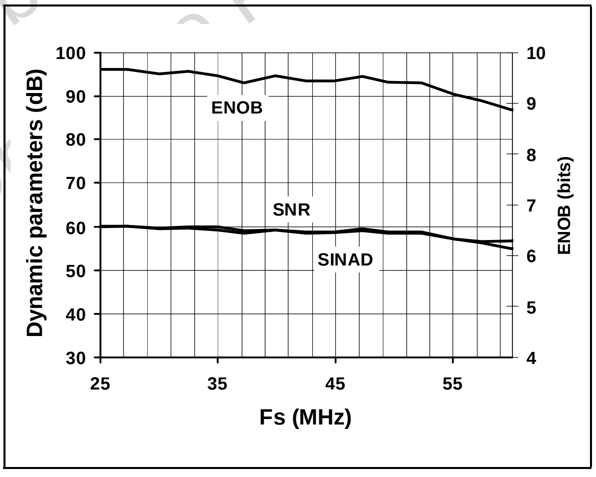
Static parameter: Integral Non Linearity
Fs=50MSPS; Fin=1MHz; Icc=20mA; N=131072pts



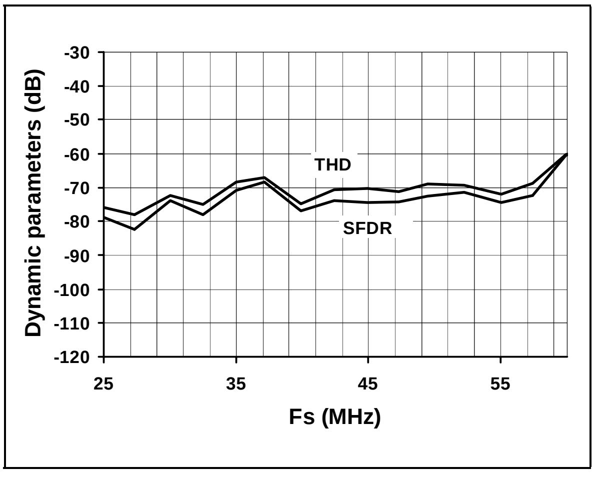
Static parameter: Differential Non Linearity Fs=50MSPS;Fin=1MHz;Icc=20mA;N=131072pts



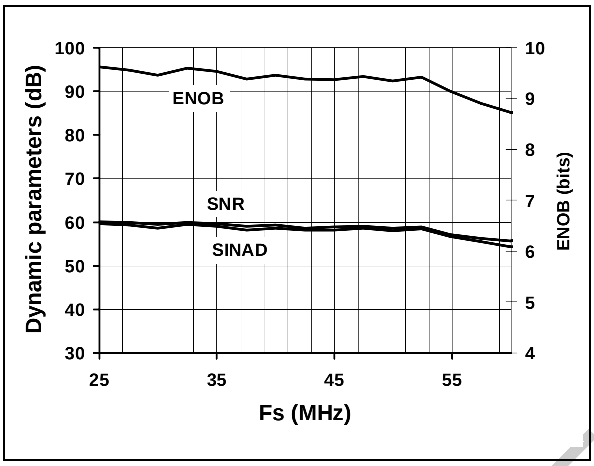
Linearity vs. Fs
Fin=5MHz; Rpol adjustment



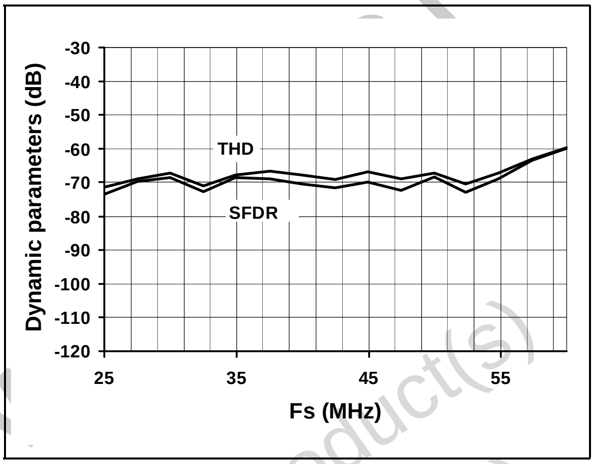
Distortion vs. Fs
Fin=5MHz; Rpol adjustment



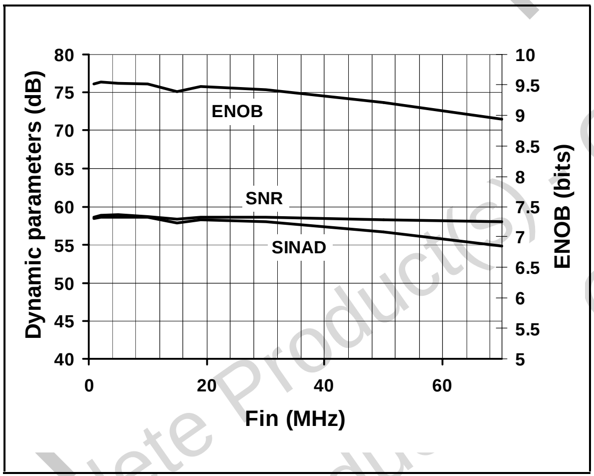
Linearity vs. Fs
Fin=15MHz; Rpol adjustment



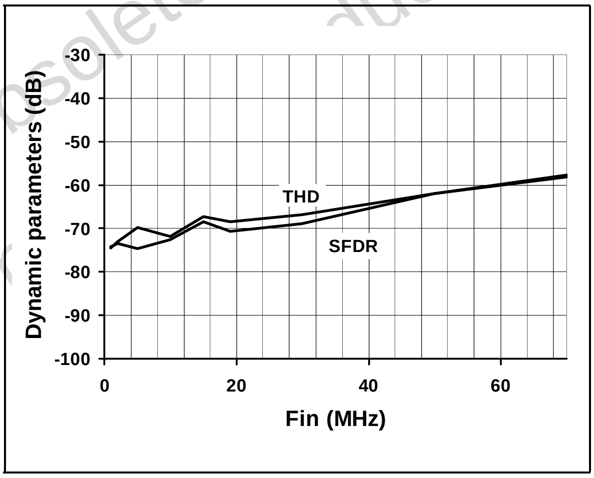
Distortion vs. Fs
Fin=15MHz; Rpol adjustment



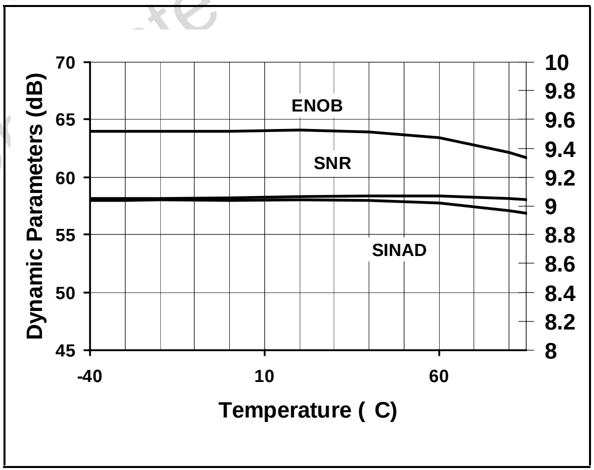
Linearity vs. Fin
Fs=50MSPS; Icca=20mA



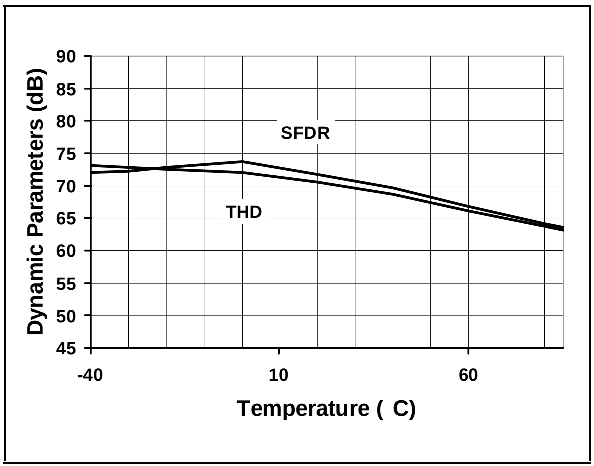
Distortion vs. Fin
Fs=50MSPS; Icca=20mA



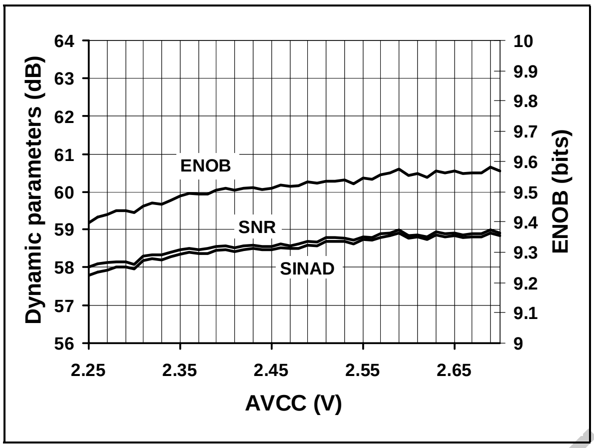
Linearity vs.Temperature
Fs=50MSPS; Icca=20mA; Fin=5MHz



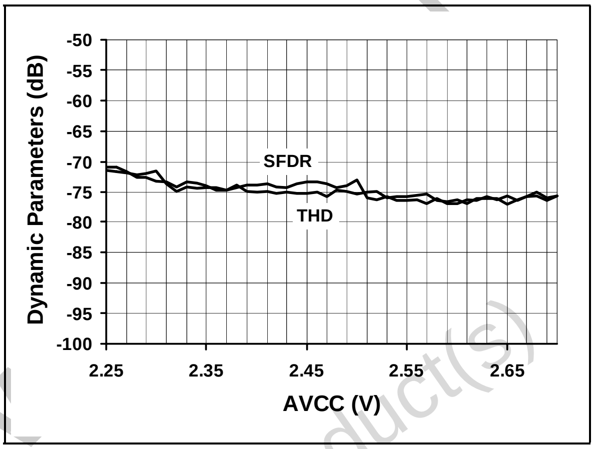
Distortion vs. Temperature
Fs=50MSPS; Icca=20mA; Fin=5MHz;



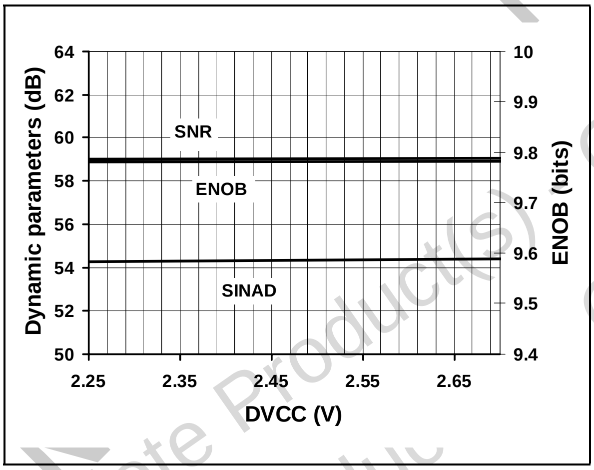
Linearity vs. AVcc
Fs=50MSPS; Icca=20mA; Fin=1MHz



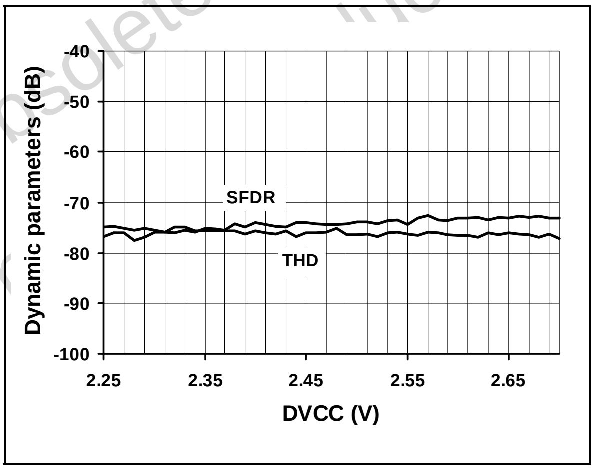
Distortion vs. AVcc
Fs=50MSPS; Icca=20mA; Fin=1MHz



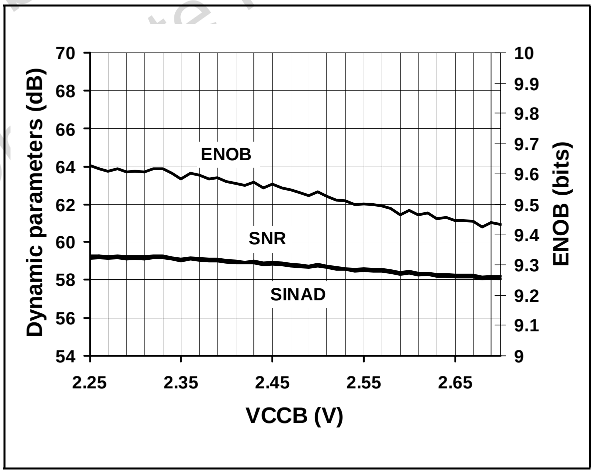
Linearity vs. DVcc
Fs=50MSPS; Icca=20mA; Fin=1MHz



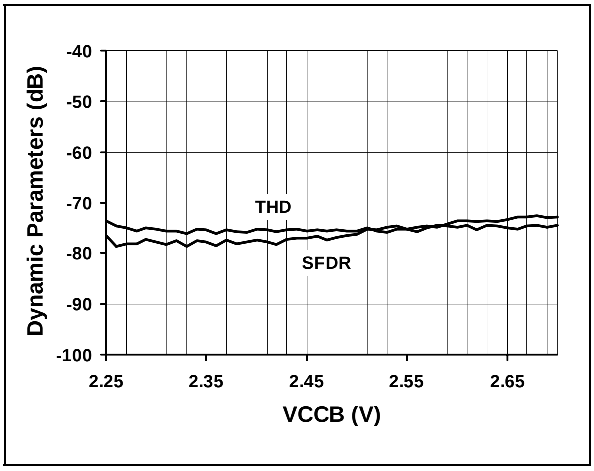
Distortion vs. DVcc
Fs=50MSPS; Icca=20mA; Fin=1MHz



Linearity vs. VccB
Fs=50MSPS; Icca=20mA; Fin=1MHz



Distortion vs. VccB
Fs=50MSPS; Icca=20mA; Fin=1MHz



DETAILED INFORMATION

The TSA1002 is a high speed analog to digital converter based on a pipeline architecture and the latest deep submicron CMOS process to achieve the best performances in terms of linearity and power consumption.

The pipeline structure consists of 9 internal conversion stages in which the analog signal is fed and sequentially converted into digital data.

Each 8 first stages consists of an Analog to Digital converter, a Digital to Analog converter, a Sample and Hold and a gain of 2 amplifier. A 1.5bit conversion resolution is achieved in each stage. The latest stage simply is a comparator. Each resulting LSB-MSB couple is then time shifted to recover from the conversion delay. Digital data correction completes the processing by recovering from the redundancy of the (LSB-MSB) couple for each stage. The corrected data are outputted through the digital buffers.

Input signal is sampled on the rising edge of the clock while digital outputs are delivered on the falling edge of the Data Ready signal.

The advantages of such a converter reside in the combination of pipeline architecture and the most advanced technologies. The highest dynamic performances are achieved while consumption remains at the lowest level.

Some functionalities have been added in order to simplify as much as possible the application board. These operational modes are described in the following table.

The TSA1002 is pin to pin compatible with the 8bits/40Msps TSA0801, the 10bits/25Msps TSA1001 and the 12bits/50Msps TSA1201. This ensures a conformity within the product family and above all, an easy upgrade of the application.

OPERATIONAL MODES DESCRIPTION

Inputs					Outputs		
Analog input differential level			DFSB	OEB	OR	DR	Most Significant Bit (MSB)
(VIN-VINB)	>	RANGE	H	L	H	CLK	D9
-RANGE	>	(VIN-VINB)	H	L	H	CLK	D9
RANGE>	(VIN-VINB)	>-RANGE	H	L	L	CLK	D9
(VIN-VINB)	>	RANGE	L	L	H	CLK	Complemented D9
-RANGE	>	(VIN-VINB)	L	L	H	CLK	Complemented D9
RANGE>	(VIN-VINB)	>-RANGE	L	L	L	CLK	Complemented D9
X			X	H	HZ	HZ	HZ

Data Format Select (DFSB)

When set to low level (VIL), the digital input DFSB provides a twoís complement digital output MSB. This can be of interest when performing some further signal processing.

When set to high level (VIH), DFSB provides a standard binary output coding.

Output Enable (OEB)

When set to low level (VIL), all digital outputs remain active and are in low impedance state. When set to high level (VIH), all digital outputs buffers are in high impedance state. This results in lower consumption while the converter goes on sampling.

When OEB is set to low level again, the data is then valid on the output with a very short Ton delay.

The timing diagram page 4 summarizes this operating cycle.

Out of Range (OR)

This function is implemented on the output stage in order to set up an "Out of Range" flag whenever the digital data is over the full scale range.

Typically, there is a detection of all the data being at í0í or all the data being at í1í. This ends up with an output signal OR which is in low level state (VOL) when the data stay within the range, or in high level state (VOH) when the data are out of the range.

Data Ready (DR)

The Data Ready output is an image of the clock being synchronized on the output data (D0 to D9). This is a very helpful signal that simplifies the synchronization of the measurement equipment or the controlling DSP.

As digital output, DR goes in high impedance state when OEB is asserted to High level as described in the timing diagram page 4.

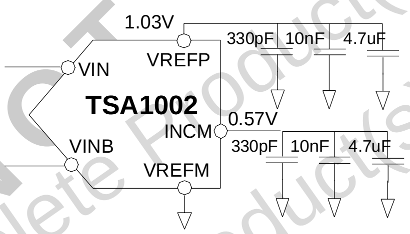
REFERENCES AND COMMON MODE CONNECTION

VREFM must be always connected externally.

Internal reference and common mode

In the default configuration, the ADC operates with its own reference and common mode voltages generated by its internal bandgap. VREFM pin is connected externally to the Analog Ground while VREFP (respectively INCM) is set to its internal voltage of 1.03V (respectively 0.57V). It is recommended to decouple the VREFP in order to minimize low and high frequency noise (refer to Figure 1)

Figure 1 : Internal reference and common mode setting



External reference and common mode

Each of the voltages VREFM, VREFP and INCM can be fixed externally to better fit to the application needs (Refer to Table íOPERATING CONDITIONSí p2 for min and max values).

The VREFP, VREFM voltages set the analog dynamic at the input of the converter that has a full scale amplitude of 2*(VREFP-VREFM).

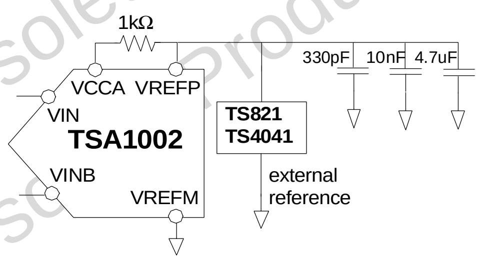
In case of analog dynamic lower than 2Vpp, the best linearity and distortion performance is achieved while increasing the VREFM voltage instead of lowering the VREFP one.

The INCM is the mid voltage of the analog input signal.

It is possible to use an external reference voltage device for specific applications requiring even better linearity, accuracy or enhanced temperature behavior.

Using the STMicroelectronics TS821 or TS4041-1.2 Vref leads to optimum performances when configured as shown on Figure 2.

Figure 2 : External reference setting



At 15Msps sampling frequency, 1MHz input frequency and -1dBFS amplitude signal, performances can be improved up to 2dB on SFDR and 0.3dB on SINAD. At 50Msps sampling frequency, 1MHz input frequency and -1dBFS amplitude signal, performances can be improved up to 1dBc on SFDR and 0.6dB on SINAD.

This can be very helpful for example for multichannel application to keep a good matching among the sampling frequency range.

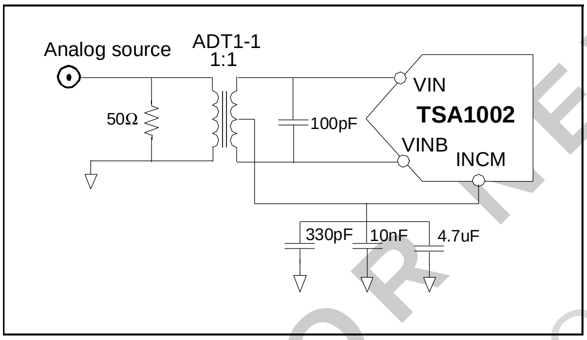
DRIVING THE ANALOG INPUT

Differential inputs

The TSA1002 has been designed to obtain optimum performances when being differentially driven. An RF transformer is a good way to achieve such performances.

Figure 3 describes the schematics. The input signal is fed to the primary of the transformer, while the secondary drives both ADC inputs.

Figure 3 : Differential input configuration with transformer



The common mode voltage of the ADC (INCM) is connected to the center-tap of the secondary of the transformer in order to bias the input signal around this common voltage, internally set to 0.57V. The INCM is decoupled to maintain a low noise level on this node. Our evaluation board is mounted with a 1:1 ADT1-1WT transformer from Minicircuits. You might also use a higher impedance ratio (1:2 or 1:4) to reduce the driving requirement on the analog signal source. For example, with internal references, each analog input can drive a 1Vpp amplitude input signal, so the resultant differential amplitude is 2Vpp.

Figure 4 : AC-coupled differential input

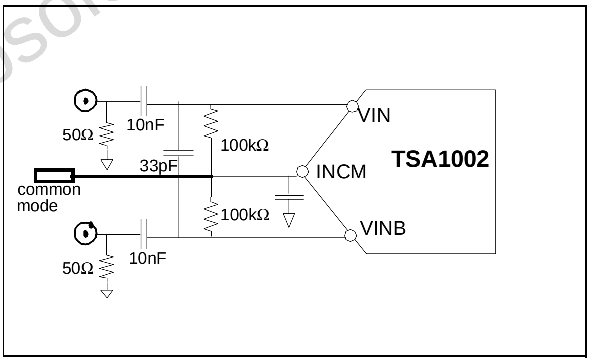
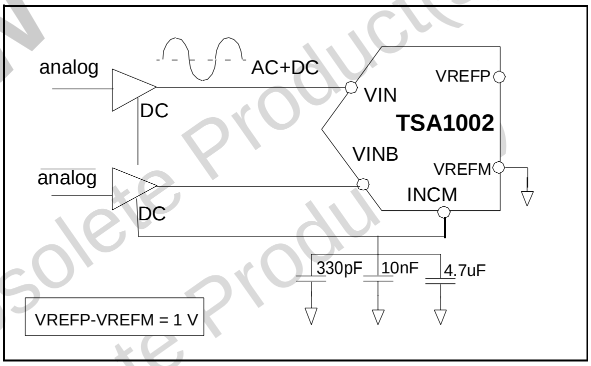


Figure 4 represents the biasing of a differential input signal in AC-coupled differential input configuration. Both inputs VIN and VINB are centered around the common mode voltage, that can be let internal or fixed externally.

Figure 5 shows a DC-coupled configuration with forced INCM to the DC analog input (mid-voltage) while VREFM is connected to ground and VREFP is let internal (1V); we achieve a 2Vpp differential amplitude.

Figure 5 : DC-coupled 2Vpp differential analog input



Single-ended input configuration

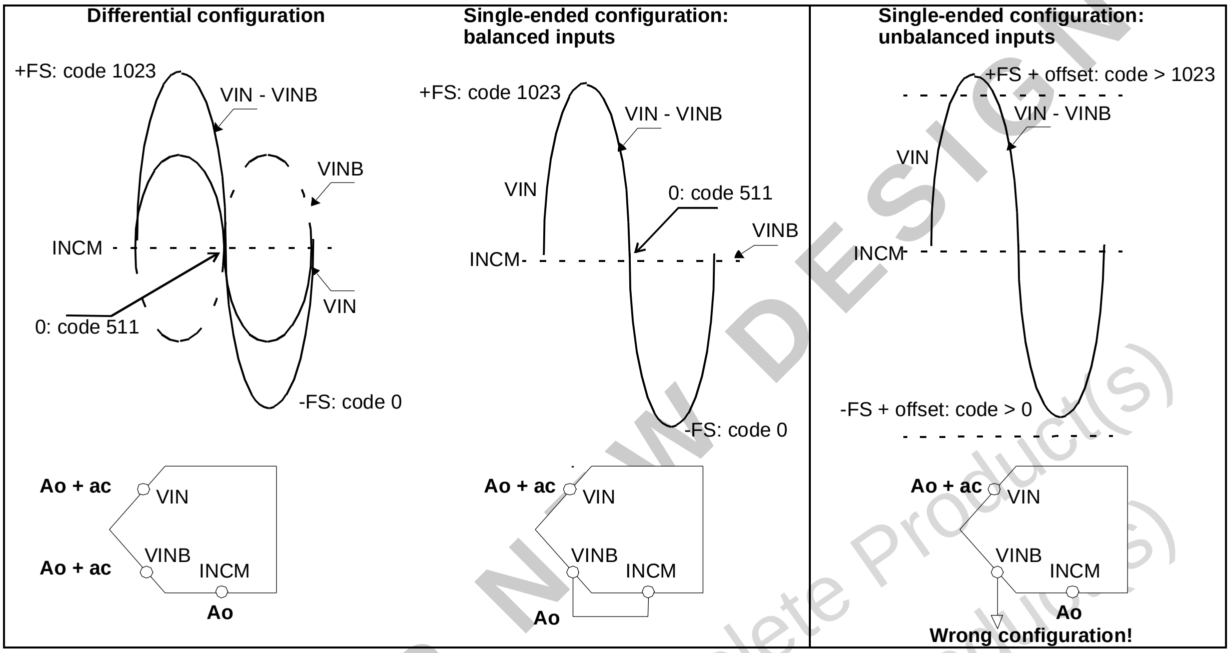
The single-ended input configuration of the TSA1002 requires particular biasing and driving. The structure being fully differential, care has to be taken in order to properly bias the inputs in single ended mode. Figure 6 summarizes the link from the differential configuration to the single-ended one; a wrong configuration is also presented.

- With differential driving, both inputs are centered around the INCM voltage.

- The transition to single-ended configuration implies to connect the unused input (VINB for instance) to the DC component of the single input (Vin) and also to the input common mode in order to be well balanced. The mid-code is achieved at the crossing between VIN and VINB, therefore inputs are conveniently biased.

- Unlikely other structures of converters in which the unused input can be grounded; in our case it will end with unbalanced inputs and saturation of the internal amplifiers leading to a non respect of the output codes.

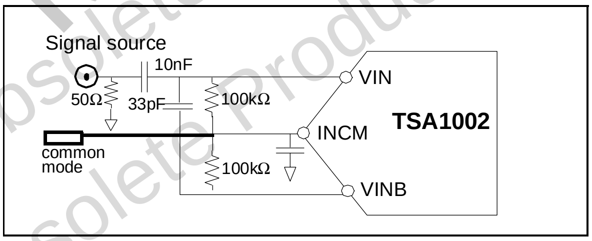
Figure 6 : Input dynamic range for the various configurations



The applications requiring single-ended inputs can be configured like reported on Figure 7 for an AC-coupled input or on Figure 8 and 9 for a DC-coupled input.

In the case of AC-coupled analog input, the analog inputs Vin and Vinb are biased to the same voltage that is the common mode voltage of the circuit (INCM). The INCM and reference voltages may remain at their internal level but can also be fixed externally.

Figure 7 : AC-coupled Single-ended input



In the case of DC-coupled analog input with 1V DC signal, the DC component of the analog input set the common mode voltage. As an example figure 8, INCM is set to the 1V DC analog input while VREFM is connected to ground and VREFP let internal; we achieve a 2Vpp differential amplitude.

Figure 9 describes a configuration for a 1Vpp analog signal with a 0.5V DC input. In this case, while VREFP is kept internally at 1V, VREFM is connected to VINB and INCM externally to 0.5V; the dynamic is then 1Vpp (VREFP-VREFM=0.5V).

Figure 8 : DC-coupled 2Vpp analog input

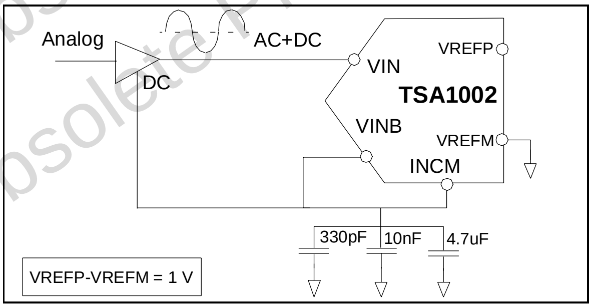
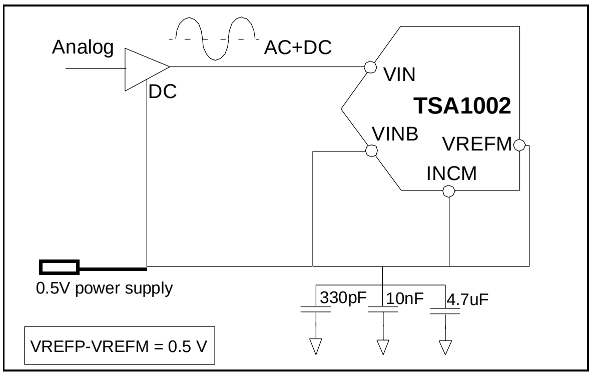


Figure 9 : DC-coupled 1Vpp analog input



Dynamic characteristics, while not being as remarkable as for differential configuration, are still of very good quality. Measurements done at 50Msps, 2MHz input frequency, -1dBFS input level sum up these performances. An SFDR of -64.5dBc, a SNR of 57.8dB and an ENOB Full Scale of 9.3bits are achieved.

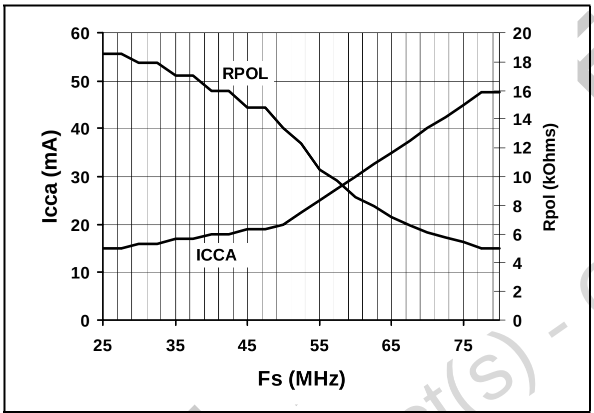
Power consumption

The internal architecture of the TSA1002 enables to optimize the power consumption according to the sampling frequency of the application. For this purpose, a resistor is placed between IPOL and the analog Ground pins. The figure 10 sums up the relevant data.

The TSA1002 will combine highest performances and lowest consumption at 50Msps when Rpol is in the range of 12kΩ to 20kΩ.

At lower sampling frequency, this value of resistor may be changed and the consumption will decrease as well.

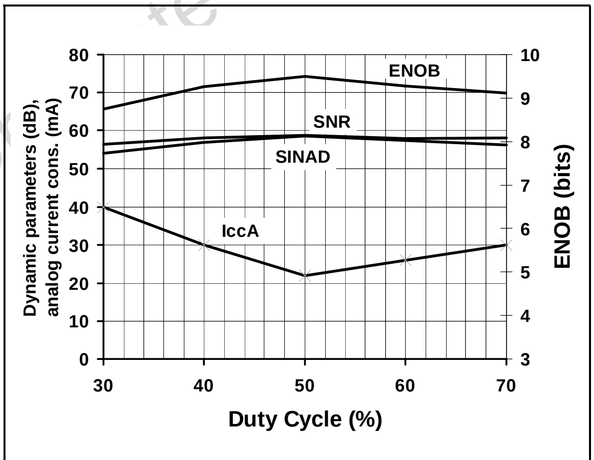
Figure 10 : Analog Current consumption vs. Fs According value of Rpol polarization resistance



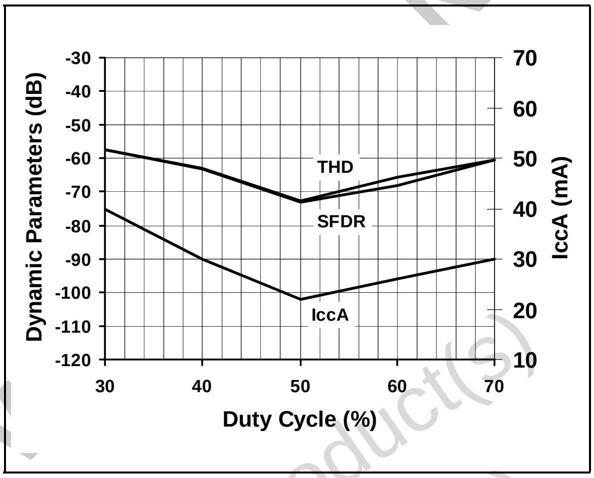
Linearity, distortion performance towards Clock Duty Cycle variation

The TSA1002 has an outstanding behaviour towards clock duty cycle variation and it may be also reinforced with adjustment of analog current consumption.

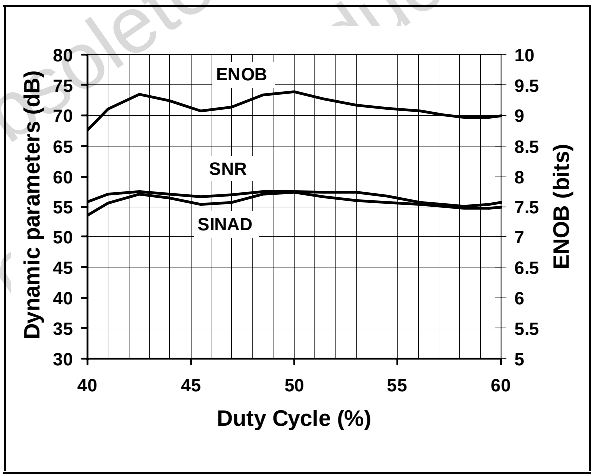
Linearity vs. Duty cycle
Fs=50MSPS; consumption optimized; Fin=1MHz



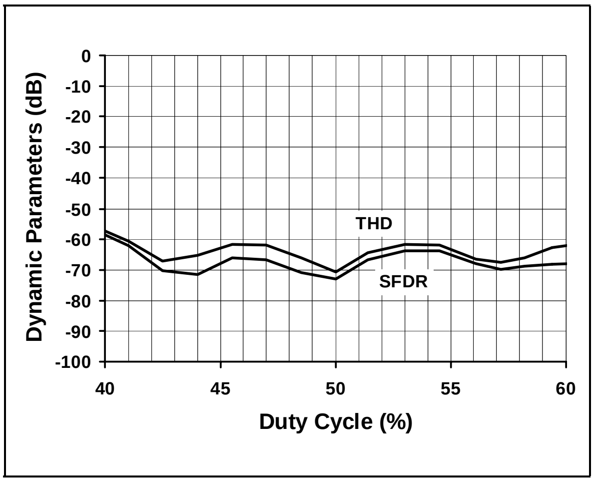
Distortion vs. Duty cycle
Fs=50MSPS; consumption optimized; Fin=1MHz



Linearity vs. Duty cycle
Fs=50MSPS; Icca=20mA; Fin=10MHz



Distortion vs. Duty cycle
Fs=50MSPS; Icca=20mA; Fin=10MHz



Clock input

The quality of your converter is very dependant on your clock input accuracy, in terms of aperture jitter; the use of low jitter crystal controlled oscillator is recommended.

The clock power supplies must be separated from the ADC output ones to avoid digital noise modulation at the output.

It is recommended to keep the circuit clocked, to avoid random states, before applying the supply voltages.

Layout precautions

To use the ADC circuits in the best manner at high frequencies, some precautions have to be taken for power supplies:

- First of all, the implementation of 4 separate proper supplies and ground planes (analog, digital, internal and external buffer ones) on the PCB is recommended for high speed circuit applications to provide low inductance and low resistance common return.

The separation of the analog signal from the digital part is essential to prevent noise from coupling onto the input signal.

- Power supply bypass capacitors must be placed as close as possible to the IC pins in order to improve high frequency bypassing and reduce harmonic distortion.

- Proper termination of all inputs and outputs is needed; with output termination resistors, the amplifier load will be only resistive and the stability of the amplifier will be improved. All leads must be wide and as short as possible especially for the analog input in order to decrease parasitic capacitance and inductance.

- To keep the capacitive loading as low as possible at digital outputs, short lead lengths of routing are essential to minimize currents when the output changes. To minimize this output capacitance, buffers or latches close to the output pins will relax this constraint.

- Choose component sizes as small as possible (SMD).

EVAL1002 evaluation board

The characterization of the board has been made with a fully ADC devoted test bench as shown on Figure 11. The analog signal must be filtered to be very pure.

The dataready signal is the acquisition clock of the logic analyzer.

The ADC digital outputs are latched by the 74LCX573 octal buffers.

All characterization measurement has been made with an input amplitude of +0.2dB for static parameters and -0.5dB for dynamic parameters.

Figure 11 : Analog to Digital Converter characterization bench

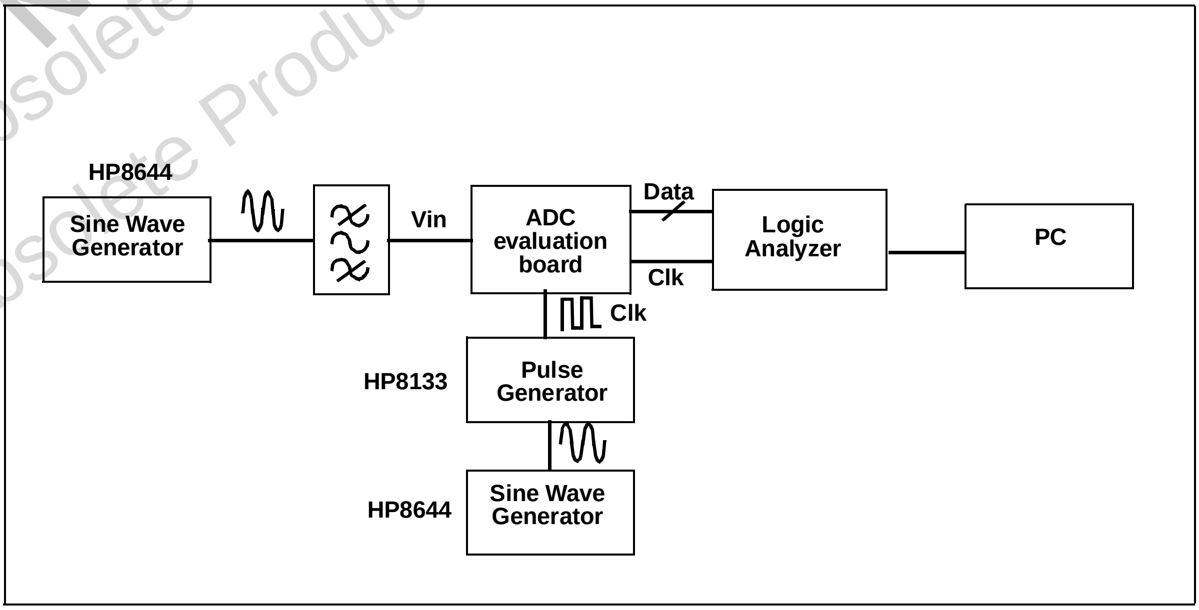


Figure 12: TSA1002 Evaluation board schematic

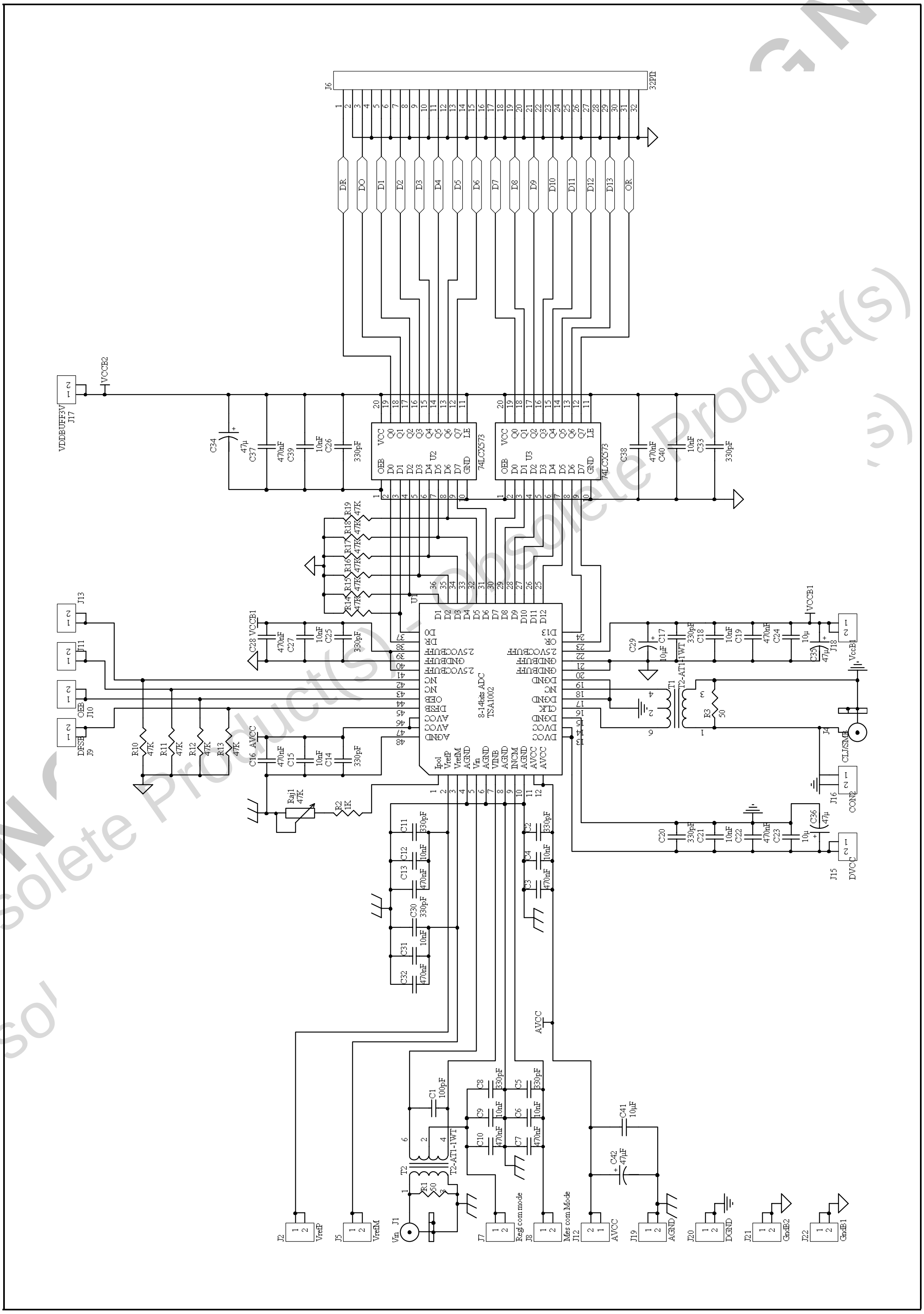
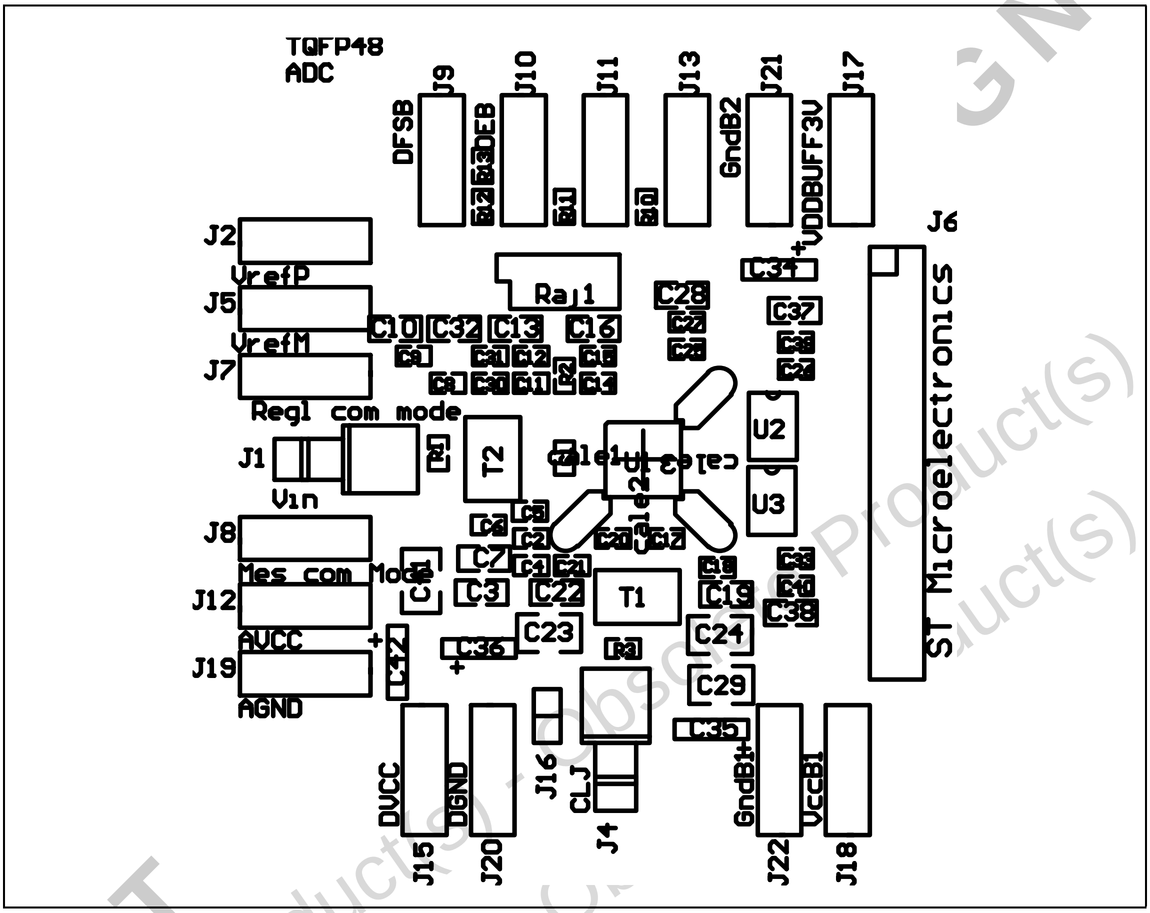


Figure 13: Printed circuit of evaluation board

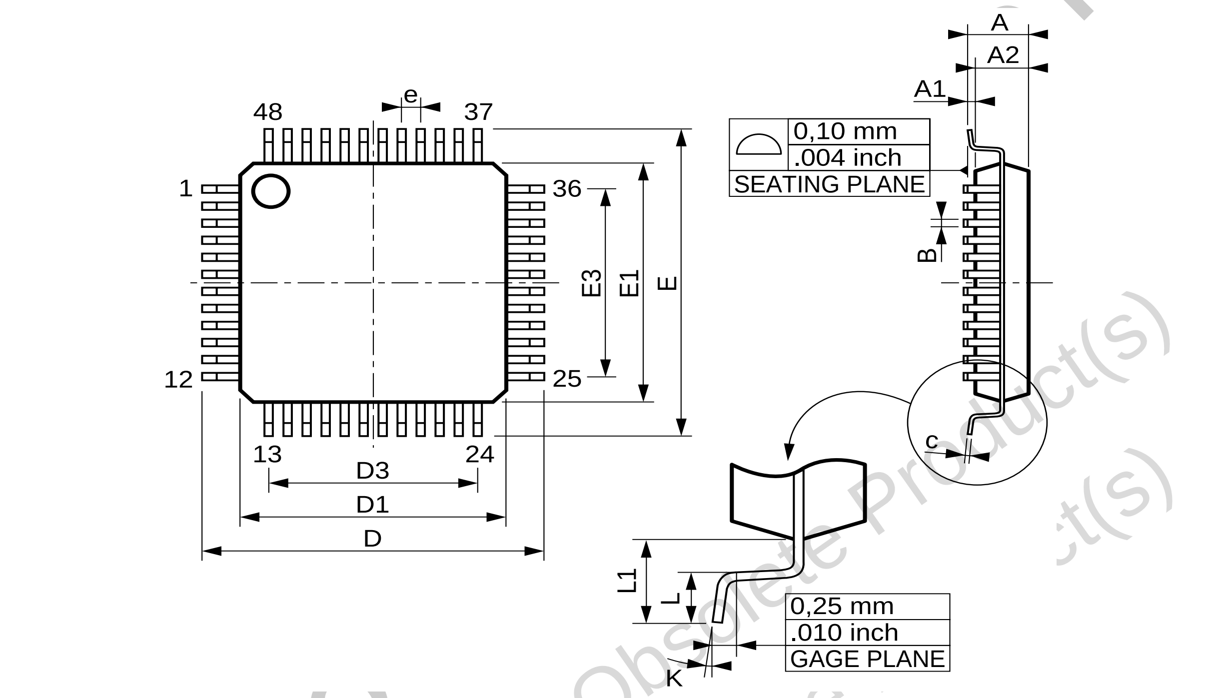


Printed circuit board - List of components

Part	Design	Footprint	Part	Design	Footprint	Part	Design	Footprint	Part	Design	Footprint
Type	ator		Type	ator		Type	ator		Type	ator	
10uF	C24	1210	330pF	C33	603	470nF	C7	805	AVCC	J12	FICHE2MM
10uF	C23	1210	330pF	C20	603	470nF	C16	805	CLJ/SMB	J4	SMB/H
10uF	C41	1210	330pF	C8	603	470nF	C19	805	AGND	J19	FICHE2MM
10uF	C29	1210	330pF	C2	603	470nF	C3	805	DFSB	J9	FICHE2MM
100pF	C1	603	330pF	C5	603	47KΩ	R12	603	DGND	J20	FICHE2MM
10nF	C12	603	330pF	C11	603	47KΩ	R14	603	DVCC	J15	FICHE2MM
10nF	C39	603	330pF	C30	603	47KΩ	R11	603	GndB1	J22	FICHE2MM
10nF	C15	603	330pF	C17	603	47KΩ	Raj1	VR5	GndB2	J21	FICHE2MM
10nF	C40	603	330pF	C14	603	47KΩ	R10	603	Mes com mode	J8	FICHE2MM
10nF	C27	603	47uF	C36	CAP	47KΩ	R19	603	OEB	J10	FICHE2MM
10nF	C4	603	47uF	C34	CAP	47KΩ	R13	603	Regl com mode	J7	FICHE2MM
10nF	C21	603	47uF	C35	CAP	47KΩ	R15	603	T2-AT1-1WT	T2	ADT
10nF	C31	603	47uF	C42	CAP	47KΩ	R16	603	T2-AT1-1WT	T1	ADT
10nF	C6	603	470nF	C22	805	47KΩ	R17	603	VccB1	J18	FICHE2MM
10nF	C9	603	470nF	C32	805	47KΩ	R18	603	VDDBUFF3V	J17	FICHE2MM
10nF	C18	603	470nF	C37	805	50Ω	R3	603	Vin	J1	SMB/H
1KΩ	R2	603	470nF	C38	805	50Ω	R1	603	VrefM	J5	FICHE2MM
32PIN	J6	IDC32	470nF	C13	805	74LCX573	U3	TSSOP20	VrefP	J2	FICHE2MM
330pF	C25	603	470nF	C28	805	74LCX573	U2	TSSOP20	TSA1002	U1	TQFP48
330pF	C26	603	470nF	C10	805	CON2	J16	SIP2			

PACKAGE MECHANICAL DATA

48 PINS - PLASTIC PACKAGE



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.216	
e		0.50			0.0197	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.216	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0 (min.), 7 (max.)					