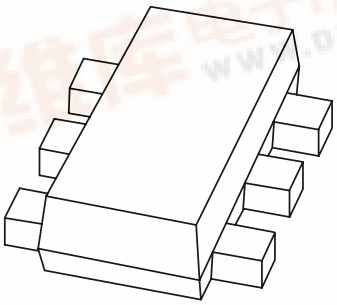
DATA SHEET



PEMB11
PNP resistor-equipped transistors; R1 = 10 kΩ, R2 = 10 kΩ

Preliminary specification

2001 Sep 13

PNP resistor-equipped transistors; R1 = 10 kΩ, R2 = 10 kΩ

PEMB11

FEATURES

- 300 mW total power dissipation
- Very small 1.6 mm x 1.2 mm ultra thin package
- Excellent coplanarity due to straight leads
- Replaces two SC-75/SC-89 packaged transistors on same PCB area
- Reduces required PCB area
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

DESCRIPTION

PNP resistor-equipped transistors in a SOT666 plastic package.

MARKING

TYPE NUMBER	MARKING CODE
PEMB11	B1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	–50	V
I_{CM}	peak collector current	–100	mA
TR1	PNP	–	–
TR2	PNP	–	–
R1	bias resistor	10	kΩ
R2	bias resistor	10	kΩ

PINNING

PIN	DESCRIPTION	
1, 4	emitter	TR1; TR2
2, 5	base	TR1; TR2
6, 3	collector	TR1; TR2

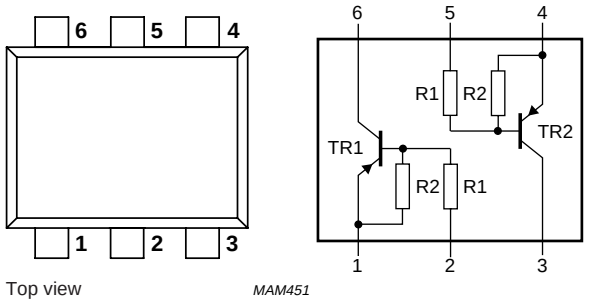


Fig.1 Simplified outline (SOT666) and symbol.

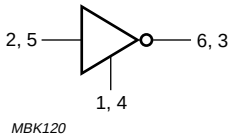


Fig.2 Equivalent inverter symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor unless otherwise specified					
V_{CBO}	collector-base voltage	open emitter	–	–50	V
V_{CEO}	collector-emitter voltage	open base	–	–50	V
V_{EBO}	emitter-base voltage	open collector	–	–10	V
V_I	input voltage				
	positive		–	+10	V
	negative		–	–40	V
I_O	output current (DC)		–	–100	mA
I_{CM}	peak collector current		–	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	300	mW

Note

1. Transistor mounted on a FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	notes 1 and 2	416	K/W

Notes

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering method is reflow soldering.

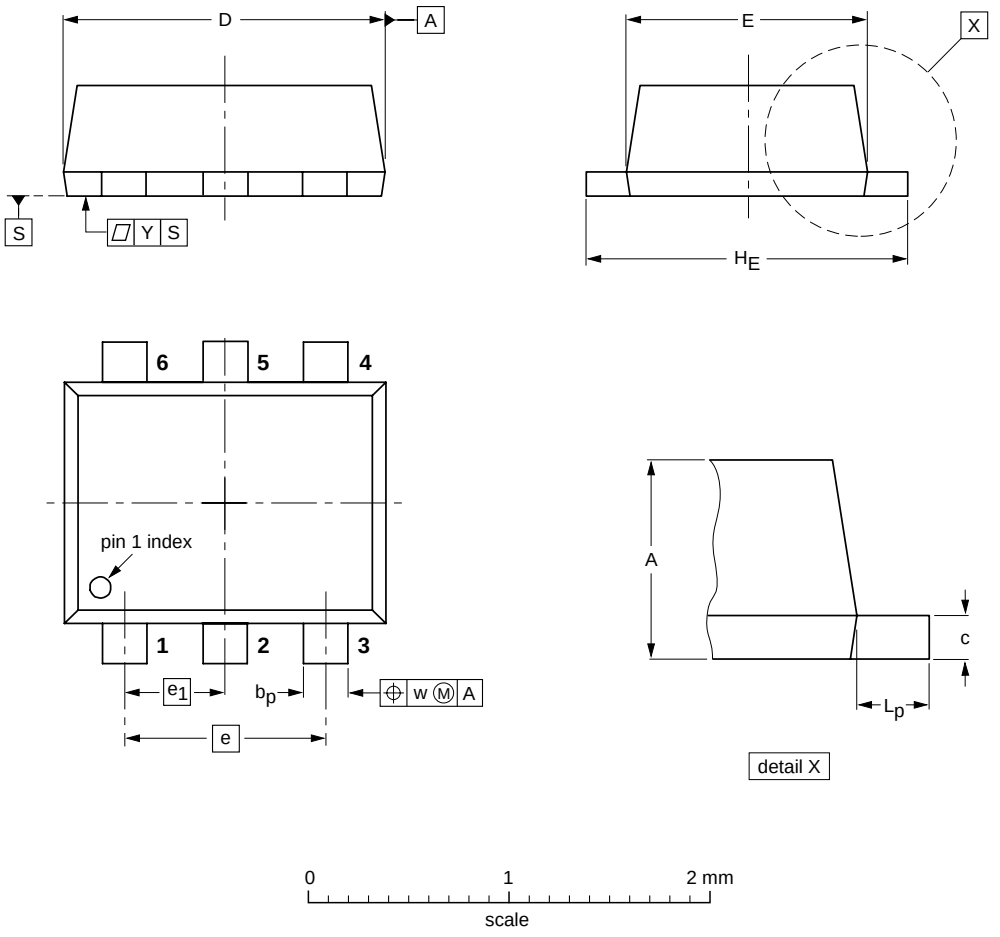
CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor unless otherwise specified						
I_{CBO}	collector-base cut-off current	V_{CB} = –50 V; I_C = 0	–	–	–100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = –50 V; I_B = 0	–	–	–1	µA
		V_{CE} = –30 V; I_B = 0; T_j = 150 °C	–	–	–50	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = –5 V; I_C = 0	–	–	–400	µA
h_{FE}	DC current gain	V_{CE} = –5 V; I_C = –5 mA	30	–	–	
V_{CEsat}	collector-emitter saturation voltage	I_C = –10 mA; I_B = –0.5 mA	–	–	–150	mV
$V_{i(off)}$	input off voltage	V_{CE} = –5 V; I_C = –100 µA	–	–1.1	–0.8	V
$V_{i(on)}$	input on voltage	V_{CE} = –0.3 V; I_C = –10 mA	–2.5	–1.8	–	V
R1	input resistor		7	10	13	kΩ
$\frac{R2}{R1}$	resistor ratio		0.8	1.0	1.2	kΩ
C_c	collector capacitance	$I_E = I_e$ = 0; V_{CB} = –10 V; f = 1 MHz	–	–	3	pF

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads **SOT666**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						~~01-01-04~~ 01-08-27

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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