PET1600-12-074NA

FEATURES

- Best-in-class, 80 PLUS certified “Platinum” efficiency
- INTEL CRPS (Common Redundant Power Supply) compatible
- Wide input voltage range: 90-264 V_{AC}
- AC input with power factor correction
- 1600W continuous and 2100W peak output power capability
- Always-On 12V/3.5A standby output
- Hot-plug capable
- Parallel operation with active current sharing
- Full digital controls for improved performance
- High density design: 33.7 W/in3
- Small form factor: 73.5 x 40.0 x 265mm
- PMBus communication interface for control, programming and monitoring
- Status LED with fault signalling

DESCRIPTION

The **PET1600-12-074NA** is a 1600 Watt AC to DC, power-factor-corrected (PFC) power supply that converts standard AC power into a main output of +12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches. The PET1600-12-074NA utilizes full digital control architecture for greater efficiency, control, and functionality. This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

1 ORDERING INFORMATION

PET	1600	-	12	-	074	N	A
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**
PET Front-Ends	1600 W		12 V		74 mm	N: Normal	A: AC

2 OVERVIEW

The PET1600-12-074NA AC/DC power supply is a fully DSP controlled, highly efficient front-end power supply. It incorporates resonance-soft-switching technology to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operational voltage range the PET1600-12-074NA maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.

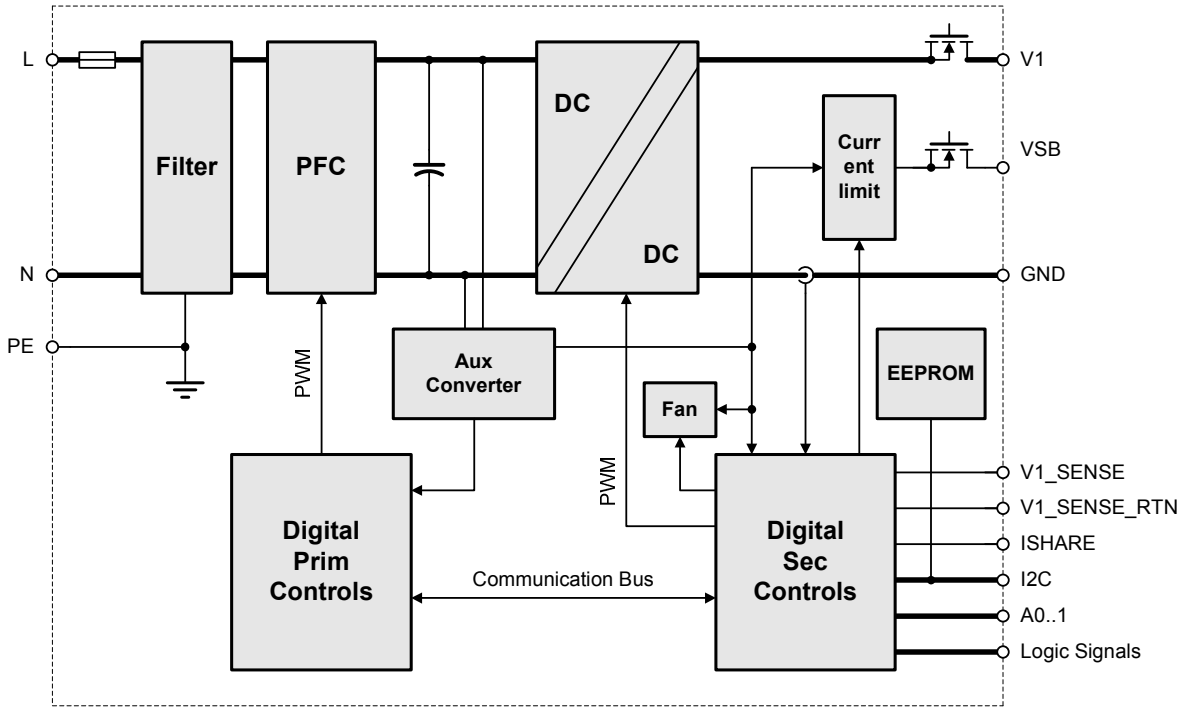
The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range.

The DC/DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.

Status information is provided with a front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I²C bus. The I²C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.

Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I²C bus.



3 ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,maxc}$	Maximum Input Voltage	Continuous			264	VAC

4 INPUT

General Condition: T_A = 0…55 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,nom}$	Nominal Input Voltage	Rated Voltage High Line ($V_{i\,nom\,HL}$)	200	230	240	VAC
		Rated Voltage Low Line ($V_{i\,nom\,LL}$)	100	115	127	VAC
V_i	Input Voltage Ranges	Normal operating ($V_{i\,min\,HL}$ to $V_{i\,max\,HL}$), High Line	180		264	VAC
		Normal operating ($V_{i\,min\,LL}$ to $V_{i\,max\,LL}$), Low Line	90		140	VAC
$I_{i\,max}$	Maximum Input Current	V_{IN}=100VAC, 100% load			13	A_{RMS}
$I_{i\,inrush}$	Inrush Current Limitation	Vi_{min} to Vi_{max}, T_{NTC}=25°C, 5ms			10	A_p
f_i	Input Frequency		47	50/60	63	Hz
PF	Power Factor	10% Load	0.8			W/VA
		20% Load	0.9			W/VA
		50% Load	0.9			W/VA
		100% Load	0.95			W/VA
THD	Total Harmonic Distortion	TBD			TBD	%
$V_{i\,on}$	Turn-on Input Voltage[1]	Ramping up	87		90	VAC
$V_{i\,off}$	Turn-off Input Voltage[1]	Ramping down	82		87	VAC
η	Efficiency[2]	V_{IN}=230VAC, 10% load	82	90.8		%
		V_{IN}=230VAC, 20% load	90	93.5		%
		V_{IN}=230VAC, 50% load	94	94.4		%
		V_{IN}=230VAC, 100% load	91	93.0		%
$T_{V1\,holdup}$	Hold-up Time V_1	12V output, 70% Load	10.6			ms
$T_{VSB\,holdup}$	Hold-up Time V_{SB}	12V_{SB}, full load	70			ms

4.1 INPUT FUSE

Time-lag 16A input fuse (5 x 20 mm) in series with the L-line inside the power supply protects against severe defects. The fuse is not accessible from the outside and is therefore not a serviceable part.

4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only 5.2µF, resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through an NTC which will limit the inrush current.

NOTE: Do not repeat plug-in / out operations within a short time, or else the internal in-rush current limiting device (NTC) may not sufficiently cool down and excessive inrush current or component failure(s) may result.

4.3 INPUT UNDER-VOLTAGE

If the sinusoidal input voltage stays below the input undervoltage lockout threshold $V_{i\,on}$, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

[1] The Front-End is provided with a minimum hysteresis of 3V during turn-on and turn-off within the ranges
[2] Efficiency measured without fan power per EPA server guidelines

4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage. If for instance the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform.

4.5 EFFICIENCY

High efficiency (see *Figure 1*) is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

Figure 1 - Efficiency vs. Load current (ratio metric loading)

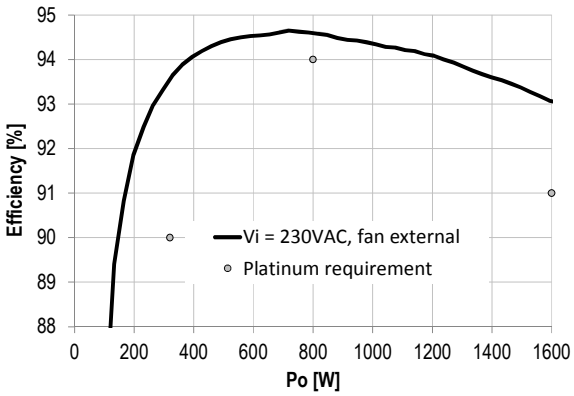


Figure 2 - Power factor vs. Load current

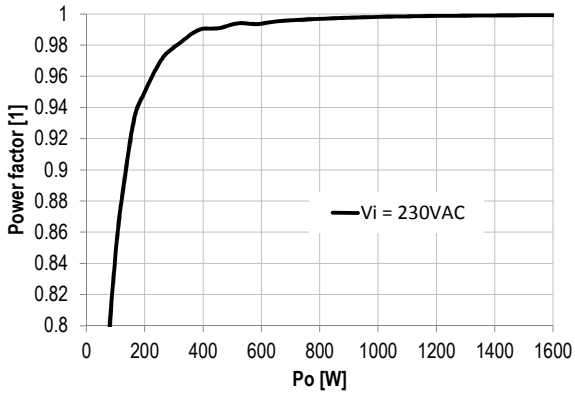
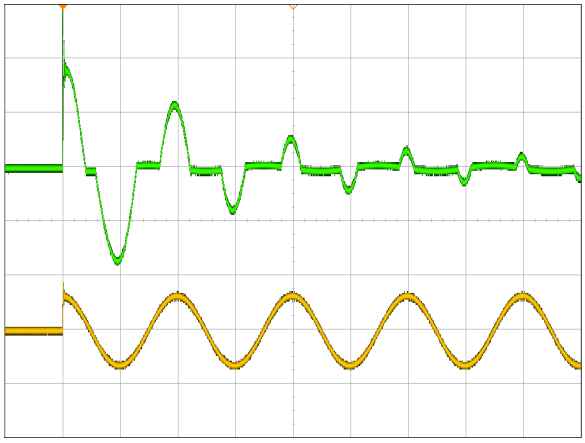


Figure 3 - Inrush current, V_{in} = 230Vac, 90°
CH1: V_{in} (500V/div), CH2: I_{in} (10A/div)



5 OUTPUT

General Condition: T_A = 0…55 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_A = 25°C		12.0		VDC
$V_{1\ set}$	Output Setpoint Accuracy		-0.5		+0.5	%$V_{1\ nom}$
$dV_{1\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$	-1		+1	%$V_{1\ nom}$
$P_{1\ nom}$	Nominal output power	$V_{i\ min\ HL}$ to $V_{i\ max\ HL}$		1600		W
		$V_{i\ min\ LL}$ to $V_{i\ max\ LL}$		1000		W
$P_{1\ peak}$	Peak Output Power[3]	$V_{i\ min\ HL}$ to $V_{i\ max\ HL}$		2100		W
		$V_{i\ min\ LL}$ to $V_{i\ max\ LL}$		1320		W
$I_{1\ nom}$	Output Current	$V_{i\ min\ HL}$ to $V_{i\ max\ HL}$	0.0		133	ADC
$I_{1\ nom\ red}$		$V_{i\ min\ LL}$ to $V_{i\ max\ LL}$	0.0		83	ADC
$I_{1\ peak}$	Peak Output Current[3]	$V_{i\ min\ HL}$ to $V_{i\ max\ HL}$	0.0		175	ADC
$I_{1\ peak\ red}$		$V_{i\ min\ LL}$ to $V_{i\ max\ LL}$	0.0		110	ADC
$V_{1\ pp}$	Output Ripple Voltage[4]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, $T_{A\ min}$ to $T_{A\ max}$			120	mVpp
$dV_{1\ load}$	Load Regulation	$V_{i\ nom\ HL}$, 0 to 100% $I_{1\ nom}$	-67	-89	-111	mV
$dV_{1\ line}$	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0.5 · $I_{1\ nom}$	-24	0	24	mV
$dV_{1\ temp}$	Thermal Drift	$V_{i\ nom\ HL}$, 0.5 · $I_{1\ nom}$			TBD	%/°C
$dI_{1\ share}$	Current Sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 10%	-4		+4	ADC
V_{iSHARE}	Current Share Bus Voltage	$I_{1\ peak}$	9.93	10.0	10.07	VDC
$dV_{1\ dyn}$	Dynamic Load Regulation	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 5 … 100% $I_{1\ nom}$,	11.40		12.60	VDC
t_{rec}	Recovery Time	dI_1/dt = 1A/µs, recovery within 1% of $V_{1\ nom}$			2	ms
$t_{V1\ rise}$	Output Voltage Rise Time	V_1 = 10…90% $V_{1\ nom}$, external capacitance < 10mF	6	8	10	ms
$t_{V1\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom\ HL}$, 0 to 100% $I_{1\ nom}$			12.60	V
$dV_{1\ sense}$	Remote Sense	Compensation for cable drop, 0 to 100% $I_{1\ nom}$			0.25	V
$C_{V1\ load}$	Capacitive Loading		0		25	mF
Standby Output V_{SB}						
$V_{SB\ nom}$	Nominal Output Voltage	I_{SB} = 0A, T_A = 25°C		12.15		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-0.5		+0.5	%V_{SBnom}
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$	-3		+1	%V_{SBnom}
$P_{SB\ nom}$	Nominal output power	$V_{i\ min}$ to $V_{i\ max}$		42		W
$P_{SB\ peak}$	Peak Output Power[5]	$V_{i\ min}$ to $V_{i\ max}$		48		W
$I_{SB\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$	0.0		3.5	ADC
$I_{SB\ peak}$	Peak Output Current[5]	$V_{i\ min}$ to $V_{i\ max}$	0.0		4	ADC
$V_{SB\ pp}$	Output Ripple Voltage[4]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{A\ min}$ to $T_{A\ max}$			120	mVpp
$dV_{SB\ load}$	Load Regulation	$V_{i\ nom\ HL}$, 0 to 100% $I_{SB\ nom}$	-200	-300	-400	mV
$dV_{SB\ line}$	Line Regulation	$V_{i\ min}$ to $V_{i\ max}$, $I_{SB\ nom}$ = 0A	-24	0	24	mV
$dV_{SB\ temp}$	Thermal Drift	$V_{i\ nom\ HL}$, $I_{SB\ nom}$ = 0A			TBD	%/°C
$dI_{SB\ share}$	Current Sharing	Deviation from $I_{SB\ tot}$ / N, I_{SB} = 0.5 · $I_{SB\ nom}$	-1		+1	ADC
$dV_{SB\ dyn}$	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5 … 100% $I_{SB\ nom}$,	11.40		12.60	VDC
t_{rec}	Recovery Time	dI_{SB}/dt = 0.25A/µs, recovery within 1% of $V_{SB\ nom}$			2	ms
$t_{VSB\ rise}$	Output Voltage Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$, external capacitance < 1mF	1	2	5	ms
$t_{VSB\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom\ HL}$, 0 to 100% $I_{SB\ nom}$			12.60	V
$C_{VSB\ load}$	Capacitive Loading		0		3100	µF

[3] Peak combined power for all outputs does not exceed 2100 W; maximum of peak power duration is 20 seconds without asserting the SMBAlert signal.
[4] Measured with a 10uF low ESR capacitor in parallel with a 0.1uF ceramic capacitor at the point of measurement.
[5] In single power supply configuration.

Figure 4 - Turn-On AC Line 230VAC, full load (200ms/div)
CH1: Vin (500V/div) CH3: V_1 (2V/div) CH4: V_{SB} (2V/div)

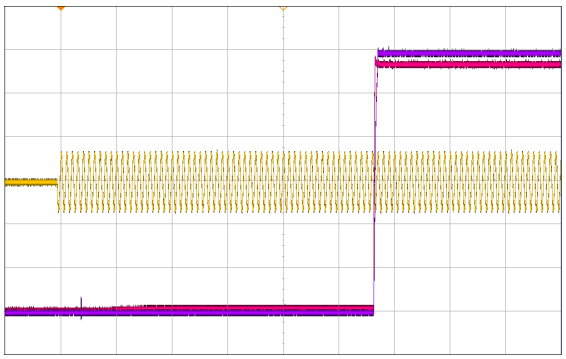


Figure 5 - Turn-On AC Line 230VAC, full load (5ms/div)
CH3: V_1 (2V/div) CH4: V_{SB} (2V/div)

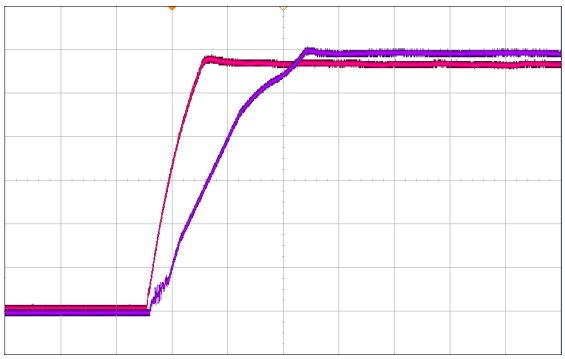


Figure 6 - Turn-Off AC Line 230VAC, full load (10ms/div)
CH1: Vin (500V/div) CH3: V_1 (2V/div) CH4: V_{SB} (2V/div)

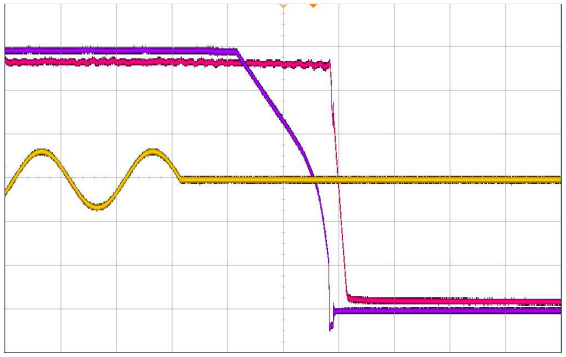


Figure 7 - Short circuit on V1 (10ms/Div)
CH3: V_1 (2V/div)

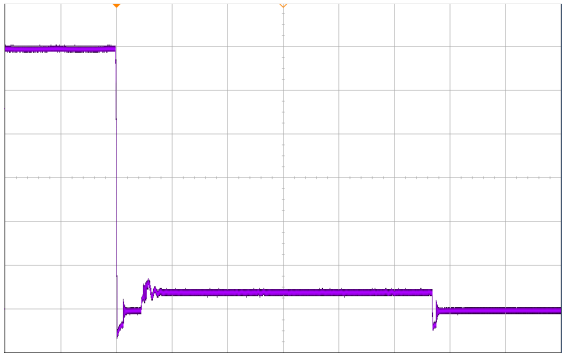


Figure 8 - AC drop out 10ms (10ms/div), 75% load
CH1: Vin (500V/div) CH3: V_1 (2V/div) CH4: V_{SB} (2V/div)

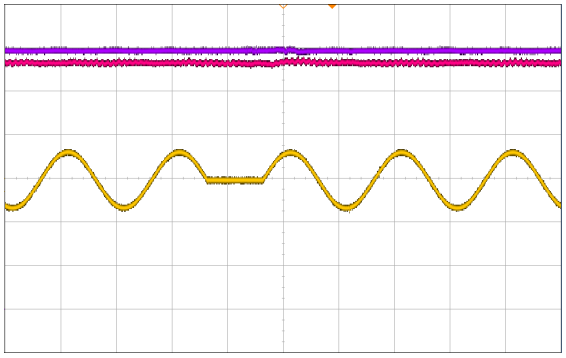


Figure 9 - Load transient V_1, 53 to 133A (1ms/div)
CH3: V_1 (2V/div) CH4: V_{SB} (2V/div)

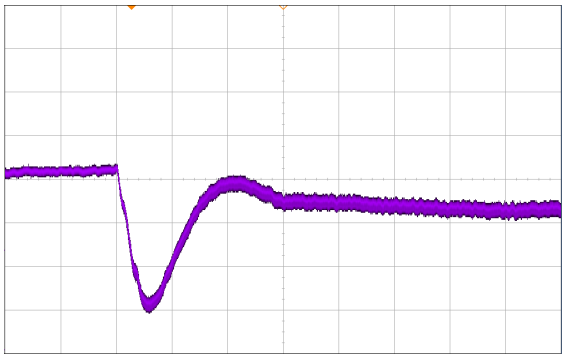
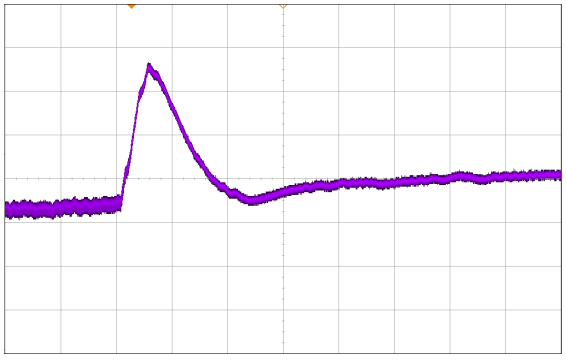


Figure 10 - Load transient V_1, 133 to 53A (1ms/div)
CH3: V_1 (2V/div) CH4: V_{SB} (2V/div)



5.1 OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in *Figure 11*. Alternatively separated ground signals can be used as shown in *Figure 12*. In this case the two ground planes should be connected together at the power supplies ground pins.

NOTE: Within the power supply the output GND pins are connected to the Chassis, which in turn is connected to the Protective Earth terminal on the AC inlet. Therefore it is not possible to set the potential of the output return (GND) to any other than Protective Earth potential.

Figure 11 – Common low impedance ground plane

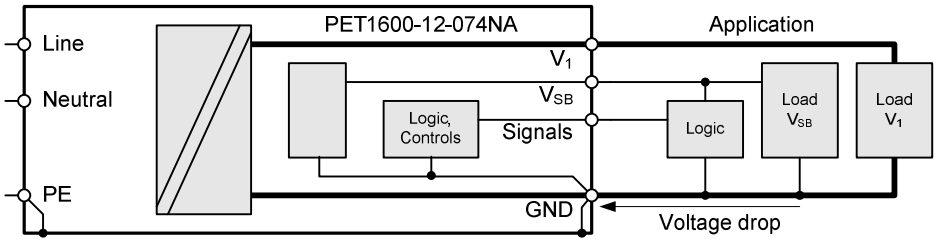
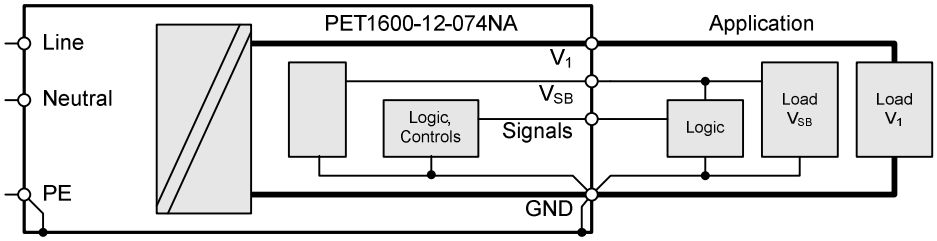


Figure 12 – Separated power and signal ground



6 PROTECTION

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input fuse (L)	Not use accessible, time-lag (T)		16		A
$V_{1\ OV}$	OV Threshold V_1	Over Voltage V_1 Protection, Latch-off Type	13.3	13.9	14.5	VDC
$t_{V1\ OV}$	OV Trip Time V_1				1	ms
$V_{VSB\ OV}$	OV Threshold V_{SB}	Over Voltage V_1 Protection, Automatic retry each 1s	13.3	13.9	14.5	VDC
$t_{VSB\ OV}$	OV Trip Time V_{SB}				1	ms
$I_{V1\ OC\ Slow}$	OC Limit V_1	Over Current Limitation, Latch-off, $V_{i\ min\ HL}$ to $V_{i\ max\ HL}$	135		140	ADC
		Over Current Limitation, Latch-off, $V_{i\ min\ LL}$ to $V_{i\ max\ LL}$	85		88	ADC
$t_{V1\ OC\ Slow}$	OC Trip time V_1	Over Current Limitation, Latch-off time	20			s
$I_{V1\ OC\ Fast}$	Fast OC Limit V_1	Fast Over Current Limit., Latch-off, $V_{i\ min\ HL}$ to $V_{i\ max\ HL}$	175		180	ADC
		Fast Over Current Limit., Latch-off, $V_{i\ min\ LL}$ to $V_{i\ max\ LL}$	110		115	ADC
$t_{V1\ OC\ Fast}$	Fast OC Trip time V_1	Fast Over Current Limitation, Latch-off time	50		60	ms
$I_{V1\ SC}$	Max Short Circuit Current V_1	V_1 < 3V			180	A
$t_{V1\ SC}$	Short Circuit Regulation Time	V_1 < 3V, time until I_{V1} is limited to < $I_{V1\ sc}$			2	ms
$I_{VSB\ OC}$	OC Limit V_{SB}	Over Current Limitation, Constant-Current Type	4		5	A
$t_{VSB\ OC}$	OC Trip time V_{SB}	Over Current Limit., time until I_{VSB} is limited to $I_{VSB\ OC}$			10	ms
T_{SD}	Over Temperature On Heat Sinks	Automatic shut-down		115		°C

6.1 OVERVOLTAGE PROTECTION

The PET1600-12-074NA front-end provides a fixed threshold overvoltage (OV) protection implemented with a HW comparator for both the main and the standby output. Once an OV condition has been triggered on the main output, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input. The standby output will continuously try to restart with a 1 s interval after OV condition has occurred.

6.2 UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored. LED and PWOK_H pin signal if the output voltage exceeds ±5% of its nominal voltage.

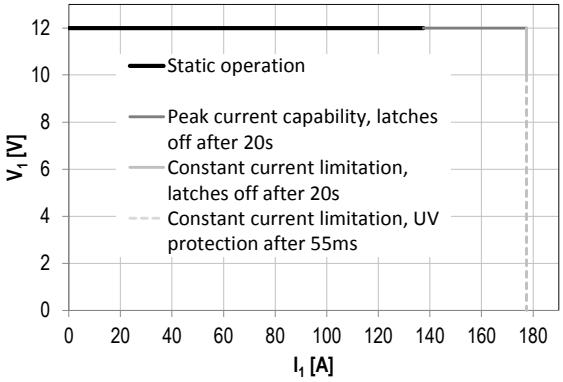
The main output will latch off if the main output voltage V_1 falls below 10V (typically in an overload condition) for more than 55 ms. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input.

6.3 CURRENT LIMITATION

MAIN OUTPUT

The main output exhibits a substantially rectangular output characteristic controlled by a software feedback loop. If output current exceeds $I_{V1\ OC\ Fast}$ it will reduce output voltage in order to keep output current at $I_{V1\ OC\ Fast}$. If the output voltage drops below ~10.0 VDC for more than 55 ms, the output will latch off (standby remains on), see also *chapter 6.2*.

Figure 13 - Current Limitation on V_1 (V_i = 230VAC)



A second SW controlled current limit will latch off the main output if the power supply is operated for long duration in its peak current capability region. This protection trips as soon as the output current exceeds $I_{V1\ OC\ Slow}$ for duration of more than 20 s.

The third current limitation implemented as a fast hardware circuit will immediately switch off the main output if the output current increases beyond the peak current trip point, occurring mainly if a short circuit is applied to the output voltage. The supply will re-start 4 ms later with a soft start, if the short circuit persists (V_1 < 10.0V for >55 ms) the output will latch off; otherwise it continuous to operate.

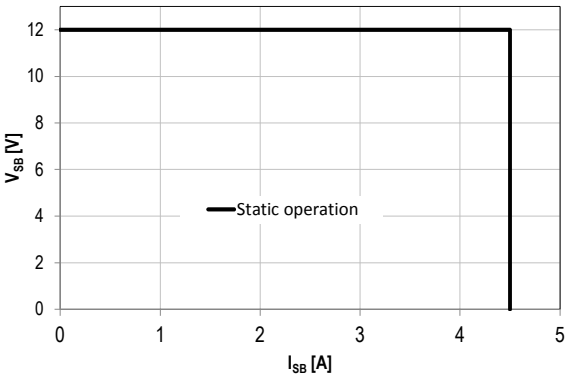
The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input.

The main output current limitation thresholds depend on the actual input applied to the power supply.

STANDBY OUTPUT

The standby output exhibits a substantially rectangular output characteristic down to 0V (no hiccup mode / latch off). The current limitation of the standby output is independent of the AC input voltage.

Figure 14 - Current Limitation on V_{SB}



7 MONITORING

The power supply operating parameters can be accessed through I²C interface. For more details refer to chapter I²C / PMBus COMMUNICATION and document URP.00234 (PET1600-12-074NA PMBus Communication Manual).

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ mon}$	Input RMS Voltage	$V_{i\ min\ LL} \le V_i \le V_{i\ max\ HL}$	-2		+2	VAC
$I_{i\ mon}$	Input RMS Current	$I_i > 6.7A_{rms}$	-3		+3	%
		$I_i \le 6.7A_{rms}$	-0.2		+0.2	A_{rms}
$P_{i\ mon}$	True Input Power	$P_i > 250W$	-4		+4	%
		$P_i < 250W$	-10		+10	W
$V_{1\ mon}$	V_1 Voltage		-0.1		+0.1	VDC
$I_{1\ mon}$	V_1 Current	$I_1 > 25A$	-1		+1	%
		$I_1 \le 25A$	-0.25		+0.25	ADC
$P_{1\ nom}$	V_1 Output Power	$P_i > 250W$	-2		+2	%
		$P_i < 250W$	-5		+5	W
$V_{SB\ mon}$	V_{SB} Voltage		-0.1		+0.1	VDC
$I_{SB\ mon}$	V_{SB} Current		-0.1		+0.1	ADC
$T_{A\ mon}$	Inlet Temperature	$T_{A\ min} \le T_A \le T_{A\ max}$	-2		+2	°C

8 SIGNALLING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
PSON_H / HOTSTANDBYEN_H						
V_{IL}	Input Low Level Voltage	PSON_L: Main output enabled HOTSTANDBYEN_H: Hot Standby mode not allowed	-0.2		0.8	V
V_{IH}	Input High Level Voltage	PSON_L: Main output disabled HOTSTANDBYEN_H: Hot Standby mode allowed	2		3.5	V
$I_{IL,H}$	Maximum Input Sink or Source Current	V_I = -0.2V to +3.5V	-1		1	mA
$R_{pull\ up}$	Internal Pull up Resistor to internal 3.3V			10		kΩ
R_{LOW}	Maximum external Pull down Resistance to GND to obtain Low Level				1	kΩ
R_{HIGH}	Minimum external Pull down Resistance to GND to obtain High Level		50			kΩ
PWOK_H						
V_{OL}	Output Low Level Voltage	$Vi < V_{i\ min\ LL}$, V_{Isink} < 4mA	0		0.4	V
V_{OH}	Output High Level Voltage	$Vi > V_{i\ min\ LL}$, I_{source} < 0.5mA	2.4		3.5	V
$R_{pull\ up}$	Internal Pull up Resistor to internal 3.3V			1		kΩ
I_{OL}	Maximum Sink Current	V_O < 0.4V			4	mA

8.2 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires in both positive and negative path. The maximum allowed voltage drop is 200 mV on the positive rail and 100 mV on the GND rail.

With open sense inputs the main output voltage will rise by 270 mV. Therefore if not used, these inputs should be connected to the power output and GND at the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.3 CURRENT SHARE

The PET front-ends have an active current share scheme implemented for V_1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

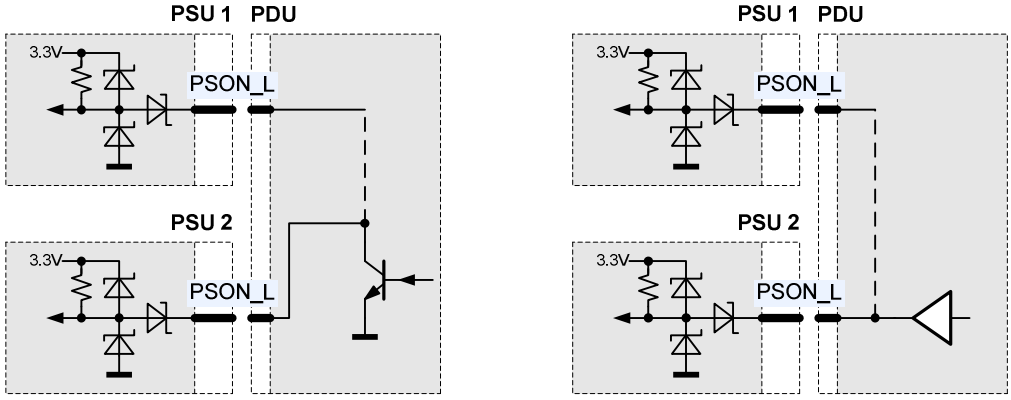
The current share function uses an analog bus to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.

The standby output uses a passive current share method (droop output voltage characteristic).

8.4 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V_1 of the front-end. With low level input the main output is enabled. This active-low pin is also used to clear any latched fault condition. The PSON_L can be either controlled by an open collector device or by a voltage source.

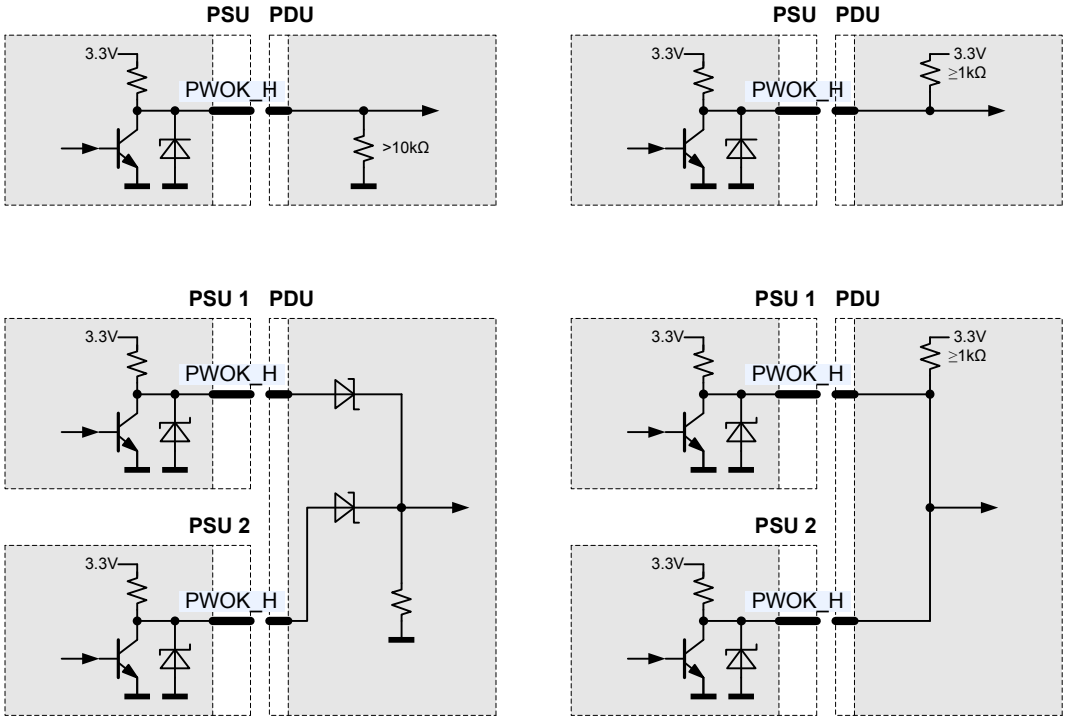
Figure 15 – PSON_H connection



8.5 PWOK_H OUTPUT

The PWOK_H is an open drain output with an internal pull-up to 3.3 V indicating whether both V_{SB} and V_1 outputs are within regulation. This pin is active-low.

Figure 16 – PWOK_H connection



8.6 HOT-STANDBY IN-/OUTPUT

The hot-standby operation is an operating mode allowing to further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable its DC/DC stage. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having a better efficiency. In order to enable the hot standby operation, the HOTSTANDBYEN_H and the ISHARE pins need to be interconnected. A power supply will only be allowed to enter the hot-standby mode, when the HOT-STANDBYEN_H pin is high, the load current is low (see *Figure 17*) and the supply was allowed to enter the hot-standby mode by the system controller via the appropriate I²C command (by default disabled). The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby mode.

If a power supply is in a fault condition, it will pull low its active-high HOTSTANDBYEN_H pin which indicates to the other power supply that it is not allowed to enter the hot-standby mode or that it needs to return to normal operation should it already have been in the hot-standby mode.

NOTE: The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby mode.

Figure 18 shows the achievable power loss savings when using the hot-standby mode operation. A total power loss reduction of 45% is achievable.

Figure 17 - Hot-standby enable/disable current thresholds

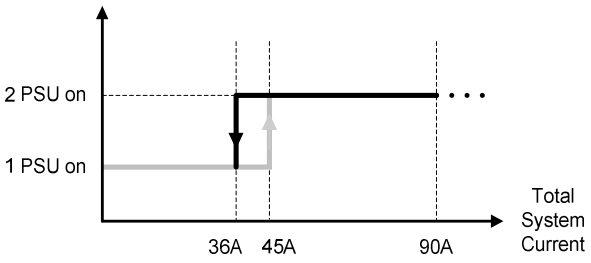


Figure 18 - PSU power losses with/without hot-standby mode

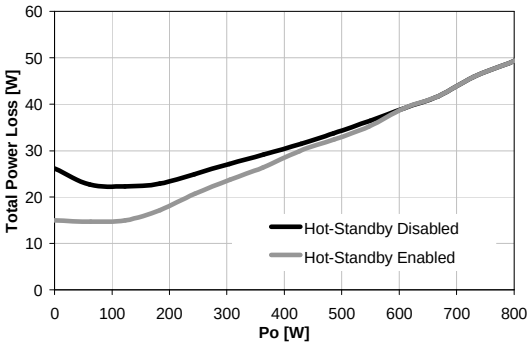
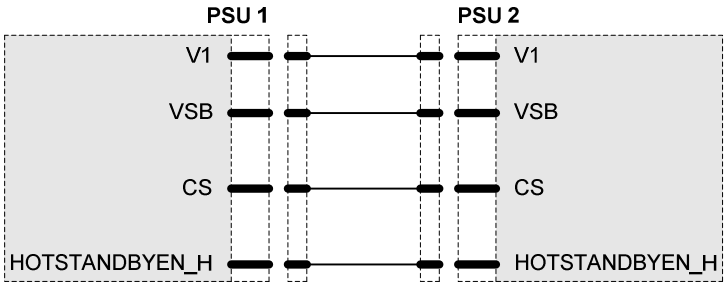


Figure 19 - Recommended hot-standby configuration



8.7 SIGNAL TIMING

Figure 20 – AC turn-on timing

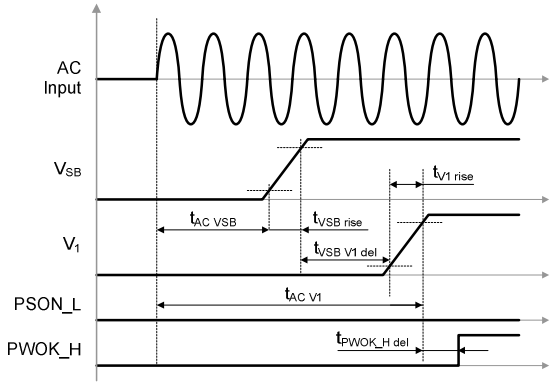


Figure 21 - AC short dips

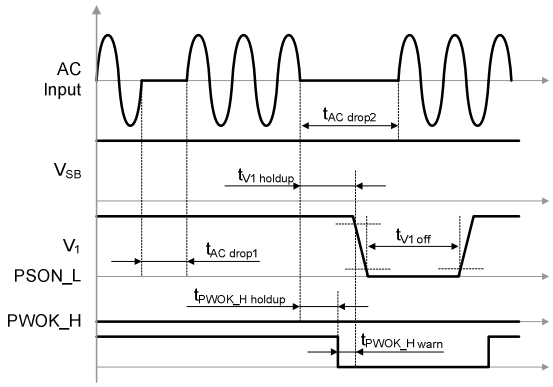


Figure 22 - AC long dips

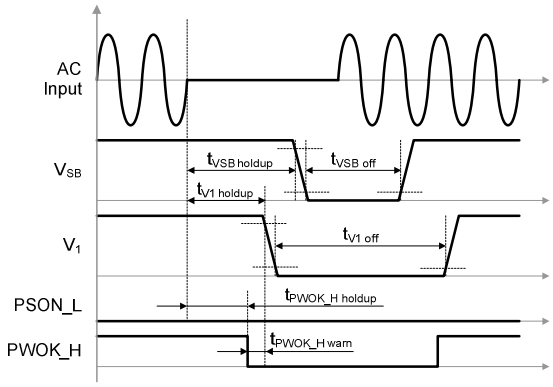
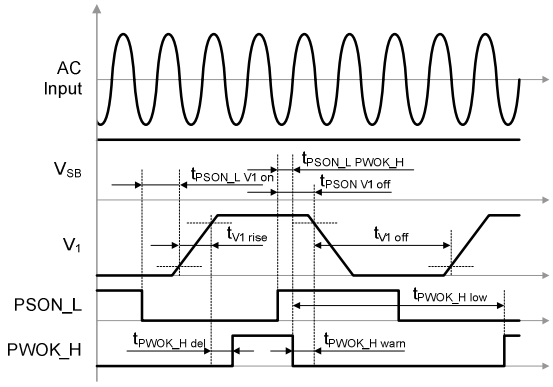


Figure 23 - PSON_L turn-on/off timing



PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$t_{AC\ VSB}$	AC Line to 90% V_{SB}				1.5	s
$t_{AC\ V1}$	AC Line to 90% V_1	PSON_L = Low			3	s
$t_{VSB\ V1\ del}$	V_{SB} to V_1 delay	PSON_L = Low	50		1000	ms
$t_{V1\ rise}$	V_1 rise time	See chapter *OUTPUT*				
$t_{VSB\ rise}$	V_{SB} rise time	See chapter *OUTPUT*				
$t_{AC\ drop1}$	AC drop without V_1 leaving regulation	0.7 · $I_{1\ nom}$, $I_{SB\ nom}$			10	ms
$t_{AC\ drop2}$	AC drop without V_{SB} leaving regulation	$I_{1\ nom}$, $I_{SB\ nom}$			70	ms
$t_{V1\ holdup}$	Loss of AC to V_1 leaving regulation	See chapter *INPUT*				
$t_{VSB\ holdup}$	Loss of AC to V_1 leaving regulation	See chapter *INPUT*				
$t_{PWOK\_H\ del}$	Outputs in regulation to PWOK_H asserted		100		500	ms
$t_{PWOK\_H\ warn}$	Warning time from de-assertion of PWOK_H to V_1 leaving regulation		1			ms
$t_{PWOK\_H\ holdup}$	Loss of AC to PWOK_H de-asserted		10.6			ms
$t_{PWOK\_H\ low}$	Time PWOK_H is kept low after being de-asserted		100			ms
$t_{PSON\_L\ V1\ on}$	Delay PSON_L active to V_1 in regulation		5		400	ms
$t_{PSON\_L\ V1\ off}$	Delay PSON_L de-asserted to V_1 disabled			TBD		ms
$t_{PSON\_L\ PWOK\_H}$	Delay PSON_L de-asserted to PWOK_H de-asserted				5	ms
$t_{V1\ off}$	Time V_1 is kept off after leaving regulation			1		s
$t_{VSB\ off}$	Time V_{SB} is kept off after leaving regulation			1		s

8.8 LED INDICATOR

The front-end has one front LED showing the status of the supply. The LED is bi-colored: green and amber, and indicates AC and DC power presence and warning or fault conditions. *Table 1* lists the different LED status.

Table 1 - LED Status

OPERATING CONDITION [1]	LED SIGNALING
No AC or AC Line in UV condition, V_{SB} not present from paralleled power supplies	Off
PSON_L High	Blinking Green 1Hz
Hot-Standby Mode	
No AC or AC Line in UV condition, V_{SB} present from paralleled power supplies	Solid Amber
V_1 or V_{SB} out of regulation	
Over temperature shutdown	
Output over voltage shutdown (V_1 or V_{SB})	
Output over current shutdown (V_1 or V_{SB})	
Fan error (>15%)	
Over temperature warning	Blinking Amber 1Hz
Minor fan regulation error (>5%, <15%)	
Firmware bootloading in process	Blinking Green 2Hz
Outputs V1 and VSB in regulation	Solid Green

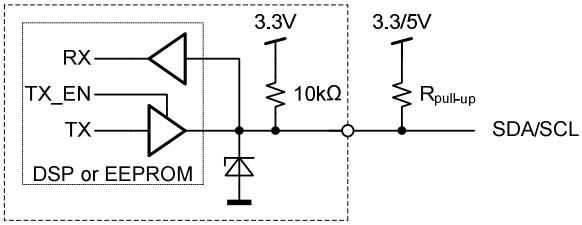
[1] The order of the criteria in the table corresponds to the testing precedence in the controller.

9 I²C / PMBus COMMUNICATION

The PET front-end is a communication Slave device only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and timing is defined in *Table 2* further characterized through:

- The SDA/SCL IOs use 3.3V logic levels
- External pull-up resistors on SDA/SCL required for correct signal edges
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

Figure 24 - Physical layer of communication interface



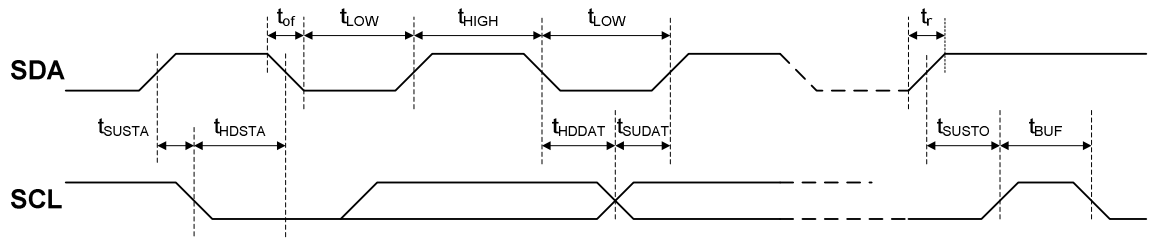
Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a live V_{SB} output (provided e.g. by the redundant unit). If only V_1 is provided, communication is not possible.

Table 2 - I²C / SMBus Specification

PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
SCL / SDA					
V_{iL}	Input low voltage		-0.5	1.0	V
V_{iH}	Input high voltage		2.3	3.5	V
V_{hys}	Input hysteresis		0.15		V
V_{oL}	Output low voltage	3 mA sink current	0	0.4	V
t_r	Rise time for SDA and SCL		20+0.1C_b[1]	300	ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[1] < 400 pF	20+0.1C_b[1]	250	ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
$R_{pull-up}$	External pull-up resistor	f_{SCL} ≤ 100 kHz		1000 ns / C_b[1]	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5		ms

[1] Cb = Capacitance of bus line in pF, typically in the range of 10…400pF

Figure 25 - I²C / SMBus Timing



9.1 ADDRESS SELECTION

The address for I²C communication can be configured by pulling address input pins A1 and A0 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor will cause the A1 / A0 pin to be in High Level if left open. A fixed addressing offset exists between the Controller and the EEPROM.

Table 3 - Address and protocol encoding

A1	A0	I2C Address [1]	
		Controller	EEPROM
0	0	0xB0	0xA0
0	1	0xB2	0xA2
1	0	0xB4	0xA4
1	1	0xB6	0xA6

[1] The LSB of the address byte is the R/W bit.

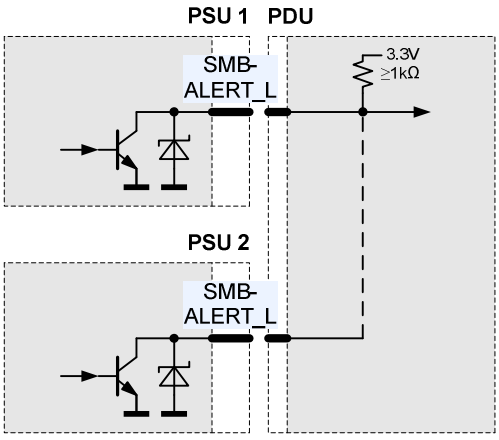
9.2 SMBALERT_L OUTPUT

The SMBALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, general failure, over-current, over-voltage, under-voltage or low-speed of failed fan. This signal may also indicate the power supply is operating in an environment exceeding the specified limits.

The SMBAlert signal is asserted simultaneously with the LED turning to solid amber or blinking amber.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
SMB_ALERT_L						
V_{ext}	Maximum External Pull up Voltage				12	V
I_{OH}	Maximum High Level Leakage Current	No Failure or Warning condition, V_O = 12V			10	µA
V_{OL}	Output Low Level Voltage	Failure or Warning condition, I_{sink} < 4mA	0		0.4	V
$R_{pull\ up}$	Internal Pull up Resistor to internal 3.3V			None		
I_{OL}	Maximum Sink Current	V_O < 0.4V			4	mA

Figure 26 – SMBALERT_L connection

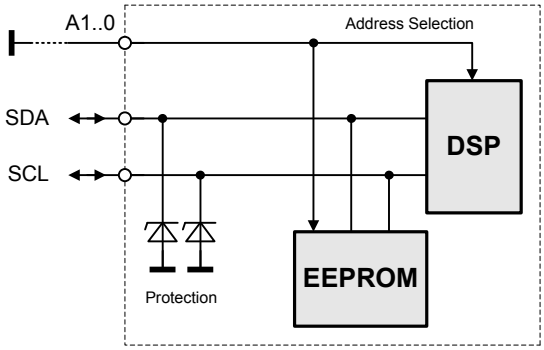


9.3 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I²C bus physical layer (see *Figure 27*) and can be accessed under different addresses, see *ADDRESS SELECTION*. The SDA/SCL lines are connected directly to the controller and EEPROM which are supplied by internal 3.3V.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

Figure 27 - I²C Bus to DSP and EEPROM



9.4 EEPROM PROTOCOL

The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.

9.5 PMBus™ PROTOCOL

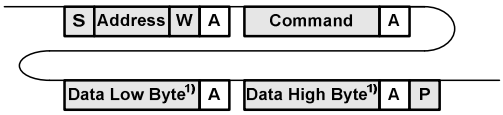
The Power Management Bus (PMBus™) is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at : www.powerSIG.org.

PMBus™ command codes are not register addresses. They describe a specific command to be executed. The PET1600-12-074NA supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

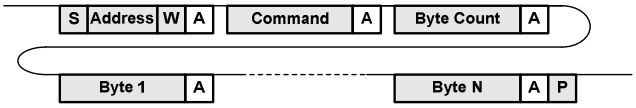
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



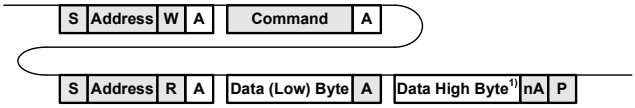
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See PET1600-12-074NA PMBus Communication Manual URP.00234 for further information.



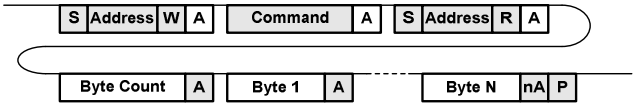
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes. See PET1600-12-074NA PMBus Communication Manual URP.00234 for further information.



9.6 GRAPHICAL USER INTERFACE

Power-One provides with its “Power-One I²C Utility” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PET1600-12-074NA Front-End. The utility can be downloaded on: www.power-one.com and supports both the PSMI and PMBus™ protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

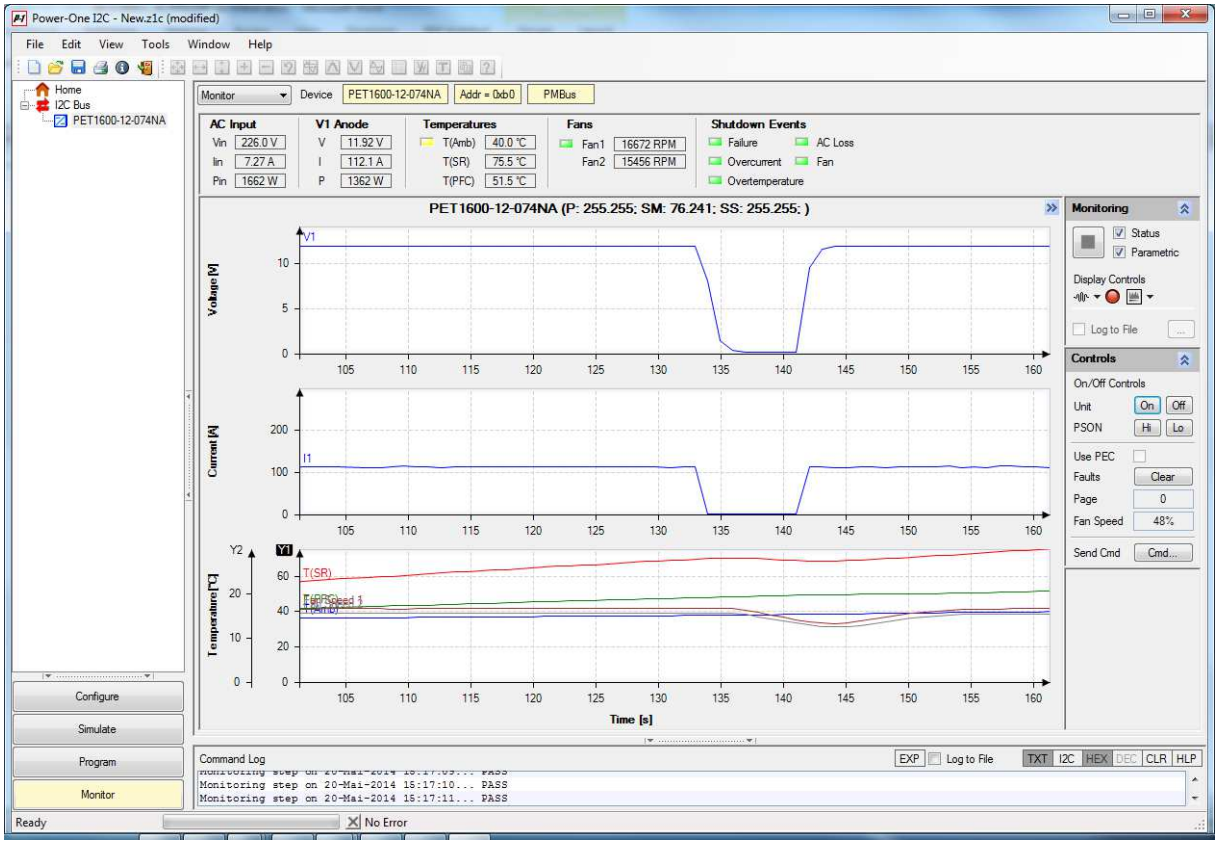
If the GUI is used in conjunction with the YTM.00045 Evaluation Board it is also possible to control the PSON_L pin(s) of the power supply.

Further there is a button to disable the internal fan for approximately 10 seconds. This allows the user to take input power measurements without fan consumptions to check efficiency compliance to the Climate Saver Computing Platinum specification.

The monitoring screen also allows to enable the hot-standby mode on the power supply. The mode status is monitored and by changing the load current it can be monitored when the power supply is being disabled for further energy savings. This obviously requires 2 power supplies being operated as a redundant system (as in the evaluation kit).

NOTE: The user of the GUI needs to ensure that only one of the power supplies have the hot-standby mode enabled.

Figure 28 - Monitoring dialog of the I²C Utility



10 TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PET1600-12-074NA is provided with a rear to front airflow, which means the air enters through the DC-output of the supply and leaves at the AC-inlet. The PET1600-12-074NA supply has been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

The PET1600-12-074NA provides access via I²C to the measured temperatures of in total 6 sensors within the power supply, see *Table 4*. The microprocessor is monitoring these temperatures and if warning threshold of one of these sensors is reached it will set fan to maximum speed. If temperatures continue to rise above shut down threshold the main output V_1 (or V_{SB} if auxiliary converter is affected) will be disabled. At the same time the warning or fault condition is signalized accordingly through LED, PWOK_H and SMBALERT_L.

Table 4 – Temperature sensor location and thresholds

TEMPERATURE SENSOR	DESCRIPTION / CONDITION	PMBus register	Warning threshold	Shut down threshold
Inlet air temperature	Sensor located on control board close to DC end of power supply	8Dh	TBD	TBD
Synchronous rectifier	Sensor located on secondary side of DC/DC stage	8Eh	TBD	TBD
Primary heat sink	Sensor located on primary heat sink	8Fh	TBD	TBD
Output oring element	Sensor located close to output	D1h	TBD	TBD
Auxiliary converter	Sensor located on secondary side on auxiliary rectifier	D2h	TBD	TBD
Bridge rectifier	Sensor located on heat sink for AC rectifier	D3h	TBD	TBD

Figure 29 - Airflow direction

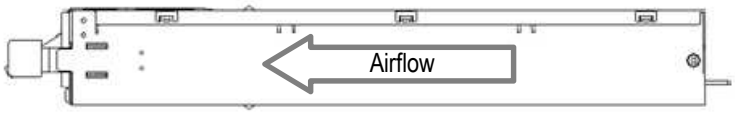


Figure 30 - Fan speed vs. main output load

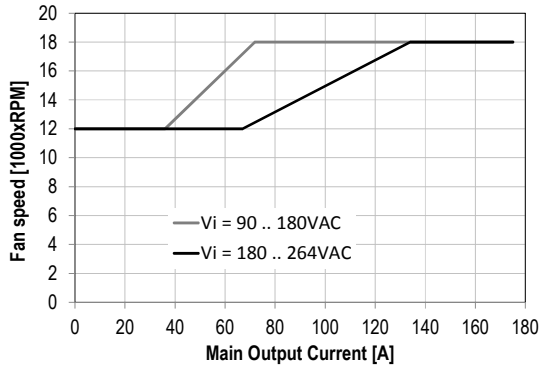
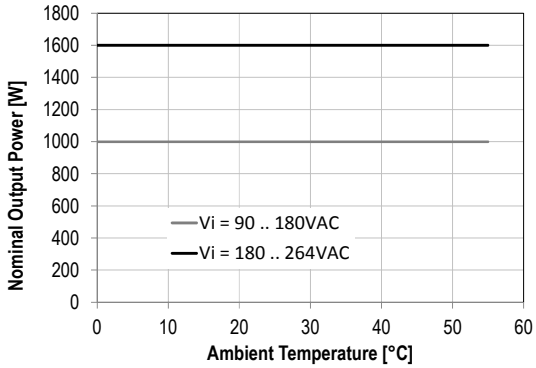


Figure 31 - Thermal derating



11 ELECTROMAGNETIC COMPATIBILITY

11.1 IMMUNITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LED, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetics Filed	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1µs Pulse Modulation, 10 kHz ... 2 GHz	A
Burst	IEC / EN 61000-4-4, Level 3 AC port ±2 kV, 1 minute	A
Surge	IEC / EN 61000-4-5, Level 3 Line to Earth: ±2 kV Line to Line: ±1 kV	A
RF Conducted Immunity	IEC / EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 … 80 MHz	A
Voltage Dips and Interruptions	IEC / EN 61000-4-11 1. Vi 230VAC, 70% load, Phase 0°, Dip 100% , duration 10.6 ms 2. Vi 230VAC, 70% load, Phase 0°, Dip 100% , duration 70 ms 3. Vi 230VAC, 70% load, Phase 0°, Dip 100% , duration100 ms	V_1: A, V_{SB}: A V_1: B, V_{SB}: A V_1: B, V_{SB}: B

11.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN 55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, single power supply	Class B 6 dB margin
	EN 55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, 2 power supplies in a system	Class B 6 dB margin
Radiated Emission	EN 55022 / CISPR 22: 30 MHz … 1 GHz, QP, single power supply	Class B 6 dB margin
	EN 55022 / CISPR 22: 30 MHz … 1 GHz, QP, 2 power supplies in a system	Class B 6 dB margin
Harmonic Emissions	IEC 61000-3-2, Vi = 115 VAC / 60 Hz & 230 VAC / 50 Hz, 100% Load	Class A
AC Flicker	IEC 61000-3-3, Vi = 230 VAC / 50Hz, 100% Load	Pass
Acoustical Noise	Distance 1 meter, 25°C, 50% Load	46 dBA

12 SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Power-One will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	UL 60950-1 2nd Edition CAN/CSA-C22.2 No. 60950-1-07 2nd Edition IEC 60950-1:2005 EN 60950-1:2006	Approved by nt body claration)
Isolation Strength	Input (L/N) to chassis (PE)	Basic
	Input (L/N) to output	*Reinforced*
	Output to chassis	None (Direct connection)
Creepage / Clearance	Primary (L/N) to chassis (PE)	According to safety standards
	Primary to secondary	
Electrical Strength Test	Input to chassis / Input to output	

Safety approvals pending

13 ENVIRONMENTAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_A	Ambient Temperature	Up to 1'000m ASL	0		+55	°C
		Linear derating from 1'000 to 3'048m ASL			+45	°C/
T_{Aext}	Extended Temp. Range				TBD	°C
T_S	Storage Temperature	Non-operational	-20		+70	°C
	Altitude	Operational, above Sea Level	-		3'048	m
		Non-operational, above Sea Level	-		10'600	m
	Shock, operational	Half sine, 11ms, 10 shocks per direction, 6 directions			1	g peak
	Shock, non-operational				30	g peak
	Vibration, sinusoidal, operational	IEC/EN 60068-2-6, sweep 5 to 500 to 5 Hz, 1 octave/min, 5 sweep per axis			1	g peak
	Vibration, sinusoidal, non-operational				4	g peak
	Vibration, random, non-operational	IEC/EN 60068-2-64, 5 to 500 Hz, 1 hour per axis			0.025	g^2/Hz
N_a	Audible noise			TBD		dBA

14 RELIABILITY

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
MTBF	Mean time to failure	T_A = 25°C, V_i = 230VAC, 0.7 · $I_{1\ nom}$, $I_{SB\ nom}$	500			kh
	Expected life time	T_A = 25°C, V_i = 230VAC, 0.7 · $I_{1\ nom}$, $I_{SB\ nom}$		TBD		years
		T_A = 55°C, V_i = 230VAC, $I_{1\ nom}$, $I_{SB\ nom}$	TBD			

15 MECHANICAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions	Width		73.5		mm
		Heigth		40.0		mm
		Depth		265.0		mm
m	Weight			1.1		kg

Figure 32 – Top and side view

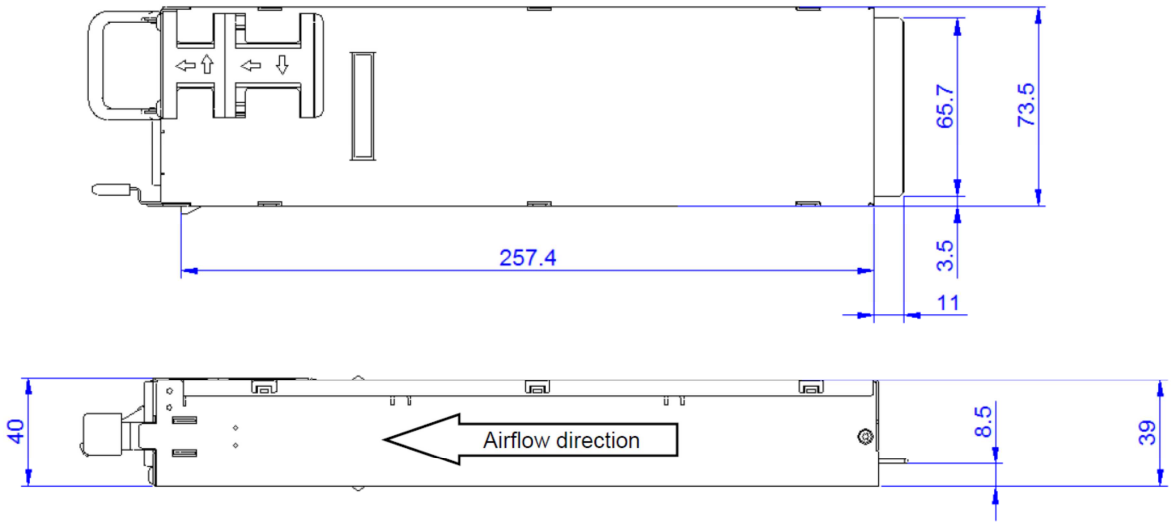


Figure 33 – Front view

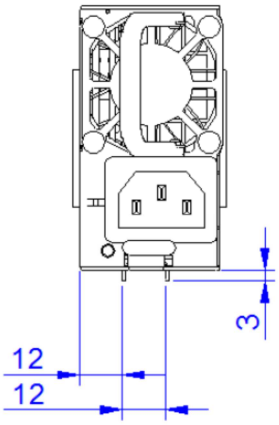
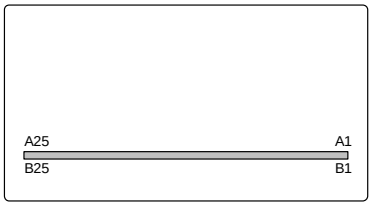


Figure 34 – Rear view



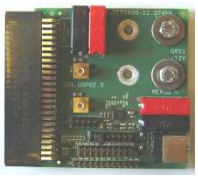
16 CONNECTORS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	AC inlet	IEC 60320 C14				
	AC cord requirement	Wire size		16		AWG
	Output connector	25-Pin PCB card edge				
	Mating output connector	FCI 10035388-106 or equivalent				

Figure 35 – Output connector pin assignment

PIN	SIGNAL NAME	DESCRIPTION
A1 ~ A9	GND	Power and signal ground (return)
B1 ~ B9	GND	
A10 ~ A18	V1	+12VDC main output
B10 ~ B18	V1	
A19	SDA	I^2C data signal line
A20	SCL	I^2C clock signal line
A21	PSON_L	Power supply on input, active-low
A22	SMB_ALERT_L	SMB Alert signal output, active-low
A23	V1_SENSE_R	Main output negative sense
A24	V1_SENSE	Main output positive sense
A25	PWOK_H	Power OK signal output, active-high
B19	A0	I^2C address selection input
B20	A1	
B21	VSB	+12V Standby positive output
B22	HOTSTANDBYEN_H	Hot standby enable signal, active-high
B23	ISHARE	Analog current share bus
B24	Reserved	For future use, keep open circuit
B25	Reserved	For future use, keep open circuit

17 ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**Power-One I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor PET1600-12-074NA Front-Ends (and other I²C units)	N/A	www.power-one.com
	**Evaluation Board** Connector board to operate PET1600-12-074NA. Includes an on-board USB to I²C converter (use *Power-One I²C Utility* as desktop software).	YTM.00045	Power-One

NUCLEAR AND MEDICAL APPLICATIONS - Power-One products are not designed, intended for use in, or authorized for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems without the express written consent of the respective divisional president of Power-One, Inc.

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